UNIVERSITY OF CALIFORNIA
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III-Nitride Blue Laser Diode with Photoelectrochemically Etched Current Aperture

A dissertation submitted in partial satisfaction of the

requirements for the degree

Doctor of Philosophy in Materials

by

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December 2015

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Ludovico Megalini

To my late father Domenico,

my mum Giovanna and my sister Mariarosaria

“La fatica non è mai sprecata. Soffri ma sogni”
(“Working hard is never wasted. You suffer but in the meantime you dream”)

Pietro Mennea,
Olympic and World Champion 200 m even runner

“We no longer have the learning of the ancients, the age of giants is past!”
“We are dwarf”, William admitted, “but dwarf who stand on the shoulders of those giants, and small though we are, we sometimes manage to see farther on the horizon than they.”

The Name of the Rose, Umberto Eco

“And anytime you feel the pain, hey Jude, refrain
Don't carry the world upon your shoulders”

Hey Jude, The Beatles

ACKNOWLEDGEMENTS

A PhD title, although it is awarded to a single student, is never, in general, the recognition of the relatively hard work of just a single student but it is instead the result of a myriad of contributions, hints, advice and suggestions of several people, and, last but not least, luck.

Indeed, I feel I have been extremely lucky in the past years to be a graduate student at UCSB and to have had the chance to work in one of the leading centers for nitride research, and even luckier for having the opportunity to work with many knowledgeable people who were kind enough to share their knowledge and expertise in many different fields.

First of all, I would like to thank my advisor Prof. Steven P. DenBaars for accepting me in his research group. I am not sure why he did so, as he receives, almost every day, a similar request from many smart American and Asian students coming from the most prestigious American and world universities, as I did not have any supporting scholarship in a time when all the universities were struggling to look for funding, and finally because I started my PhD at an age when PhD students are, in general, going to graduate. I hope that this work repays, at least in part, all the support, encouragement and advice, that he gave me. The fact that he is a successful manager, a MOCVD world expert and has set up a great MOCVD lab, is definitely something to mention and which I will utilize as an example to follow.

I want to thank also the other members of my Committee: Prof. Bowers, Prof. Mishra, Prof. Nakamura, Prof. Speck and Dr. Cohen. I have had the chance to interact in different degrees with all of them so I am grateful to all of them for sharing their ideas and thoughts with me. In particular, Prof. Bowers who provided some important insights for the estimation of the roughness-induced scattering loss analysis.

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I would like to thank the Fulbright Commission for helping me get to UCSB. Although I have been essentially funded entirely by the SSLEEC, I got my MSc (and the first months of my PhD) thanks to a Fulbright-Finmeccanica scholarship. I will never forget that sunny morning of July, about five years ago, when my cell phone rang and from the other side a voice said: "Mr. Megalini? I am from the Fulbright Commission in Rome and I am glad to announce that you are the winner of the Fulbright-Finmeccanica scholarship for this year". In particular, Dr. Barbara Pizzella has been very kind in assisting me in filing all the required documents and incredibly patient in answering all my doubts and questions. Carlo Musso of Finmeccanica was also available when necessary.

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Finally, I do want to thank my family: my late father Domenico, my mother Giovanna and my sister Mariarosaria for all the invaluable support they have given me throughout the years. That support cannot ever be overrated and my gratitude is beyond words!!

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2. L. Megalini, L.Y. Kuritzky, J.T. Leonard, R. Shenoy, K. Rose, S. Nakamura, J.S. Speck, D.A. Cohen, S.P. DenBaars, *Selective and controllable lateral photoelectrochemical etching of nonpolar and semipolar InGaN/GaN multiple quantum well active regions,* Appl. Phys. Express **8** (**6**), 066502, 2015.

3. L. Megalini, R. Shenoy, K. Rose, J.P. Speck, J. E. Bowers, S. Nakamura, D.A. Cohen, S.P. DenBaars, *Estimation of roughness-induced scattering losses in III-Nitride laser diodes with a photoelectrochemically etched current aperture,* Physica Status Solidi A (under review)

4. L. Megalini, D.S. Saito, E.J. Garcia, A.J. Hart and B.L. Wardle, *Impedance of Aligned Carbon Nanotube Arrays and Polymeric Nanocomposites*, Journal of Nano Systems & Technology, **1**, 1, 2009.

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AWARDS

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ABSTRACT

III-Nitride Blue Laser Diode with Photoelectrochemically Etched Current Aperture

by

Ludovico Megalini

Group III-nitride is a remarkable material system to make highly efficient and high-power optoelectronics and electronic devices because of the unique electrical, physical, chemical and structural properties it offers. In particular, InGaN-based blue Laser Diodes (LDs) have been successfully employed in a variety of applications ranging from biomedical and military devices to scientific instrumentation and consumer electronics. Recently their use in highly efficient Solid State Lighting (SSL) has been proposed because of their superior beam quality and higher efficiency at high input power density.

Tremendous advances in research of GaN semi-polar and non-polar crystallographic planes have led both LEDs and LDs grown on these non-basal planes to rival with, and with the promise to outperform, their equivalent c-plane counterparts.

However, still many issues need to be addressed, both related to material growth and device fabrication, including a lack of conventional wet etching techniques.

GaN and its alloys with InN and AlN have proven resistant essentially to all known standard wet etching techniques, and the predominant etching methods rely on chlorine-based dry etching (RIE). These introduce sub-surface damage which can degrade the electrical properties of the epitaxial structure and reduce the reliability and lifetime of the final device.

Such reasons and the limited effectiveness of passivation techniques have so far suggested to etch the LD ridges before the active region, although it is well-known that this can badly affect the device performance, especially in narrow stripe width LDs, because the gain guiding obtained in the planar configuration is weak and the low index step and high lateral current leakage result in devices with threshold current density higher than devices whose ridge is etched beyond the active region. Moreover, undercut etching of III-nitride layers has proven even more challenging, with limitations in control of the lateral etch distance.

In this dissertation it is presented the first nitride blue edge emitting LD with a photoelectrochemical etched current aperture (CA-LD) into the device active region. Photoelectrochemical etching (PECE) has emerged as a powerful wet etching technique for III-nitride compounds. Beyond the advantages of wet etching technique, PECE offers bandgap selectivity, which is particularly desirable because it allows more freedom in designing new and advanced devices with higher performances.

In the first part of this thesis a review of PECE is presented, and it is shown how it can be used to achieve a selective and controllable deep undercut of the active region of LEDs and LDs, in particular the selective PECE of MQW active region of (10-10) *m*-plane and (20-2-1) plane structures is reported.

In the second part of this thesis, the fabrication flow process of the CA-LD is described. The performance of these devices is compared with that of shallow etched ridge LDs with a nominally identical epitaxial structure and active region width and it is experimentally shown that the CA-LD design has superior performance. CW operation of a (20-2-1) CA-LD with a 1.5 μm wide active region is demonstrated.

Finally, in the third and last part of this thesis, the CA-LD performance is discussed in more details, in particular, an analysis of optical scattering losses caused by the rough edges of the remnant PEC etched active region is presented.

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Chapter 1

Introduction

1.1 Application of GaN-based blue LD for Solid State Lighting (SSL)

III-nitride semiconductors hold promise for energy efficient optoelectronics [1,2] and high-power, high-frequency electronic devices [3]. In particular, because they offer the possibility of making alloys with direct bandgaps ranging from 0.7 eV to 6.2 eV, they have enabled devices emitting from the UV to the green part of the EM spectrum, with capability to emit up in the red region.

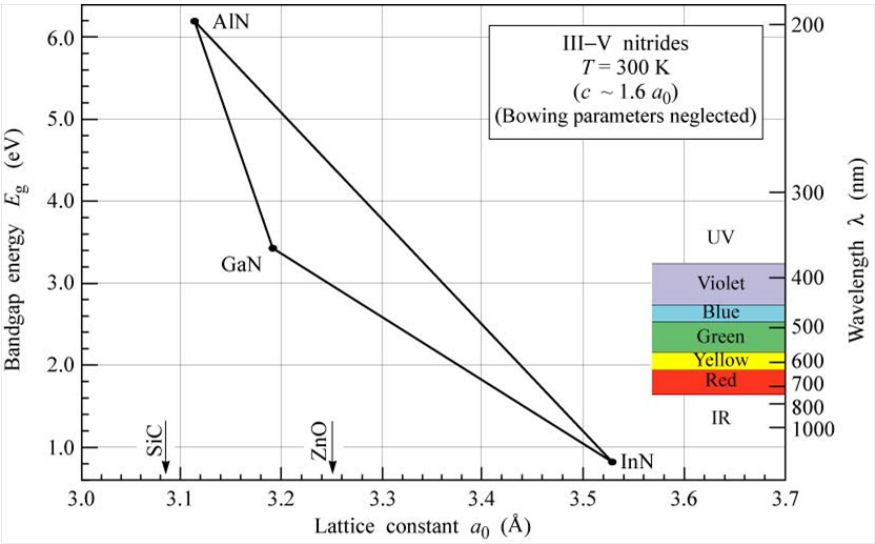

Figure 1 Bandgap energy and relative wavelength of Nitride-based devices

Figure 1 shows that AlN, GaN and InN have a relatively large difference of lattice constant, this is even more different than that of the traditional non-native substrates generally used, such as sapphire, SiC or Si. This along with other severe issues such as In incorporation [4], In fluctuation in the QW [5], cracking of high Al-content layers [6], thermal management of the different epitaxial layers during the growth [7, 8] and many others, have so far posed extremely severe challenges to the fabrication of high efficient and high power optoelectronics devices spanning the full range of possibilities allowed by this material system, causing the so-called "green gap" of high efficiency performance in the green-yellow spectral range, and on the other side of the spectrum the fabrication of low power UV devices.

On other hand, devices emitting in the violet-blue range (both LEDs and LDs) are mature and employed in a variety of commercial applications. Blue emitters are particularly appealing as they find applications not only in consumer electronics but also as pump source for solid state lighting (SSL) [9]. This is a big and profitable market: today's lighting uses

15-22% of electricity depending on the countries, with 609TWh used in the US alone in 2013 [10]. Blue LEDs with efficiency as high as ~150 lm/W are now replacing both low efficiency incandescent bulbs (15-20 lm/W – their use has been recently banned in several countries) and halogen and fluorescent lamps (~100 lm/W) as shown in Fig. 2.

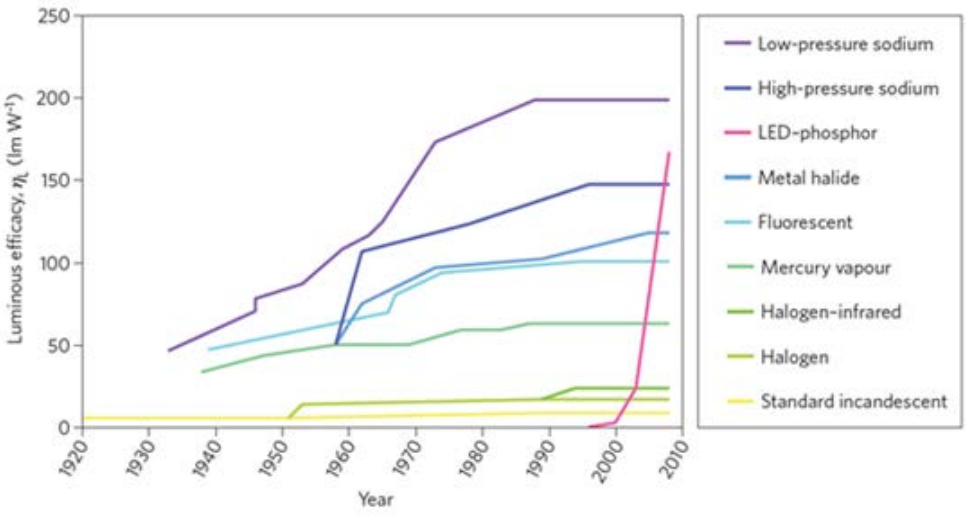

Figure 2 Historic development of the most common white-light sources [From 11]

Such high importance of nitrides for lighting has been acknowledged by the award of the 2014 Nobel prize for Physics to Shuji Namakura, Hiroshi Amano and Isamu Akasaki "*for the invention of efficient blue light emitting diodes which has enabled bright and energy saving white light sources*".

However, current LEDs are still far from their maximum theoretical efficiency (estimated to be about 350 lm/W), and more importantly they suffer from a non-thermal droop, which impedes high-performance operation at high current densities. This efficiency droop is mainly caused by the Auger-related *C* term in the widely adopted *ABC* model [12] which related the injected current *J* in the LED and the internal quantum efficiency η_{IQE} as:

$$J = q \cdot d_{MQW} \cdot \frac{(An + Bn^2 + Cn^2)}{\eta_{\text{injected}}}$$

$$\eta_{IQE} = \frac{Bn^2}{An + Bn^2 + Cn^3}$$

where q is the electron charge, d_{MQW} is the active layer (usually a MQW) thickness, η_{injected} is the injection efficiency, B is the bimolecular radiative recombination coefficient, while the non-radiative coefficients are A (Shockley-Read-Hall) and C (electron-electron-hole or electron-hole-hole Auger recombination).

Other mechanisms have been proposed as possible explanations of this phenomenon such as carrier overshoot and leakage [13] and different remedies to mitigate the problem have been suggested such as: a) increase of the active layer thickness [14], eventually by using a double-heterostructure to spread the carriers over a larger volume (this idea has the drawback of lowering the IQE as the material quality degrades for thick In-rich layers) or by increasing the number of QW (but this presents the problem of achieving a uniform carrier injection through all MQW, problem particularly exacerbated in c- plane devices) [15], c) use of nanowire LED structures as these can have a higher aspect ratio than the planar MQW leading to a larger active region area and might also allow to relieve the strain constraints for achieving the high In content needed for green-emitting devices (this solution has been currently adopted only at research laboratory levels) [16], and d) use of nonpolar (semipolar) planes which enable the elimination (mitigation) of the polarization-induced electric fields caused by the quantum-confined Stark effect (QCSE) and therefore the overlap of the electron/hole wavefunction is enhanced (this does not eliminate the droop problem, though) [17].

Another alternative solution which has spurred great interest is blue Laser Diode-(LD-) based Solid State Lighting (SSL) [18]. Already employed in a variety of applications ranging from consumer electronics to scientific instrumentations and automotive applications, LD have also been recently suggested also as the logical successors to the Light Emitting Diodes (LEDs) and their use in highly efficient Solid State Lighting has been proposed because of their superior beam quality and higher efficiency at high input power density.

When combined with phosphors, for example yttrium aluminum garnet (YAG:Ce), blue LDs can provide a more color-stable, higher power white light source than LEDs because of their narrower line width which gives the highest luminous efficacy [19]. The narrower line width had initially raised concerns about “spectral deficiencies” of LDs-based lighting compared to LEDs-based lighting. However, experimental tests have shown “slight preferences for the laser white over the warm-white and cool-white LEDs, an extremely slight preference for the laser white over the neutral-white LED”. As a consequence, the spiky spectra of LDs do not appear to be a showstopper for their application in solid state lighting [20].

One of the most important advantages of LDs with respect to LEDs is that once they have reached threshold, LDs do not suffer from the parasitic recombination mechanisms which typically affect LEDs [21]. As described previously, as the input power density increases, LEDs become less efficient: although reduced in non c-plane orientations, such efficiency droop poses severe limitations to LEDs output power. On the other hand, in LDs all the carrier-densities-related parasitic recombination mechanisms are clamped – at least to the first order both the photon and the gain compression related to hole burning are negligible – as it is possible to assume that the carriers density clamps at lasing threshold

(and as a consequence also the gain clamps). Therefore, at the lasing threshold, LDs allow a higher photon output per unit semiconductor area and they can achieve a higher cost effectiveness than LEDs. This is well illustrated in Fig. 3 which shows that the power conversion efficiency (PCE) of LDs is by far superior than LEDs at higher power densities.

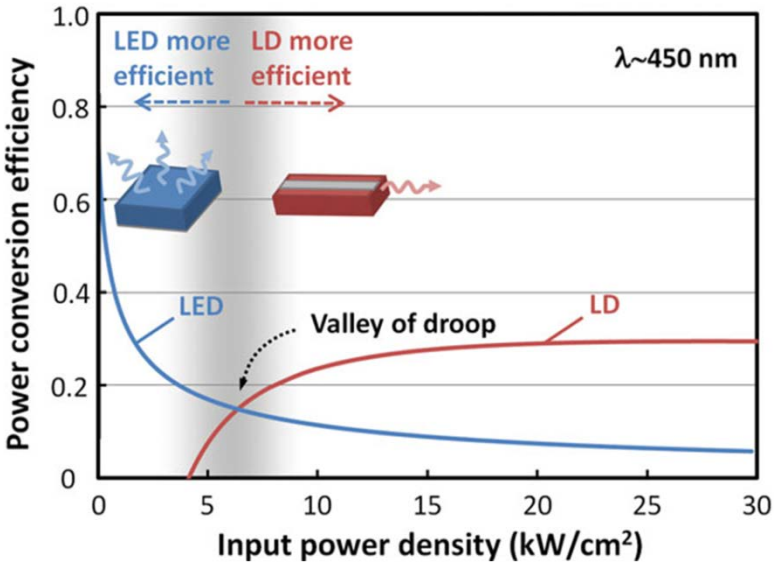

Figure 3 Comparison of Power Conversion Efficiency of LDs and LEDs [From 9]

Finally LDs deliver directional light, a feature which is appealing in several applications such as automotive (BMW has already employed laser-based headlamps in its luxury model cars) and can be ultimately used for visible light communication (also known as Li-Fi) [22].

1.2 Overview of non-polar and semipolar Nitride LDs

The earlier nitride devices and most of the current commercial are fabricated using crystal grown along the *c*- axis of the wurtzite crystal structure.

In September 1992 Nakamura fabricated the first double heterostructure-based light emitting diode which became 1 candela InGaN based LED the following year. Soon after, Nichia announced its commercial blue LED. In January 1996 Nakamura reported the first pulsed blue InGaN laser at room temperature and at the end of the same year he announced the first continuous wave (CW) blue electrical injected laser at room temperature.

In spite of these great results, progress in nitrides research has shown that these devices grown on *c*- plane have some fundamental impairments which limited their performance. In particular, the alternating layers of Ga and N atoms of the c- direction cause the structure to be polar, as a result of the different electronegativities of these two atoms. The dipoles of every layer in the unit cell will neutralize each other in the bulk, however sheet charges exist at the surface and at the interfaces as shown in Fig. 4. Although these fixed charges are in general desirable for some electronics devices as they naturally form two-dimensional electron gases (2DEGs), on the other hand they are detrimental for optoelectronics applications as they cause tilting of the energy bands inside the active region: this decreases the overlap of the electron and hole wavefunction and as a consequence it reduces the oscillator strength of the radiative transitions and causes a red-shift of the emission wavelength [23, 24]. Injecting carriers can partially screen these polarization-induced fields and produced a blue-shift of the emission wavelength. These effects are known as quantum-confined Stark effect (QCSE) or quantum-confined Franz-Keldysh effect.

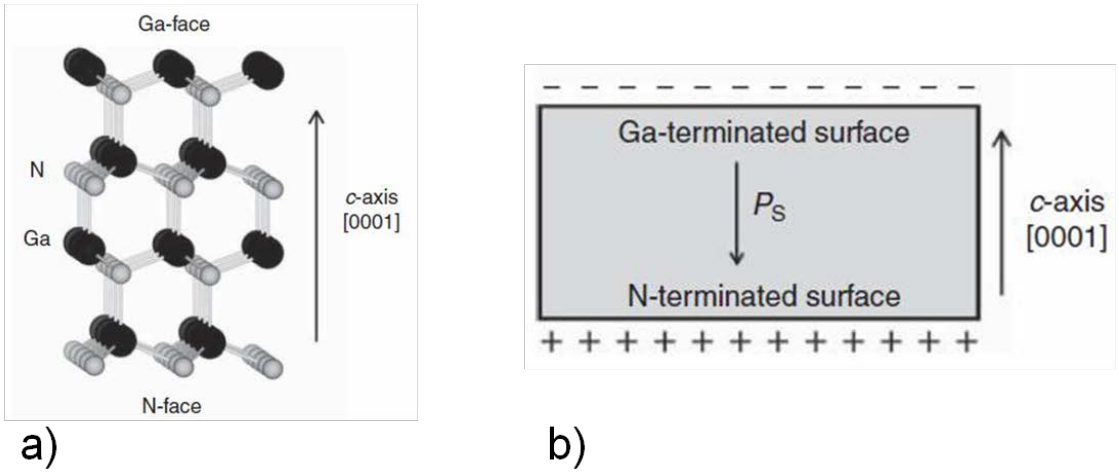

Figure 4 Schematic of GaN unit cell and relative sheet charge at the interface (From [16]).

In order to overcome this problem, the use of non-polar and semipolar planes have been suggested. The non-polar planes are those which cut across the crystal side and include the {11-20} and {10-10} planes, which are also known respectively as *a*- and *m*- planes. Semipolar planes are those planes which have a nonzero *l* Miller index and at least two nonzero *h*, *i* or *k* Miller indices. The main features of these planes is to have absent (non-polar) or reduced (semipolar) polarization field as experimentally demonstrated firstly on a planar m- plane thin film grown on (100)-oriented g-LiAlO2 substrate [25]. The most commonly used semipolar and nonpolar planes are shown in Fig. 5.

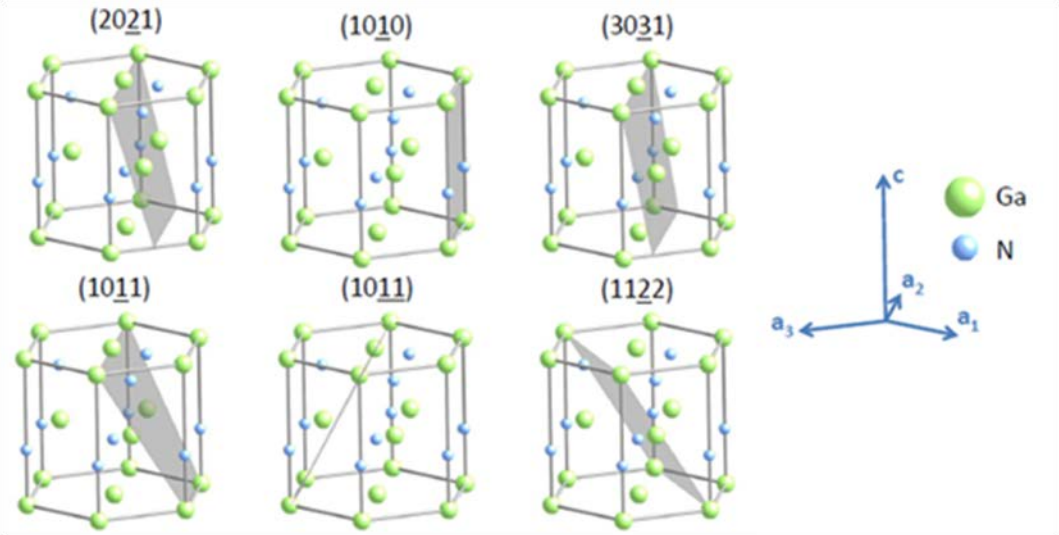

Figure 5 Most commonly used semipolar and non-polar planes

Mainly Rohm, Sharp, Sumitomo and Kaai (and more recently Soraa [26]) at industrial level and at university level particularly UCSB in the US [27], have led the way in research efforts to investigate and fabricate devices on non-polar and semipolar plane as shown in Fig. 6. Mentioning only LDs works at UCSB, the early results have been achieved with devices fabricated on m- plane and emitting in the violet: in 2007 Schmidt demonstrated the first m- plane LD [28], Feezell reported the first AlGaN-cladding-free m- plane LD operating in pulse conditions [29] and Farrell in CW mode [30]. Emission with pulsed lasing at 442 nm, 481 nm and 465 nm were obtained in 2009 on ACF *m*- plane, intentionally misoriented miscut substrates and asymmetric p-GaN/n-AlGaN cladding layers and in the following year CW lasing at 461 nm on ACF *m*- plane [31] In the meantime also semipolar planes have been investigated and pulsed lasing at 516 nm for ACF (20-21), at 445 nm for ACF (30-31) LDs were reported between 2009 and 2010. In 2014, Watt-level performance

under pulsed conditions for devices emitting at 445 were reported on (20-2-1) [32] and CW operation with power ~10 mW using ACF (20-2-1) and current aperture design was achieved as described in this dissertation [33].

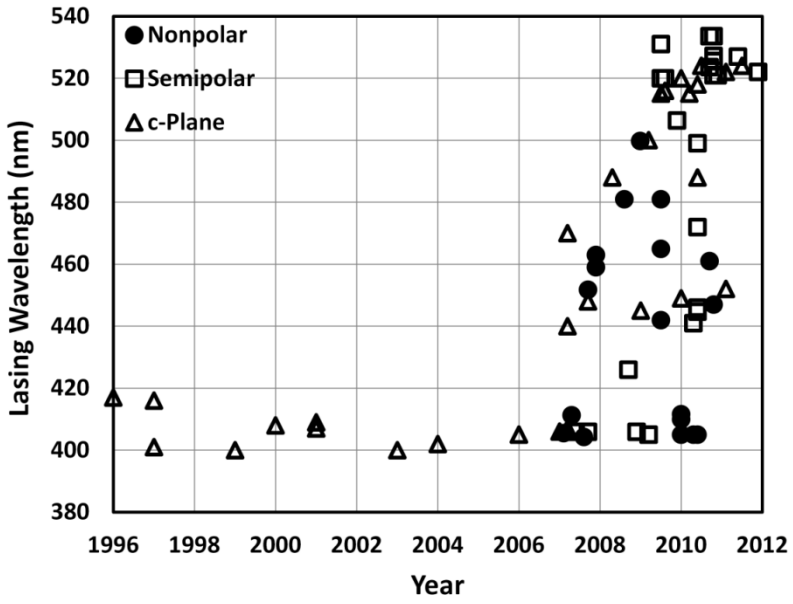

Figure 6 Progress of c-plane, semipolar and non-polar devices (Reprinted with author permission from Ref. [27])

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Chapter 2

Photo-Electro-Chemical (PEC) Etching

2.1 Introduction

Etching is one of the most crucial steps of the fabrication of any micro-nano device. Differently from other III-V semiconductors, GaN and its alloys with InN and AlN have a high bond strength energy (up to 8.92 eV/atom for GaN) which make them chemically very stable and extremely resistant to essentially any conventional chemical etchant, with some mild etch of the N-face in hot KOH as reported in Table 1 [1,2,3].

Although this is an advantage to devices which need to stand harsh conditions, such extreme lack of chemical reactivity makes this material system resistant to traditional wet etching and chemical etching techniques and therefore etching of nitride films has been so far

carried out using mainly chlorine-based dry etching methods, in particular Reactive Ion Etching (RIE), Inductively Coupled Plasma etching (ICP), Electron Cyclotron Resonant Etching (ECR), Chemically Assisted Ion Beam Etching (CAIBE) and Magnetron-reactive Ion Etching (MIE) are the techniques which have mostly been used.

Table 1. Compilation of etching results in acid and base solutions, performed at room temperature (25°C) unless otherwise noted

	GaN	InN	AlN	InAlN	InGaN
Citric acid (75°C)	0	0	0	0	0
Succinic acid (75°C)	0	0	0	0	0
Oxalic acid (75°C)	0	Lifts off	Lifts off	Lifts off	Lifts off
Nitric acid (75°C)	0	Lifts off	0	Lifts off	Lifts off
Phosphoric acid (75°C)	0	0	Oxide removed	Oxide removed	0
Hydrochloric acid (75°C)	0	0	0	0	0
Hydrofluoric acid	0	Lifts off	0	0	Lifts off
Hydriodic acid	0	0	0	0	0
Sulfuric acid (75°C)	0	Lifts off	0	0	0
Hydrogen peroxide	0	0	0	0	0
Potassium iodide	0	0	0	0	0
2% Bromine-methanol	0	0	0	0	0
n-Methyl-2-pyrrolidone	0	0	0	0	0
Sodium hydroxide	0	Lifts off	Lifts off	Lifts off	Lifts off
Potassium hydroxide	0	Lifts off	22,650 Å min^{-1}	0	0
AZ400K Photoresist developer (75°C)	0	Lifts off	~60–10,000 Å min^{-1}	Composition dependent	0
Hydriodic acid/hydrogen peroxide	0	0	0	0	0
Hydrochloric acid/hydrogen peroxide	0	0	0	0	0
Potassium triphosphate (75°C)	0	0	0	0	0
Nitric acid/potassium triphosphate (75°C)	0	Lifts off	0	0	0
Hydrochloric acid/potassium triphosphate (75°C)	0	0	0	0	0
Boric acid (75°C)	0	0	0	0	0
Nitric/boric acid (75°C)	0	Lifts off	0	0	Lifts off
Nitric/boric/hydrogen peroxide	0	Lifts off	0	0	Removes oxide
$HCl/H_2O_2/HNO_3$	0	Lifts off	0	Lifts off	Lifts off
Potassium tetraborate (75°C)	0	Oxide removal	Oxide removal	Oxide removal	Oxide removal
Sodium tetraborate (75°C)	0	0	0	0	0
Sodium tetraborate/hydrogen peroxide	0	0	0	0	0
Potassium triphosphate (75°C)	0	0	0	0	0
Potassium triphosphate/hydrogen peroxide	0	0	0	0	0

Table 1 Etching results for Nitride common wet etchants (Reprinted with permission from Ref. [3])

Although these can provide relatively fast etch rates (up to a few hundred nm/min) and nearly vertical sidewalls, they have several drawbacks.

First, dry etching produces sub-surface damage (most notably to the p-GaN layer and to the device active region). Such damage is in general proportional to the RF power used during the dry etching operation [4], which needs to be relatively high in order to have a reasonable etching rate, and increases both the surface recombination velocity and the

density of nonradiative recombination centers [5]. Surface recombination is modelled using SRH statistics[1]:

$$R_{sr} = \frac{a_s}{V} \cdot \frac{np - n_i^2}{{}^{n}/_{v_h} + {}^{p}/_{v_e}}$$

where n, p, n_i, a_s, V, v_h, v_e are the the electron, hole, intrinsic carrier concentration, surface are, volume, hole and electron surface velocity respectively. The equation indicates that the surface recombination is both dependent on the material system, as hole and electron surface velocity is tipycal of each semiconductor, and on the geometry of the system. Table 2 summarizes the surface velocity for different compound semiconductors.

Compounds Seminconductors	Surface recombination velocity vs (cms/2
InGaAs/GaAs (QW)	≈ 1 – 2 *10^5
GaAs (Bulk)	≈ 4 – 6 *10^5
InP (Bulk)	< 10^4
GaN (Bulk)	≈ 10^4 – 10^5

Table 2 Surface recombination velocity for different III-V compounds

The geometrical dimensions dependency indicates that device having a big form factor, i.e. long and narrow ridge width (wridge ≤2.5µm) edge emitting laser diodes, can therefore be particularly affected from this phenomenon. In particular, simulations from Satter show that

[1]The expression can be approximated as $R_{sr} = \frac{a_S}{V} \cdot v_s \cdot \mathrm{n}$ at high level injection, regime where LDs typically operate

decreasing the surface recombination velocity leads to a decrease in the threshold current density and to an increase in the slope efficiency.

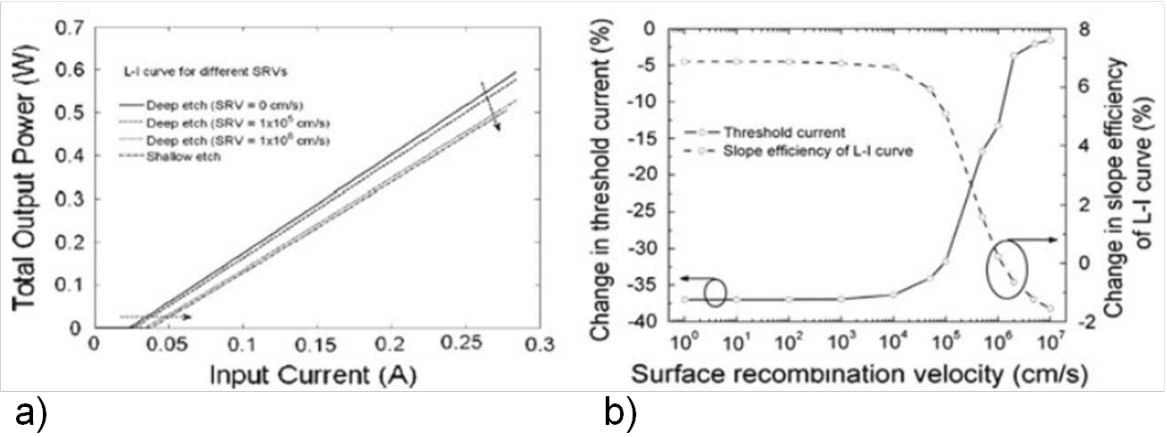

Figure 7 Impact of surface recombination velocity on output power, threshold current density and slope efficiency. (Reprinted with permission from Ref. [6])

The final effects of this damage is the degradation of the electrical properties of the epitaxial structure and reduce the performance, reliability and lifetime of the final device [7-10]. A possible way reduce the surface recombination velocity is to passivate the device etched surface. For example, AlGaAs-based devices are usually passivated by oxidizing the AlGaAs waveguides [11].

Unfortunately no treatment has been found really effective to passivate surface and recover from dry-etching damage Nitrides devices. In fact although a $(NH_4)_2S$ treatment has been proposed to reduce the surface recombination velocity from $\sim 1 \cdot 10^5$ cm/s down to $5.8 \cdot 10^2$ cm/s [12] and short KOH dips have also been suggested to recover the active region from dry etching damage the effectiveness of such passivation technique has proven to be limited and to avoid this issue [13], the ridge of LDs is usually etched before the active region. However, as it will be discussed in more detail in Chapter 3, this design choice is

detrimental in particular to narrow-ridge (<= 2.5 μm) LD as the threshold current of the devices increases as the LD ridge is etched less.

Secondly, dry etching can induce high surface roughness, generally correlated to corrugations of the photoresist profile and the etch rate, between the waveguide core and the cladding [14]. This is undesirable in optoelectronics devices because it decreases the facets reflectivity in the case of LD, making also extremely difficult to extract the internal parameters of the devices, and it causes high optical scattering loss especially in the case of high-index-contrast (HIC) optical devices [15].

Indeed, poor quality etching can reduce device performance through optical scattering loss α_s which is proportional to the product of the square of the root-mean-square (RMS) sidewall surface roughness σ and the core-cladding effective index contrast Δn and inversely proportional to the emission wavelength of the device [16].

Thirdly, precise control of the etch depth is hard to achieve, being in general ~40nm at the best, without resorting to selective RIE and etch stop layers [17].

Lastly, dry etching technique are not lateral dimension selective therefore they do not allow for controllable lateral [18-20] or isotropic etch like the wet etching does [21].

By contrast, wet etching offers the possibility of compositional and crystallographic-selective wet etching and it has been successfully applied to Si and other III-V semiconductors. Many studies have described the wet etching of InGaAsP compounds by mixtures of H_2SO_4:H_2O_2:H_2O, $C_6H_8O_7$:H_2O_2:NH_4OH, HCL: H_2O and other acids/bases to fabricate complex optoelectronic devices such VCSEL, buried aperture oxide laser, constricted mesa laser and also electronic device such as InGaAs FinFETs [22-27].

Photo-Electro-Chemical Etching (PECE) has emerged in the recent years as a powerful wet etching for Nitrides.

2.2 Photo-Electro-Chemical PEC etching

PEC etching is a particular wet etching process which takes advantage of light (photo) along with electrochemical (oxidation-reduction) reactions to etch [28].

Along with the wet etching benefits, PEC etch offers other unique advantages:

- Bandgap selectivity
- Dopant selectivity
- Defect selectivity
- Crystallographic selectivity

The bandgap selectivity is particularly desirable for creating a controllable undercut into the epitaxial structure, which is useful to improve the performance or widen the design space of both optoelectronics devices such as PEC current aperture edge-emitter lasers (CA-LD), which is shown in this work, vertical cavity surface emitting lasers (VCSEL) [29], and current aperture vertical electron transistors (CAVET) [30].

In addition, it has been reported that short KOH dip can help the sample to recover from the dry etching damage as shown in Fig. 8

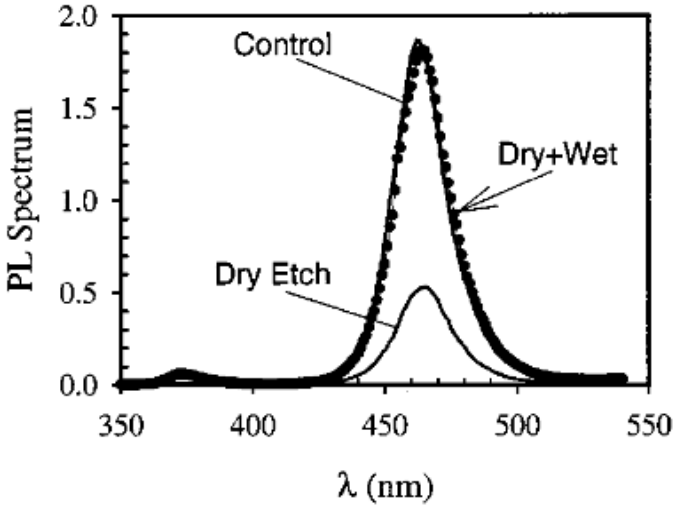

Figure 8 Dry etching damage recovering after 5s KOH:H2O (~0.04 M) wet-etching a GaN structure [From 13]

2.2.1 Basic physics of PEC etching process

The PEC etching process consists of illuminating with a supra-bandgap light source a sample immersed into an electrolyte: this results in the generation of electron/hole pairs which, after they separate because of the internal electric field, make the etching occur. The semiconductor acts as anode, the metal deposited on the *n*- side acts as cathode and the conductive electrolytic medium which closes the circuit. The holes migrate to the surface which therefore become oxidized and finally etched by the electrolyte. In order to improve the photogenerated charges separation bias can be applied to the sample in such a way that it is reversed biased.

The system semiconductor – electrolyte can indeed be treated similarly to a semiconductor – Schottky barrier, although there are some important differences.

In a semiconductor the Fermi level can be expressed as:

$$E_{Fn,p} = E_{Fi} + k_B T ln(\frac{N_{D,A}^{+,-}}{n_i})$$

where $E_{Fn,p}$ is the Fermi level in a n (p) semiconductor, E_{Fi} is the intrinsic Fermi level, k_B is the Boltzman constant, T is the temperature, $N_{D,A}^{+,-}$ is the concentration of ionized donors (acceptors) in a *n* (*p*) semiconductor and n_i is the intrinsic carrier concentration. Similarly in a re-dox electrolyte the electrochemical potential (which can be identified with the Fermi level in a semiconductor) is given by the Nernst equation:

$$E_{redox} = E_{redox}^{0} + \frac{RT}{nF} ln\left(\frac{c_{ox}}{c_{red}}\right)$$

where E_{redox}^{0} is the standard half cell reduction potential, *R* is the universal gas constant, *T* is the temperature, *n* is the number of moles of electrons transferred in the cell reaction, *F* is the Faraday constant (the number of coulombs per mole of electrons: F = 9.6485*10^4 C · mol^{-1}), c_{ox} and c_{red} are the concentrations (or activities) of the oxidized and reduced species. At room temperature both $k_B T$ and $\frac{RT}{F}$ are equal to ~25.6 mV.

The energy band diagram of an isolated n-semiconductor/electrolyte is represented below.

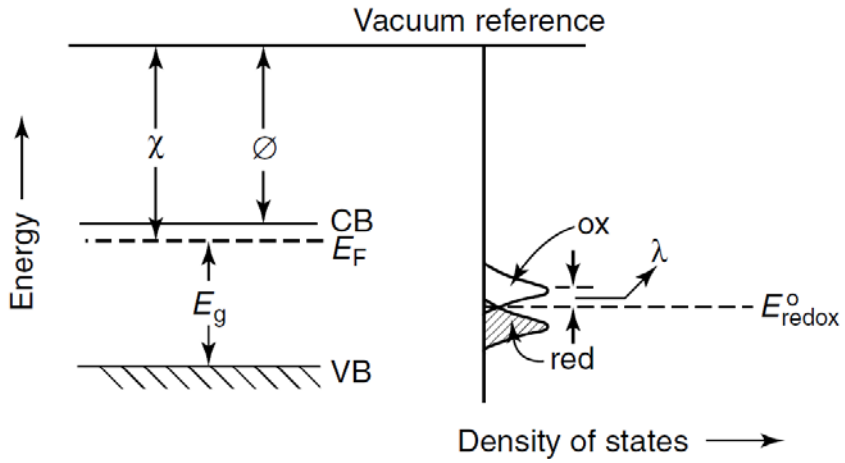

Figure 9 Schematic of the energy band diagram of a semiconductor and an electrolyte

Fig. 9 illustrates the two main differences between the semiconductor and the electrolyte:

- In a semiconductor the energy vacuum level is adopted as reference, in electrochemistry it is the standard hydrogen electrode (SHE or NHE). It is commonly accepted that it lies 4.5 eV below the vacuum level that is $E_{F,redox} = E^0_{redox} - 4.5$ (eV)

- In a semiconductor the minimum of the conduction (top of the valence) band are sharply defined for electrons (holes), and this difference represents the energy bandgap (Γ point). For an electrolyte, the thermal energy of the system is described by a set of harmonic oscillators leading to a Gaussian-like distribution of the energy levels both for the semi-empty and the semi-occupied energy levels (the conduction and the valence bands respectively in the analogy) given by:

$$D_{ox} = exp\left(-\frac{E - E_{F,redox} - \lambda^2}{4k_B T\lambda}\right)$$

and

$$D_{red} = exp\left(-\frac{E - E_{F,redox} + \lambda^2}{4k_B T\lambda}\right)$$

where k, T and $E_{F,redox}$ have been described before, E is energy at which the charge transfer to the electrolyte occurs and λ is the solvent reorientation (or reorganization) energy for the solvent shells of the redox species. The semiconductor band-edge positions relative to some solutions redox levels have been computed by capacitance measurements using the Mott-Schottky relation. For an *n*-type semiconductor, this expresses the semiconductor depletion layer as function of the flat-band potential V_{FB} as:

$$\frac{1}{C_{sc}^2} = \frac{2}{qN_D\varepsilon_0\varepsilon_s}\left[(V - V_{FB}) - \frac{k_B T}{q}\right]$$

Fig. 10 shows the band alignment of several semiconductors in contact with an electrolyte with pH = 1 (GaN for pH = 0).

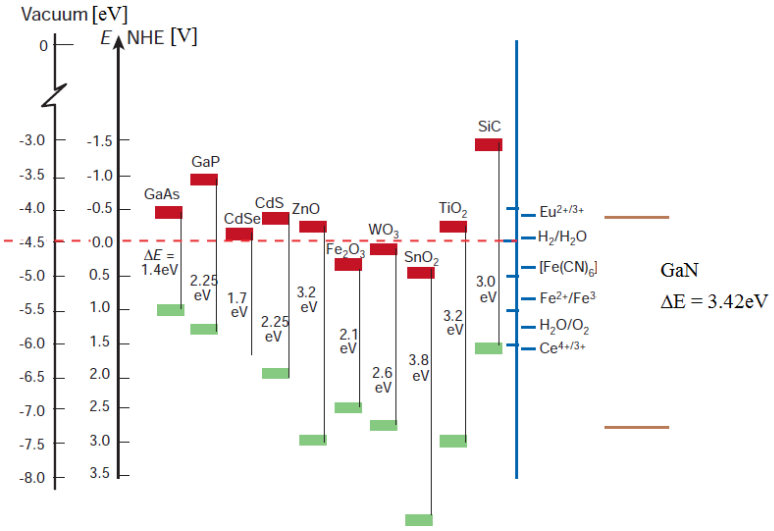

Figure 10 Energy Band diagram of several semiconductor and electrolytes

When the semiconductor and the electrolyte come in contact the different Fermi of the two systems line up as a consequence of the electric charge transfer and the conduction and valence bands bend, as represented in Fig. 11.

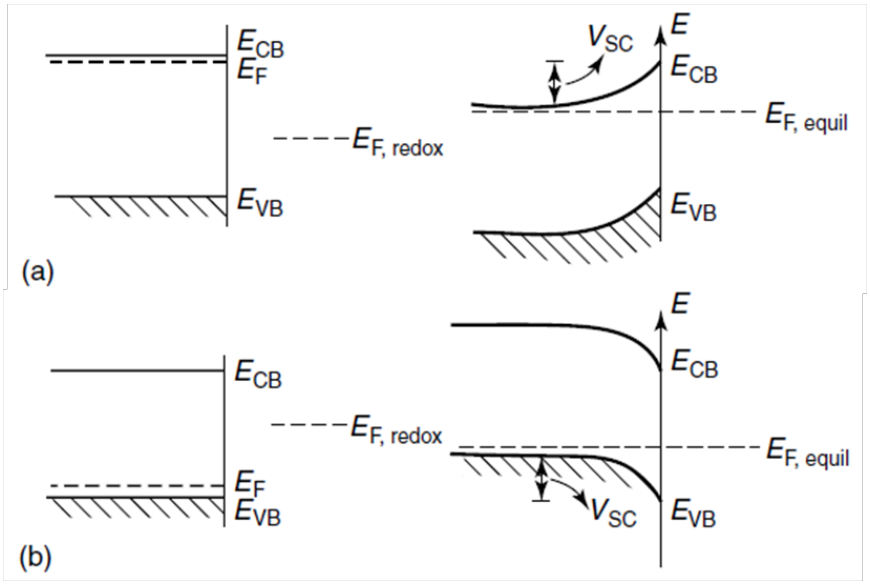

Figure 11 Energy Band diagram of a *n*- and *p*- semiconductor in contact with electrolyte

In all the experiments presented in this work, it can be assumed that the active region which was PEC etched is slightly n-doped. Although the QWs in all the grown structures are nominally un-doped, they are in fact u.i.d. (un-intentionally doped) since unintentionally doping comes from the environment (mainly O) and the carrier gases (mainly C). Therefore, when the sample is illuminated and dipped into an electrolyte solution, whose Fermi level is below that of the sample, the energy bands bends upwards as in the Fig. 12

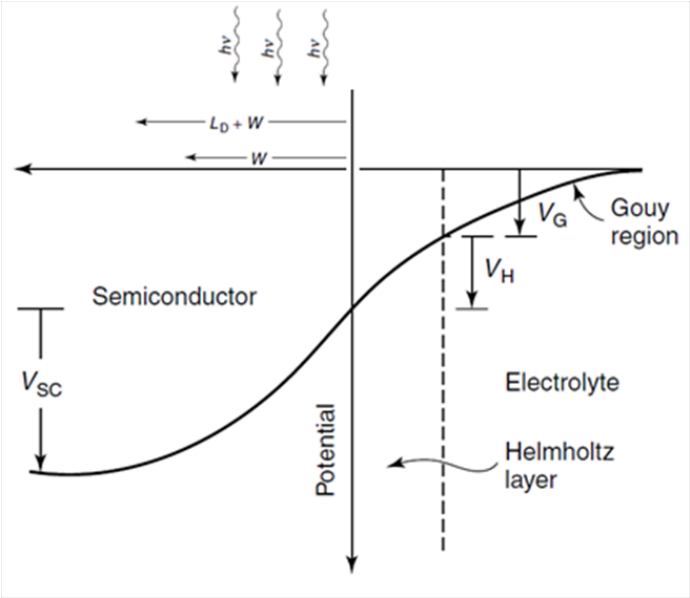

Figure 12 Energy band diagram of n-doped semiconductor in contact with an electrolyte.

where W is the depletion region and LD is the Debye (or diffusion) length. The depletion region width is computed as $W_0 = \sqrt{\frac{2\varepsilon_S\varepsilon_0}{qN_D}}$ and when bias is applied the equation modifies to $W = W_0 \cdot \sqrt{V_{bi} - V}$ where ε_S is the dielectric constant of the semiconductor, ε_0 is permittivity of the vacuum, q is the electron charge, N_D is the donor density, V is the applied bias and V_{bi} is built-in potential. The active region is typically unintentionally *n*-type doped with doping level as high as ~10E16 which leads to an upward bending of the energy bands and to a depletion width in the range ~100nm. By contrast, for concentrated electrolytes that is those with pH >12 – as the one used in this work – or with pH <2, the depletion width – which is correspond to the compact (*Helmholtz*) and diffuse (*Gouy*) layers represented in Fig. 12 – is essentially negligible (typical 0.4 - 0.6 nm), quite similar to the metal-semiconductor case.

The diffusion length is the region beyond which all the photogenerated carriers recombine and for a *n*- type semiconductor it is computed as:

$$L_h = \sqrt{D_h \tau_h} = \sqrt{k_B T \mu_h \tau_h}$$

where D_p is the diffusion coefficient for the hole, μ_p is the hole mobility, τ_p is the hole life-time.

The photogeneration process creates an equal number of electrons and holes:

$$\frac{\partial n}{\partial t}|light = \frac{\partial p}{\partial t}|light = G_{light}(x, \lambda)$$

However, what really matters is the change with respect to the equilibrium condition in the carrier concentrations, that is:

$$\Delta n \equiv n - n_0$$

and

$$\Delta p \equiv p - p_0$$

where

- *n*, *p* are the electrons (holes) concentrations under arbitrary conditions
- n_0 and p_0 are the electrons (holes) concentrations at equilibrium
- Δn and Δp are the excess electrons (holes) concentrations from equilibrium. If this number is positive (negative), a generation (recombination) process has occurred. When the perturbation is small (i.e. low light intensity) only the minority carriers concentration changes significantly (low level injection case).

Such condition implies:

$\Delta p \ll n_0$ and $n \cong n_0$ in an *n*- type semiconductor

$\Delta n \ll p_0$ and $p \cong p$ in a *p*- type semiconductor

Following the procedure suggested by Gartner [31] , the total current density J_{Tot} can be computed as

$$J_{Tot} = J_{DL} + J_{Diff} - J_{Rec}$$

where $J_{DL}$is the drift current density due to the carriers generated inside the depletion region, J_{Diff} is the diffusion current density of minority carriers generated outside the depletion layer in the bulk of the semiconductor and diffusing into the junction, J_{Rec} is the recombination current, mainly due to traps, defect, recombination center in general.

The generation rate for a monochromatic radiation with intensity I_0 shining on a material with absorption coefficient α can be expressed as

$$G(x) = I_0 \cdot \alpha e^{-\alpha x}$$

Then J_{DL} can be computed as

$$J_{DL} = q \cdot \int_0^W g(x)dx = qI_0 \cdot (e^{-\alpha W} - 1)$$

while in the quasi-neutral region J_{Diff} is governed by the following equation:

$$D_p \frac{d^2p}{dx^2} - \frac{p - p_0}{\tau_p} + G(x) = 0$$

This equation using the boundary conditions:

$$p = p_0 \quad \text{for} \quad p = \infty$$

and

$$p = 0 \quad \text{for} \quad p = W$$

has the following solution:

$$p = p_0 - (p_0 + Ae^{-\alpha W}) \cdot e^{\frac{W-x}{L_p}} + Ae^{-\alpha x}$$

with $A = \frac{I_0}{D_p} \cdot \frac{\alpha^2 L_p^2}{\alpha \cdot (1-\alpha^2 L_p^2)}$

From semiconductor theory the diffusion current density is $J_{Diff} = qD_p \frac{dp}{dx}$ that is

$$J_{Diff} = qD_p \cdot \left[\frac{p_0}{L_p} \cdot e^{\frac{W-x}{L_p}} - \frac{A}{L_p} e^{-\alpha W} \cdot e^{\frac{W-x}{L_p}} - \alpha A e^{-\alpha x}\right]$$

therefore at the edge of the depletion region $x = W$ we get:

$$J_{Diff} = qD_p \cdot \left[\frac{p_0}{L_p} - e^{-\alpha W} \cdot \left(\frac{A}{L_p} - \alpha A\right)\right]$$

$$= qD_p \cdot \left[\frac{p_0}{L_p} - e^{-\alpha W} \cdot \left(\frac{1}{D_p} \cdot \frac{\alpha^2 L_p^2}{\alpha \cdot (1-\alpha^2 L_p^2)} \cdot \frac{1-\alpha L_p}{L_p}\right)\right]$$

and finally

$$J_{Diff} = -qI_o \frac{\alpha L_p}{(1+\alpha L_p)} \cdot e^{-\alpha W} - qp_0 \frac{D_p}{L_p}$$

In the depletion region the recombination current J_{Rec} can be computed using the Shockley-Sah-Noyce method:

$$J_{Rec} = \mathrm{q} \cdot R(x) dx$$

where $R(x)$ is the recombination rate as described by Sah-Noyce-Shockley equation:

$$R(x) = \sigma \cdot v_{th} \cdot N_t \cdot \frac{np}{n+p}$$

where σ is the capture cross section for the electrons and the holes (assuming $\sigma = \sigma_n = \sigma_p$ is generally assumed), v_{th} is the carrier thermal velocity, N_t is the density of traps with energy level at or near the intrinsic Fermi level E_{Fi}. J_{Rec} has it maximum value when $n = p$ that is when the intrinsic Fermi level is halfway between the quasi-Fermi levels for the electrons (E_{Fn}) and the holes (E_{Fp}). In that case, R_{max} is equal to:

$$R_{max} = \frac{1}{2}\sigma \cdot v_{th} \cdot N_t \cdot n_i \cdot e^{qV/2k_BT}$$

since

$$np = n_i^2 \cdot e^{qV/k_BT}$$

Finally the space-charge recombination density current becomes:

$$J_{Rec} = \frac{1}{2}\sigma \cdot v_{th} \cdot N_t \cdot n_i \cdot e^{qV/2k_BT} \cdot W_0 \cdot \sqrt{V_{bi} - V}$$

As stated earlier, the total density current is the sum of all these contributions:

$$J_{Tot} = qI_0 \cdot (e^{-\alpha W} - 1) +$$
$$-qI_o \frac{\alpha L_p}{(1 + \alpha L_p)} \cdot e^{-\alpha W} +$$
$$-qp_0 \frac{D_p}{L_p} \frac{1}{2} \sigma \cdot v_{th} \cdot N_t \cdot n_i \cdot e^{qV/2k_BT} \cdot W_0 \cdot \sqrt{V_{bi} - V}$$

2.3 PEC etch of Nitrides

Although the idea of anodic-etching GaN dates back to the early ’60s [32], GaN photo-electrochemical etching was successfully achieved only in the mid-90s’ [33,35].

As for the case of PEC etching other semiconductors, PEC etching of Nitrides consists in a sequence of oxidation and reduction processes which are started by creation of electron-hole pairs into a particular layer (which in this work is always an InGaN/GaN active region) by a suitable light source. In particular for GaN the following reactions have been proposed [36]:

$$2\,GaN + 6\,h^{+} + 6\,OH^{-} \rightarrow\ Ga_2O_3 + 3\,H_2O + N_2\uparrow$$

$$Ga_2O_3 + 6\,OH^{-} \rightarrow Ga_2O_3^{3-} + 3\,H_2O$$

Several studies have reported the etching of *n*- type GaN producing whiskers and surface with different degrees of roughness depending essentially on the quality of template, light power intensity, bias applied and solution stirring. Several electrolytes at different concentration have also been tested ranging from H_2SO_4:H_2O_2 to KOH, HF:HNO_3 and HF:C_2H_5OH and KOH, with this last now established as the most commonly used electrolyte [37]. In general, a low concentrated and a slowly stirred solution favor a smoother etched surface. A p-GaN/InGaN/n-GaN p-i-n structure has been used to etch p-type GaN [38], which has been notoriously more difficult to PEC etch because of the unfavorable band-bending at the p-semiconductor/electrolyte interface as described in the previous section.

Along with the energy band bending at the interface semiconductor-electrolyte, the internal band bending of the structure is also important. Fig. 13 shows Silence [39] simulations of simple *n-i-n* and *p-i-n* structures which illustrate how the holes are more confined in an *n-i-n* structure while in the case of a *p-i-n* structure the electric field tends to push them outside the quantum well.

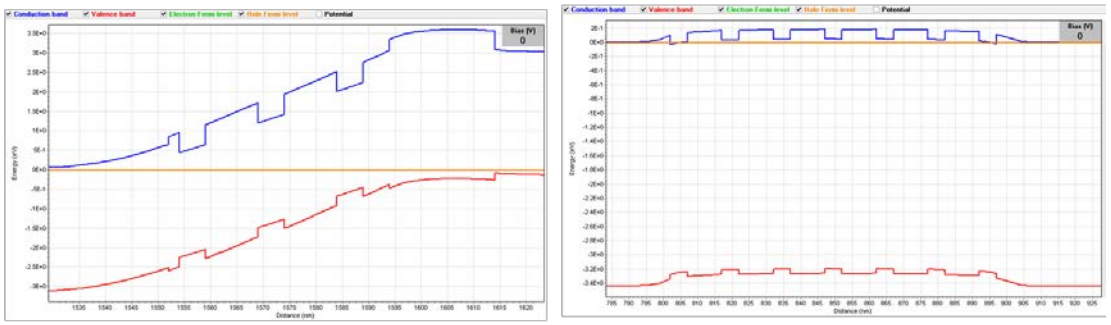

Figure 13 SilenSE simulations of p-i-n (a) and n-i-n MQW structure (b)

By this mean, complex electronic and optoelectronics devices like CAVET transistors and microdisk lasers, porous GaN structures, photonic crystals embedded in GaN LEDs and more recently VCSEL fabricated in *m*- plane have been obtained.

Sacrificial GaN-based layers wet etching have proven to be even more challenging. No good control of the lateral profile and at the same time of the selectivity has been reported for any GaN-based materials wet etching. LEDs sidewalls roughening, etching of the active region and at the same time the *n*- side layer along the *10-10* crystal plane and of the *p*- side at an angle of 27° with respect to the *10-1-1* plane have been reported, while sacrificial layers have been employed to remove the substrate. In general, in all these studies a relatively high bias (up to 20V) has been applied, and the etching is usually achieved in two different times, with the actual etching following the oxidation step (1 μm/h).

Furthermore no control of the etch profile has been provided. Other groups have focused their attention on AlInN/GaN structure, where the AlInN layer has been selectively oxidized and etched from GaN with different oxidation/etching rates and microbridges, planar microcavities and microdisk lasers have been reported [40-42]. Metal mask have been used only as contact to bias the sample and their effect have only been studied to understand the enhancement of etching rate near their border and the trenching effects they had caused. This last phenomenon has been explained in terms of electron capture by the metal which therefore enhance the probability of the holes to oxidize the semiconductor and therefore its subsequent etch. In the next section it will be discussed how masking certain areas selectively can actually led to a good control of regions which are to be etched [43,44].

2.4 Control of the PEC etched active region width

One of most important issues in fabricating nitride CA-LD is to achieve a good control of the extension of undercut of the active region obtained by PEC etching. Halting the etching process at some desired point of the epitaxial structure is in fact critical both to avoid the complete undercut of the active layer and lift-off the *p*- epilayers (similarly this method is in fact exploited for substrate removal) and to compute the main parameters of the LD during the testing (i.e. the threshold current density), as the active region area will be different from the *p*- epilayers area. Although previous reports have shown the importance of protecting the *p*- epilayers during the PEC etch as the p-GaN surface if oxidized by the photogenerated holes overflowing from the quantum wells would be etched if exposed to the

electrolyte solution, essentially no studies have been reported on how to achieve a good control of the PEC etched undercut.

To this goal, several samples by MOCVD on free standing (FS) *m*- plane GaN template provided by Mitsubishi Chemical Corporation (MCC) were grown according to the following structure: a low temperature nucleation layer, 200nm-800nm *n*- GaN, 50nm *n*- InGaN waveguide (~6% In), a series of InGaN/GaN MQWs, 20nm AlGaN EBL, 50nm *p*- InGaN (~6% In), a *p*- GaN with a small *p*++-GaN layer on top. *N*- and *p*- type doping levels are estimated to be in the order of 10^{19} and mid-10^{17} respectively, the In composition of the MQW was ~15 – 18% based on PL measurements. Stripes of different width and length were patterned by standard stepper lithography. These stripes have been oriented either along the (0001) direction, being this the orientation typically used to fabricate optoelectronics devices (the material gain is maximized). A thick SiN_x/SiO_y (~1.5um) deposited by Advanced PECVD followed the deposition of a thick metal stack Pd/Au (200/5000A) deposited by ebeam evaporation. The metal opaque mask on top was meant to block the light and therefore the photogeneration of the electron/hole pairs needed for the PEC-etch process to start. The insulators-based hard mask has been used instead of photoresist as this would dissolve during the PEC etch as the developers are indeed KOH-based. The main purpose of the multilayer oxides is to reduce the intrinsic tensile (compressive) strain that the SiN_x (SiO_y) have, respectively. This strain can in fact be quite high and cause severe bending of the structures as shown in Chapter 3. Mesa structures by Cl2-based RIE etching the stripes down through the *p*- GaN. The resulting structure was covered again with SiN_x (~200nm) to protect the *p*- epilayers from the electrolyte during the PEC etch. On the backside of the samples we deposited 100/5000 Å Ti/Au layer for the *n*-

contact. Finally the samples were then deeply etched again using the previously SiN_x mask (self-aligned process) in order to expose the MQWs and part of the *n*- GaN layer.

Before proceeding with the actual PEC-etching step, the samples were immersed into a HCL solution under dark illumination for a few minutes to remove the native oxide.

A schematic of the flow process and the final structure of a sample before the PEC etch step is depicted in Fig. 14.

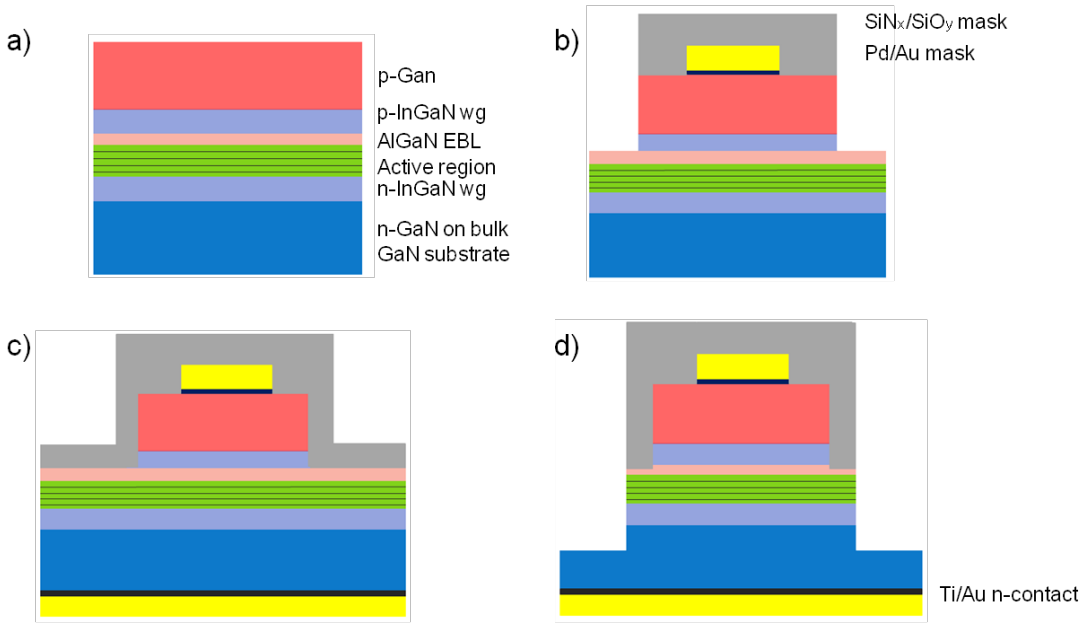

Figure 14 Schematic of the process flow. (a) LD epitaxial structure (b) structure after metal and dielectric multilayer deposition, dielectric etch, and p-GaN etch (c) structure after depositing the (~100 nm) protective dielectric and depositing backside PEC etch cathode (d) structure after removing the thin protective dielectric, dry etching to the n-GaN and PEC etching the active region.

The PEC etching was performed by dipping the samples into a 1 M KOH solution at room temperature. Although an external bias was applied only in the very first experiments, all the results presented in this thesis have been obtained with no bias applied. As light source to generate the excitons into the active region both a fluorescence microscope (Olympus Eclipse LV150, emission range: 380-420nm, light output power: 13.6 mW/cm^2 as measured

by a calibrated photodetector), a violet laser diode (λ = 405nm) and a broadband white lamp (Oriel, 68806 Basic Arc Lamp), with a GaN filter were used as it is illustrated. A schematic of the setup most commonly used in these experiments and photos of the final setup are presented in Fig. 15.

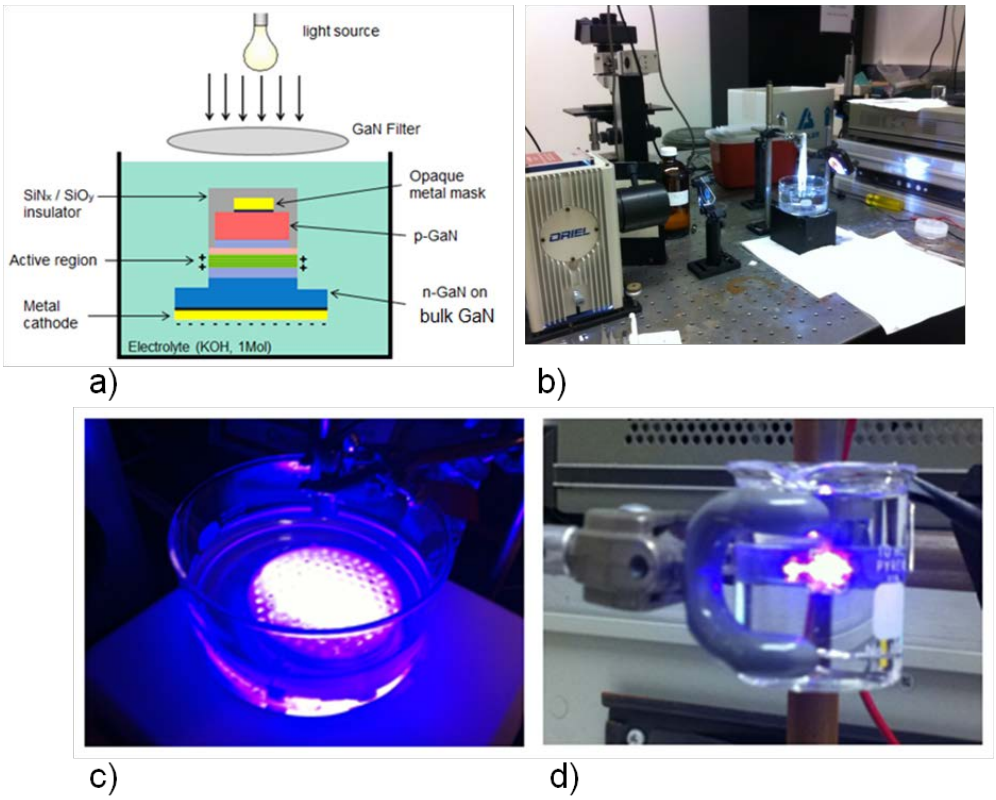

Figure 15 a) schematic of the PEC etching system, illumination source provided by b) a broadband lamp, c) a 405 nm LD, d) PEC etching with bias applied

After etching, the samples were rinsed in DI water, N2-blow dried and characterized by optical microscope using a Nomarski filter for differential interference contrast (DIC) imaging (Olympus LG-PS2). In order to evaluate the role of the metal in halting the photo-induced etching, the metal stripes and the insulators masks were removed by aqua regia and

HF respectively. The fluorescence region area corresponded indeed to the area covered by the opaque metal mask during the PEC etching, as observed in Fig. 16.

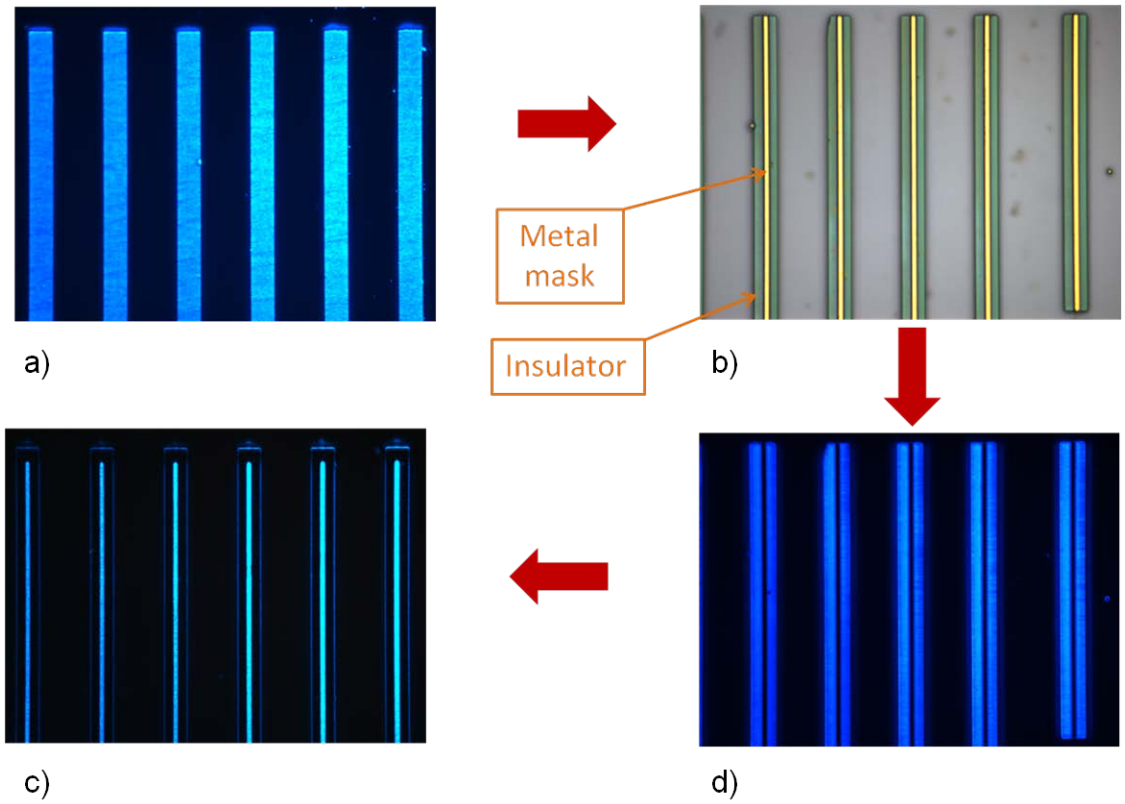

Figure 16 (a) Fluorescent image of LD stripes prior to PEC etching, (b) LD stripes with metal stripe mask (yellow) and protective SiNx/SiOy/SiNx (green) on top of p-GaN, (c) fluorescence emission visible from the unmasked "wing" regions of the LD stripes, (d) fluorescence emission after metal removal from the remaining active region after the PEC-etching. This corresponds to the area protected by the metal stripe during the PEC-etching.

Finally, the stripes were cleaved or FIB-ed and analyzed with scanning electron microscopy (FEI Sirion and JEOL 7600F). SEM images have revealed that the etching had indeed occurred at the MQWs and then it stopped close to the edge of region where the light absorption was blocked by the opaque mask.

Figure 17 (a) shows SEM images of two adjacent waveguide structures with different ridge widths. The etching occurred only within the MQW layers and stopped close to the edge of

the region where the light absorption was blocked by the opaque metal mask, which was 5 μm wide for both the cases (Fig. 17 (b) and (c)).

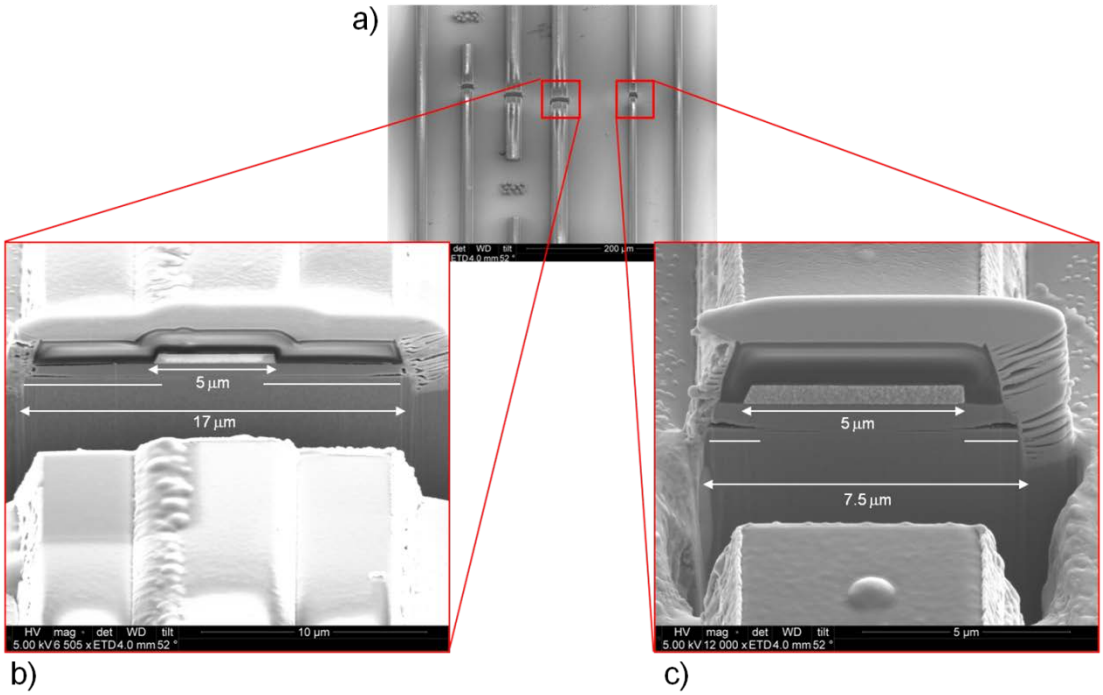

Figure 17 SEM images of a) A top view of two adjacent (20-2-1) LD bars after PEC-etching, b) and c) cross section of the same PEC-etched region LDs showing that the undercut stops close to the edge of the opaque metal mask.

A careful analysis of the SEM images has actually revealed that in several stripes the etching did not stop exactly at the edge of the dark region produced by the opaque metal mask and in fact regions which were not directly illuminated during the PEC etch also show signs of etching. Some of the very narrow stripes in this initial setup etched completely through when larger stripes had a very large lateral undercut, which suggests a relatively low light-exposed-area : masked-area etch selectivity, estimated to be max ~ 3.5 : 1.

The limitations of PEC etch resolution have previously been attributed to the diffusion of holes into the dark region: the un-illuminated semiconductor region which is

within the hole diffusion length $L_h = \sqrt{D_h \tau_h}$ can still be oxidized and therefore etched [45]. Following the equations described in Section 2.2.1, the steady-state carriers profile corresponding to the geometry of the system (dark and transparent areas) at the very beginning of the etching is shown in Fig. 18.

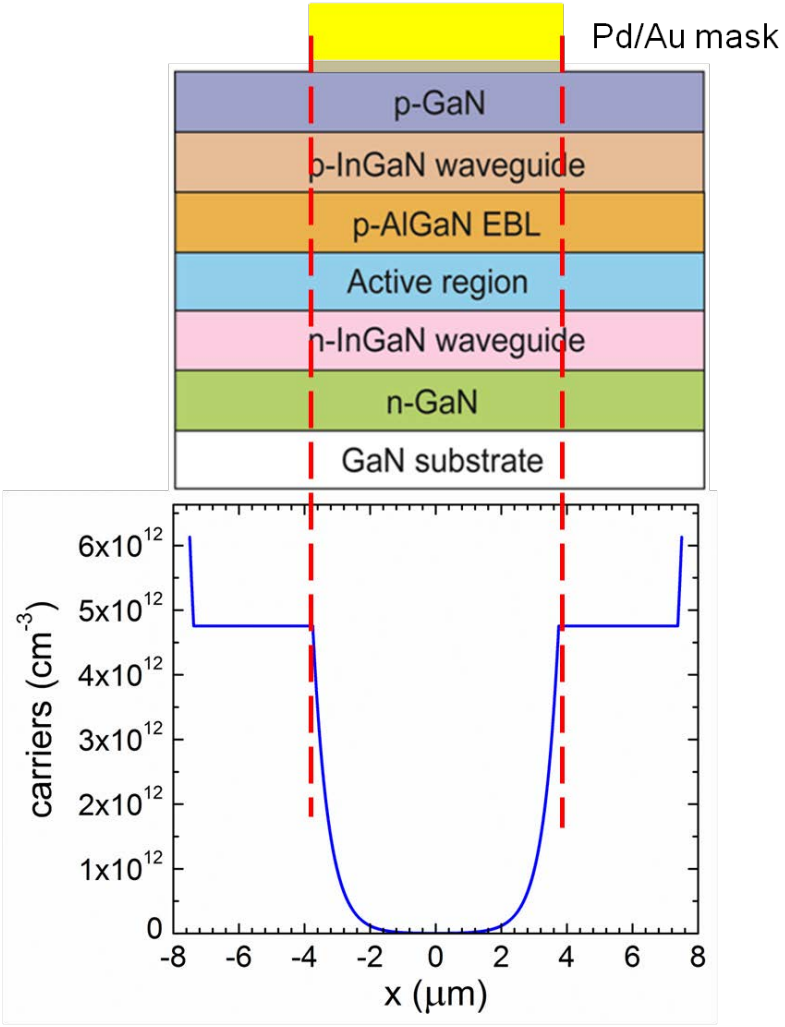

Figure 18 Carrier profile distribution at steady state and t=0$^+$ of the PEC etching

However, this argument alone does not explain the deep undercut below the metal mask that were observed (in some cases on the order of μm), even assuming the fastest etch rate we measured for some sets of samples.

Other explanations have been proposed: limited reaction velocities between the electrolyte and the photo-oxidized materials, variation in the photo-potential produced by different ratios of dark vs. illuminated area, light waveguiding effects, temperature dependency of the etching efficiency, light scattering from the edge of the opaque mask and from the inside of the rough PEC-etched structure [46-54]. AFM measurements taken after complete undercut etching of an *m*-plane InGaN/GaN MQW etched overnight in a 0.1 M and 1 M KOH solution indicate that the in plane roughness of PEC etch structure is very smooth as shown in Fig. 19. The sample etched in 0.1 M KOH shows a roughness on the order of the epitaxial roughness (0.24 nm RMS). Etching in 1 M KOH resulted in an increase in the chemical component of the etching, yielding a higher RMS roughness (0.92 nm RMS) due to the formation of pits.

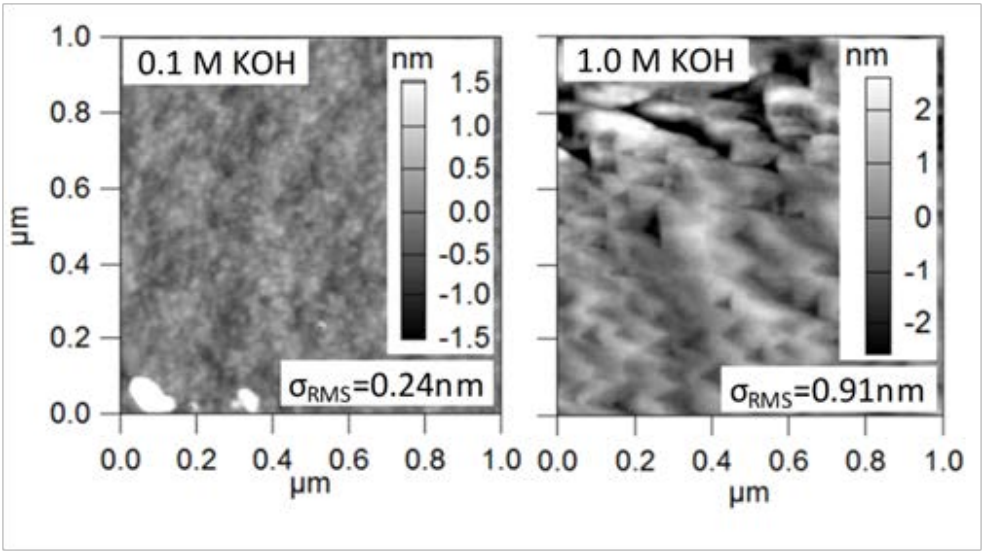

Figure 19 AFM images of completely undercut *m*-plane InGaN MQW layers, showing the exposed GaN surface. The samples were PEC etched in (a) 0.1 M KOH and (b) 1 M KOH overnight, with 405 nm illumination. The 0.1 M etch has an RMS roughness on the order of the epitaxial roughness, while the 1 M etch shows signs of a stronger chemical component to the etch, resulting in the formation of pits and increased roughness.

In contrast, the unpolished backside of the substrate is much rougher and the light which it scatters can play a more important role in limiting the resolution [55].

Using LightTools® [56], a commercial ray tracing software, simulations were performed[1] in an ambient refractive index of n=1.33 to simulate the aqueous environment of the PEC etch and to assess the effect of internal light scattering and reflection on the PEC undercut resolution. Although the metal stripes are meant to block 100% of the incident light to the sample, some of the light can pass through the non-metalized top surface, bounce on the backside of the substrate and illuminate the MQW region which was intended to be dark as shown in Fig. 20 (a). Two models were designed to show the effect of different amounts of metal masking (Fig. 20 (b) and (c)).

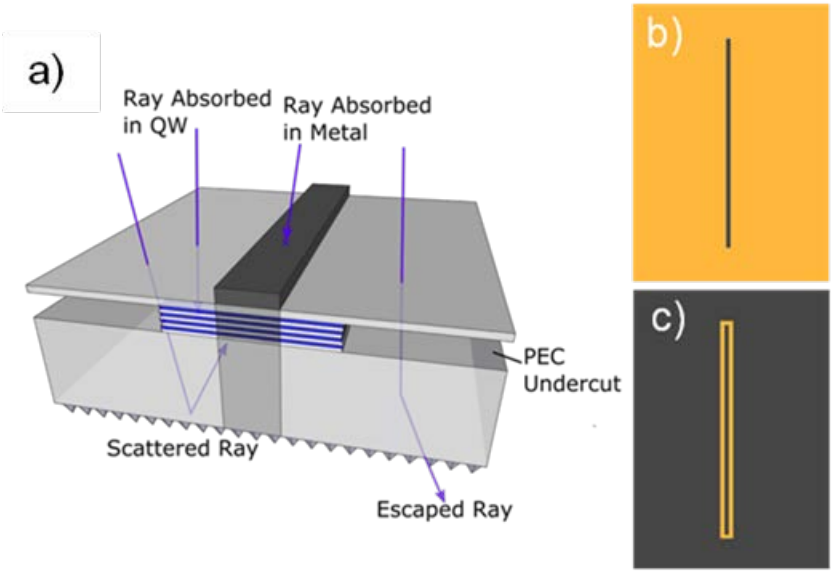

Figure 20 (a) Schematic (not to scale) illustrating the lateral PEC undercut concept and the effects of light scattering and absorption discussed in the ray tracing model. (b) show an opaque metal stripe (grey) mask only, (c) extra metal masking over the entire sample surface (orange).

[1]The LightTools simulations presented in this work were done by L. Kuritzky, Prof. Speck group, UCSB.

The first model included only the opaque metal stripe mask used to define the 7.5 μm x 1500 μm laser stripe active area (Fig. 5 (b)), placed at the center of a 2000 × 2000 × 300 μm^3 GaN wafer (n = 2.5, $\alpha = 6\ cm^{-1}$). The absorption coefficient accounts for a weighted average of the bulk GaN and the QW absorption. The wafer backside was given surface roughening of closely packed regular hexagonal pyramids, 4.3 μm tall and 5.3 μm wide at the base (diameter of the circumscribed circle). The incident rays on chip's top surface, were given an angular range of 0-20˚ to simulate the rough light source collimation used in the experimental setup. Rays that struck the metal mask were immediately terminated. A simulated detector was placed on the bottom surface of the metal stripe to count the rays that scattered from the sample backside and returned to hit the underside of the metal stripe (Fig. 5 (a)).

The second model was the same as the first, but with extra metal masking which covered the entire wafer surface, except for a 3.5 μm gap around all edges of the laser ridge. In the case with only the metal stripe mask ((Fig. 5 (b)), the backscattered light from the roughened substrate corresponded to a power density of ~ 26 mW/cm^2 in the MQW region that was meant to be dark. This is ~40.5% of the power density from the unblocked 405 nm LD and indicates that a significant amount of backscattered light may be contributing to overetching of the MQW region. The second simulation showed that with additional metal masking beyond that needed to define the laser stripe active region (Fig. 5 (c)), the backscattered light power density was reduced to ~1.6 mW/cm^2, which is only 2.5% of the incident power density from the unblocked LD.

These results suggest the importance of reducing the light scattering and reflection to improve etch resolution. We tested this concept experimentally by using additional opaque

metal masking in the field (similar to Fig. (c)) to reduce the scattered and reflected light in the structure. We PEC etched stripes of different widths (range: 4.5 - 9 μm) and lengths (range: 150 - 1800 μm). The total lateral undercut, d, is $d = d_1 + \beta \cdot t_2$ where $t_2 = T_{etching} - t_1$ and it can be expressed as

$$d = d_1 \cdot \left(1 - \frac{\beta}{\alpha}\right) + \beta \cdot T_{etching}$$

where d_1, (d_2), t_1 (t_2) and α and β are the undercut, etch time and etch rate of the transparent (masked) region, respectively, such that $d_1 = a \cdot t_1$, $d_2 = \beta \cdot t_2$ and $T_{etching}$ is the total etching time. Fig. 21 shows the plot of total lateral undercut, d, vs. the undercut in the transparent region, d_1. The slope indicates an etch selectivity of the light-exposed-area : masked-area as high as ~ 13 : 1.

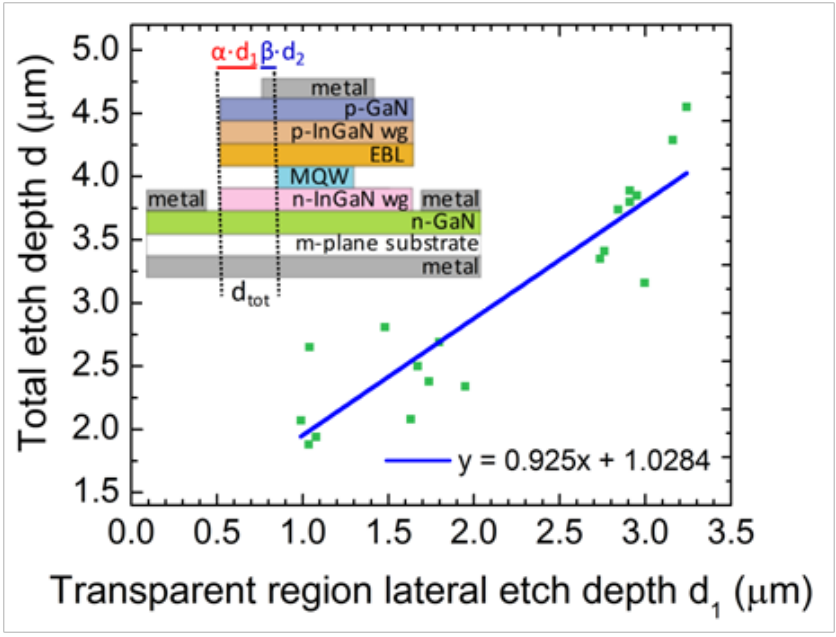

Figure 21 Plot of the total lateral undercut d vs. the undercut in the transparent region d_1. Inset: Schematic of the system.

Eventually the insertion of an absorbing layer (for example an InGaN layer or an InGaN/InGaN superlattice) between the active region and the backside contact may also help improving the PECE resolution along with the structural and morphological properties of the entire structure.

2.5 Ga vs N face PEC etch and nanopillars unetched

Experiments were also performed to evalaute the different etch of the Ga (*c*+) face vs the N (*c*-) face. The N-face is known to be more chemical reactive than the Ga-face and on the c-plane the N-face etches with typical crystallographic pyramidal-shape profile while the Ga face is essentially not etched at all. On other hand, on *m*- plane the intrinsic polarization field pushes the hole towards the Ga face which as result etches even faster than the N-face.

In order to study the different etching rate of the *c*+ (Ga) and *c*- (N) face, stripes were oriented along the (11-20) *a*- direction since this is a natural cleaving plane for *m*-plane GaN. The different etching rate of the Ga and N face were measured for different set of samples and Ga-face has been estimated to etch 2.5x – 4x faster then the N-face.

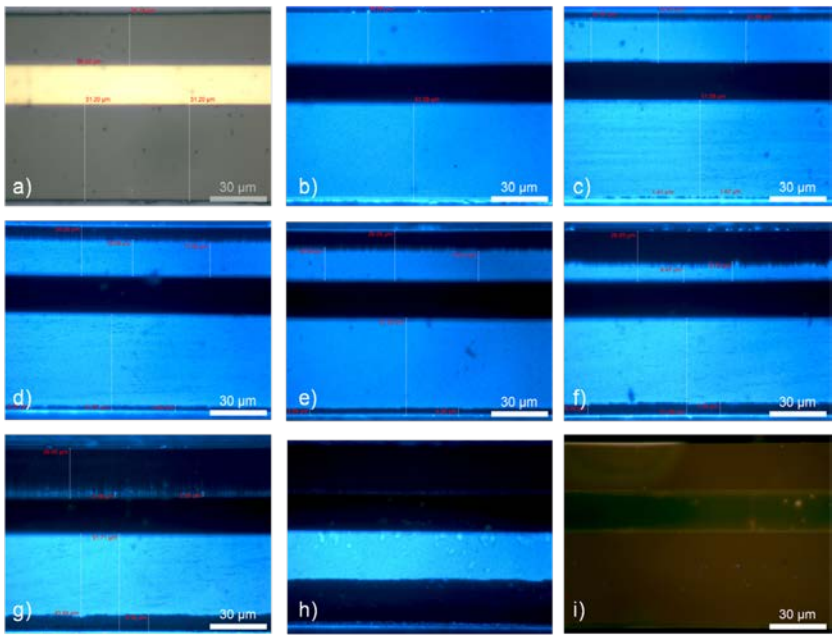

Figure 22 Stripe oriented along the direction and showing the different PEC etching rate of the Ga and N face.

Various etching rate have been recorded for different samples, although the epitaxial structure was similar, with etching rate ranging from few tens nm/min up to ~1.2um/min. Such big differences in etching rate might be attributed to small fluctuations in the quality of the epitaxial structure. Indeed PEC-etching is a technique very sensible to the material quality and uniformity. Defects act as effective recombination centers favoring the excitons recombination which in turn impede the etching. The possibility of stress relaxation via misfit dislocations exists if a critical thickness is exceeded for strained layer growth on semipolar or nonpolar planes. Figure 23 shows a fluorescence microscope image for a laser structure similar to the one studied here but grown and fabricated on an *m*- plane $(1\bar{1}00)$ GaN substrate. The laser stripes are oriented along the in-plane a $[11\bar{2}0]$ direction, and the PEC etch occurred on the c (0001) and c- (000-1) faces of the crystal. For this sample, the thickness (~100 nm) of the $In_{0.06}Ga_{0.94}N$ SCH layer under the MQW activation region

exceeded the critical thickness and MDs consistent with glide on an inclined m-plane formed with line directions along [0001]. These defects are visible as dark (non-radiative) lines in the fluorescence image in Fig. 8. The termination of these MDs at the (0001) and (000-1) sidewalls leads to uneven PEC etching on these faces as the dangling bonds associated with the MDs provide sites for non-radiative carrier recombination and thus no etching can occur. This idea is further supported by the symmetry of roughness seen about the a-axis in Fig. 23 (a), since the MDs terminate at both c-faces, so both faces will see a locally reduced etching rate in the presence of a dislocation. This may also be responsible for the fact that few stripes were not etched at all although they were close located to other stripes that PEC etched as shown on Fig. 23 (b).

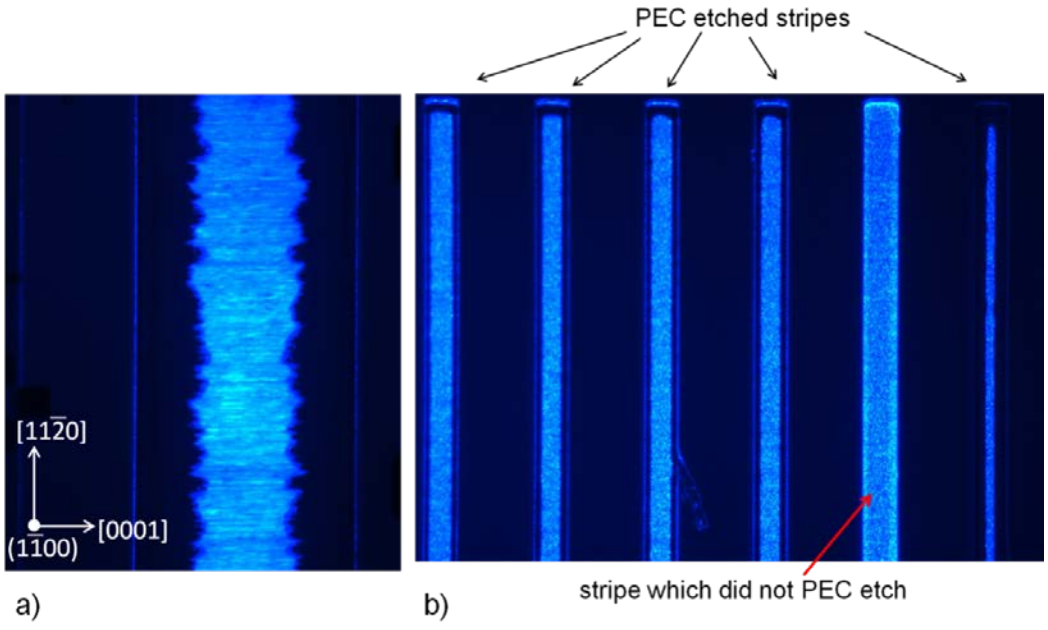

Figure 23 a) fluorescence image of a PEC etched LD grown on m- plane and oriented along the 11-20 direction, b) fluorescence image of different LDs showing that one bar does not show any sign of PEC etch.

SEM images have also revealed the presence of nano-regions (~ 100nm) where PEC etching did not occur as shown in Fig. 24.

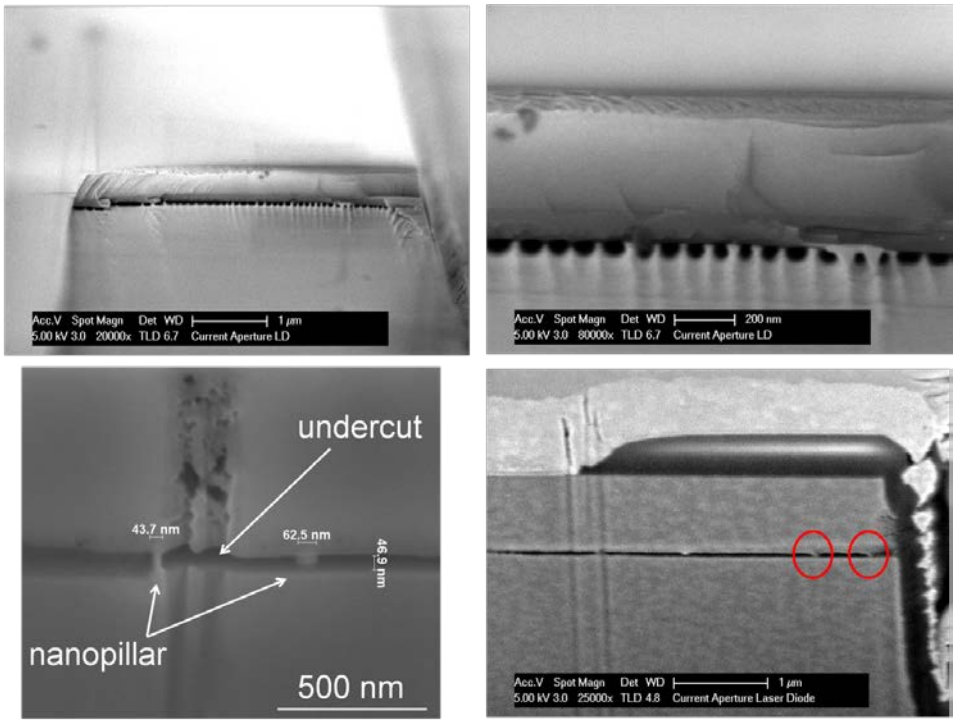

Figure 24 SEM images of nanopillars in aperture region

Finally, a tapered shape profile at the end of all the etched structure has been observed, similarly to what has been reported in the PEC etch of other material system where it has been attributed to the local enhancement of the electric field at curved interface produced by holes local accumulation in the space charge region [57,58].

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Chapter 3

Nitride Current Aperture Laser diode design and fabrication process

3.1 Introduction

Since its invention, engineers have struggled to improve the efficiency of laser diodes by complex engineering both its epitaxial layers and, more generally, the materials quality, and also by improving the fabrication process.

Edge emitting LDs have been fabricated in several configurations as summarized in Figure 25. The planar configuration (Fig. 25 (a) is very easy and fast to fabricate but it offers a very weak the gain guiding, a low index step and high lateral current leakage (although this is

reduced with ion implantation, Fig. 25 (b)) which results in devices with high threshold current density and in general having poor performance.

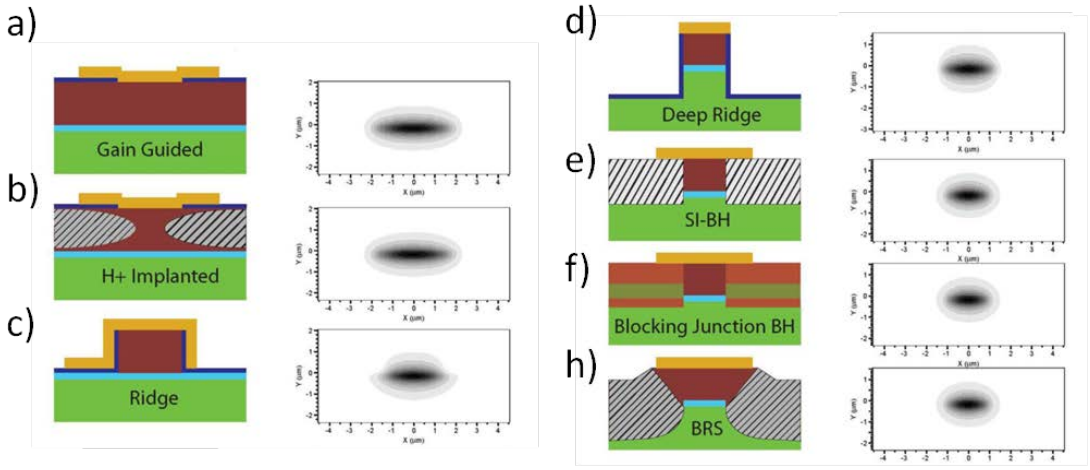

Figure 25 LD designs and relative optical model profile. From [1]. Reprinted with authors permission

On the other hand the buried heterostructure configuration (Fig. 25 (e) – (h)) provides excellent current and photon confinement at the cost of expensive growth and difficult processing.

LD etched ridge (Fig. 25 (c) and (d)) represents a fair trade-off between performance and manufacturing costs. The ridge etch depth plays a fundamental role to achieve both low threshold current density and mode stability. It is usually etched before the active region to avoid the issues explained in Chapter 2, however this design choice hampers the realization of high performance devices, in particular for narrow width ridges.

An advanced design is represented by *current aperture laser diode* (CA-LD) or *constricted mesa* laser diode. In the words of Prof. J. E. Bowers, who had proposed this design in 1985 [2] on InP-based devices, it is "*any semiconductor laser which uses an undercut (constricted) mesa as the dominant means of optical and current confinement (mushroom-stripe lasers)*".

Its schematics is depicted in Fig. 26

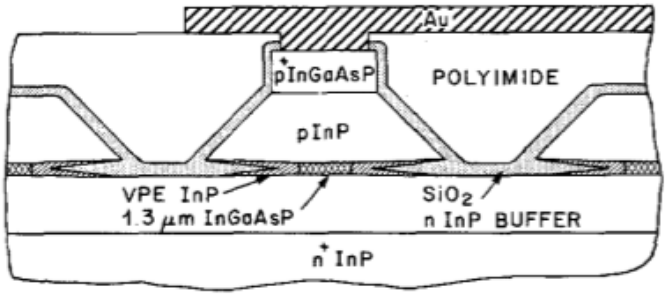

Figure 26 Original schematic of the constricted mesa LD [From 3]

In this chapter it will be described how photoelectrochemical etching (PEC etching) has been used to fabricate the first Current aperture LD on *m*- plane and *20-2-1* plane. It will be shown that by using this technique LDs can be etched past the active region, befitting the deep etch ridge design which is particularly advantageous for the narrow width ridges, and at the same time the RIE-induced damages to the active layer region (their exact extension has not been reported for nitrides but in GaAs-based devices they can as deep as a few hundreds of nanometers) can be effectively removed by laterally etching the active region of the device, good control of this lateral etching is demonstrated.

3.2 Advantages of CA-LD design

The nitride CA-LD presented in this work is essentially a deep etched ridge nitride LD with undercut into the active region. Therefore it offers a larger p-GaN surface for the same active region width of an equivalent shallow etched LD, which is advantageous for reducing the series resistance and parasitic elements, and it can benefit of the deep etch relative to the

shallow etch design advantages. The following sections will analyze in more detail these features.

3.2.1 Reduction of active region area from *n*- and *p*- layers area

The main feature of the CA-LD is the reduction of the active region area from the bottom *n*- and top *p*- layers by a selective lateral etching of the active region, which in the case of the nitride-based CA-LD is obtained by photoelectrochemical (PEC-) etching. This naturally leads to a wider p-layers area compared to both shallow and deep etch ridge LDs having the equal active region area, as schematically show in Fig. 27.

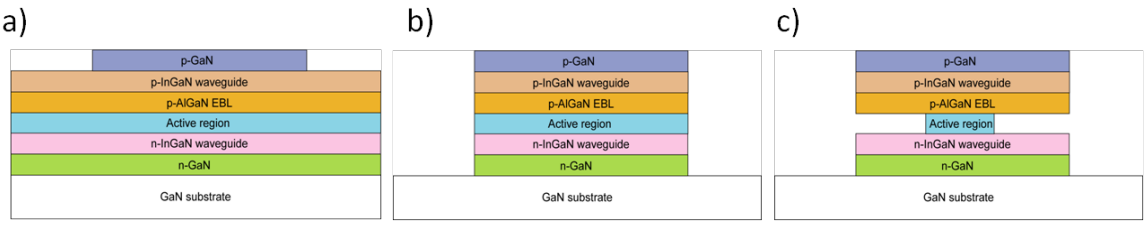

Figure 27 Nitride LD designs a) shallow etch ridge, b) deep etch ridge, c) current aperture.

A larger *p*-contact for the similar active region area is beneficial because it helps to decrease the contact resistance and to increase the speed of the device. Indeed this is desirable for device operating both in DC and in AC as the series resistance and the parasitic capacitances are important limiting factor for high performance devices and the cut-off frequency f_T scales as 1/RC, which makes this feature particularly appealing for high speed communication and in Li-Fi applications.

Initial experiments to achieve a larger p-GaN contact area have been performed by using angular RIE etching without PEC etching the device active region.

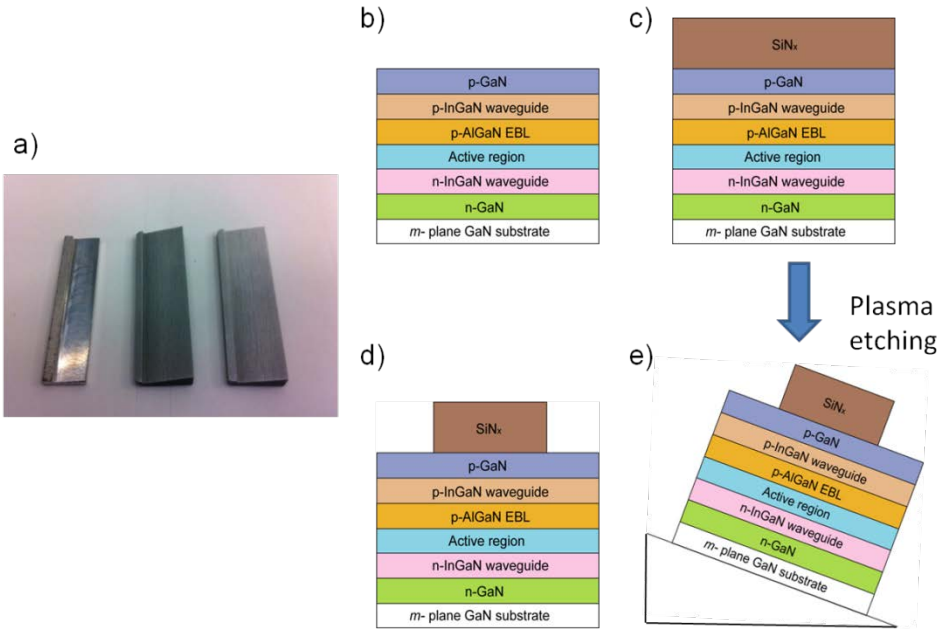

Figure 28 a) angular stage holders of different angles, b) – e) flow process of the angular RIE etch ridge

InGaN/GaN LD structures were grown by metalorganic chemical vapor deposition (MOCVD) on free-standing (10-10) bulk GaN substrates provided by Mitsubishi Chemical Corporation (MCC). Following a plasma-enhanced chemical vapor deposition (PECVD) of a blanket ~1 μm SiN_x, ridges were defined by a CF_4/CHF_3-based ICP etch of the oxide. These insulator stripes were then used as a hard mask for the subsequent Cl_2-based RIE of the GaN structure. Tilted stages covered by several microns of oxide like the ones shown in Fig. 28 a) were initially used, however the maximum angle of the available stage was 15 degrees and it was not enough to achieve a significant angle on the structure. An improvement was obtained by tilting the samples of a bigger angle as shown in Fig. 29 a) and b).

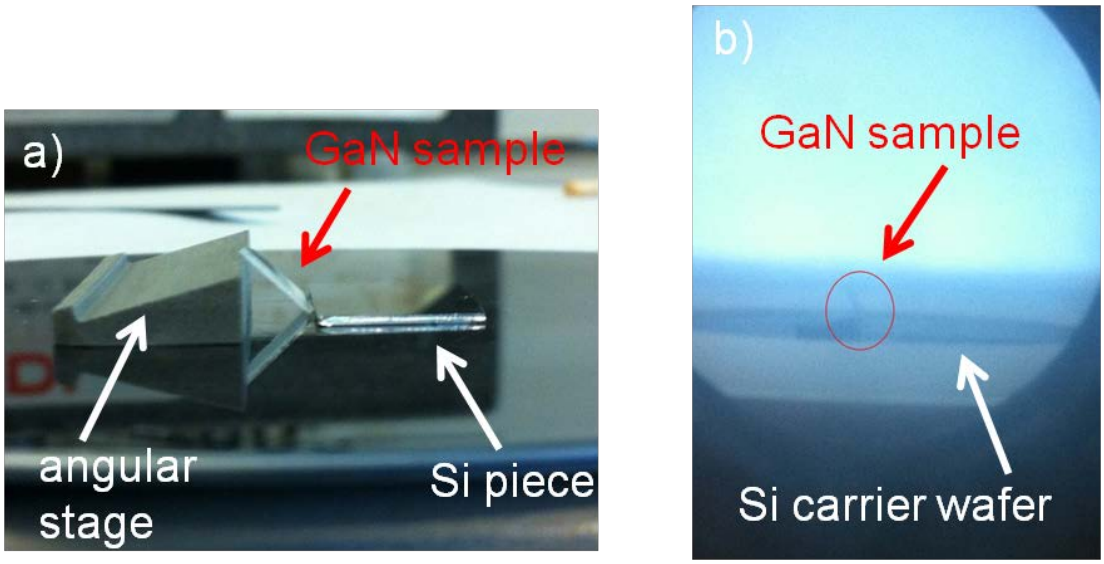

Figure 29 b) Angular RIE etching setup b) photo of the sample inside the RIE chamber.

One edge of the sample was sitting on the highest part of the angled stage (the maximum sample height allowed in the RIE system used was 11.3 mm) and the other edge of sample was fixed to a Silicon piece which in turn adhered to the carrier wafer using pumping oil.

The result of the first etching is shown in Fig. 30.

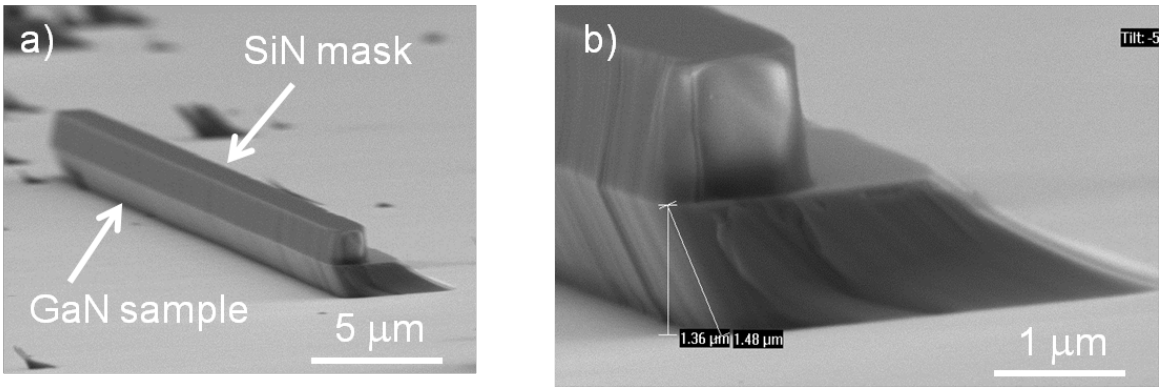

Figure 30 SEM image of angular profile after the 1st RIE angular etch.

The angular etching was then repeated on the side of the sample which was "shadowed" during the first etch and finally a triangular-trapezoidal-like shape was obtained (Fig. 31).

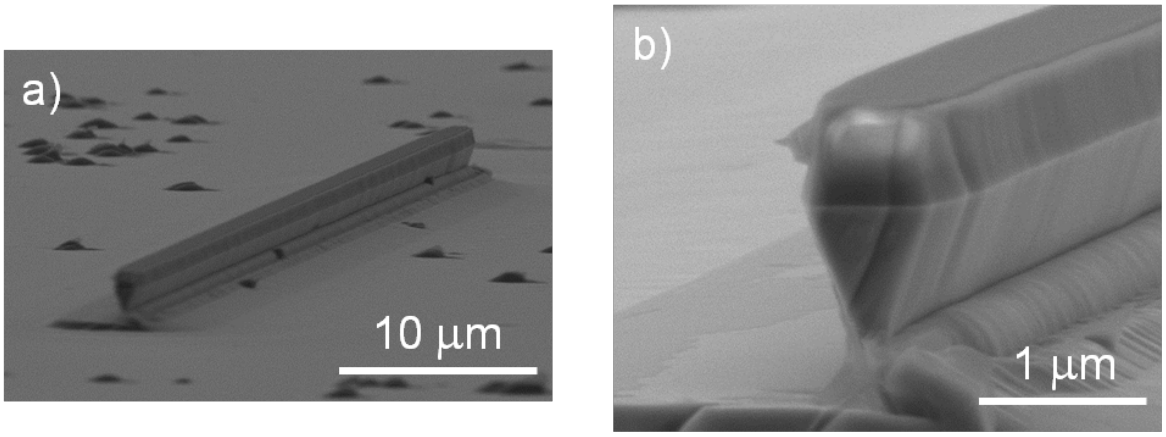

Figure 31 Triangular-trapezoidal-like shape after double-angular RIE etch

Although this technique produced quite angled sidewall and a relatively wider (~3x) p-GaN surface compared to the active layer, it has several drawbacks.

Firstly, both the uniformity and the repeatability both across stripes located on different place of the samples and also among different samples are quite poor, as it is hard to manually control the angle formed by the samples (which have different length) and the angular stage.

Secondly, the active region is directly exposed to RIE plasma and this is known to cause damage as described in Chapter 2.

Thirdly, severe striations have been observed after the etching: these are a relevant source of optical scattering loss as described in Chapter 5 and they hamper the realization of high performance devices that would be fabricated in this way.

3.2.2 Deep etch ridge and related benefits for narrow ridge LDs high performance

The ridge geometry and in particular the ridge etch depth plays a fundamental role to achieve both low threshold current density and mode stability, especially in narrow stripe width LDs. Basically, the ridge can be etched before (shallow etch design) or past (deep etch resign) the active region.

Usually, nitride edge emitting laser diodes are fabricated with a shallow etch ridge, mainly to avoid the issues related to dry etching described in the previous chapter. However, compared to the deep etch ridge design, the shallow etch ridge design presents several drawbacks which become more pronounced as ridge width becomes narrower, while no significant difference between these two designs has been noted for LDs having ridge width larger than ~5 um.

The main disadvantage is represented by the dramatic increase in the threshold current density and voltage in narrow (3 um or less) shallow etch ridge compared to deep etch ridges, as several theoretical and experimental works have demonstrated [4-7].

Threshold current densities in shallow etched *c*- plane LD as high as 3x times the threshold current densities in deep etched ridge LD (*c*- plane LDs grown on SiC substrates) having a ridge width between 1 and 2 um have been reported. Even high threshold current densities have been reported for the planar design as shown in Fig. 32

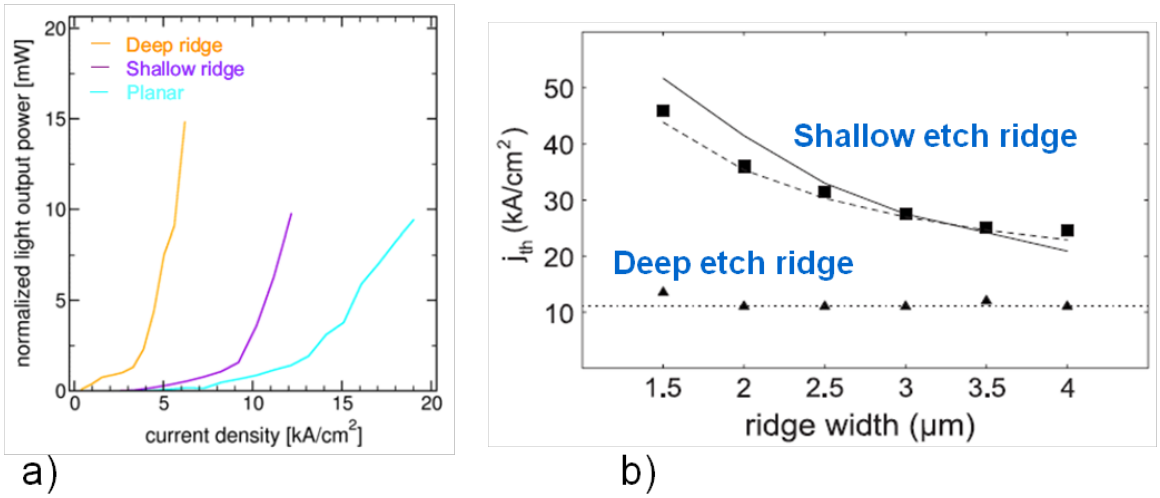

Figure 32 Threshold current densities in the planar, shallow etch and deep etch ridge design. From [4, 5]

A similar result has been shown by Kelchner at UCSB: *m*- plane LDs having ridge width of 5 um and 2.5 mm were compared, with the latter showing a decrease in threshold current densities as the LD ridge was etched past the active region.

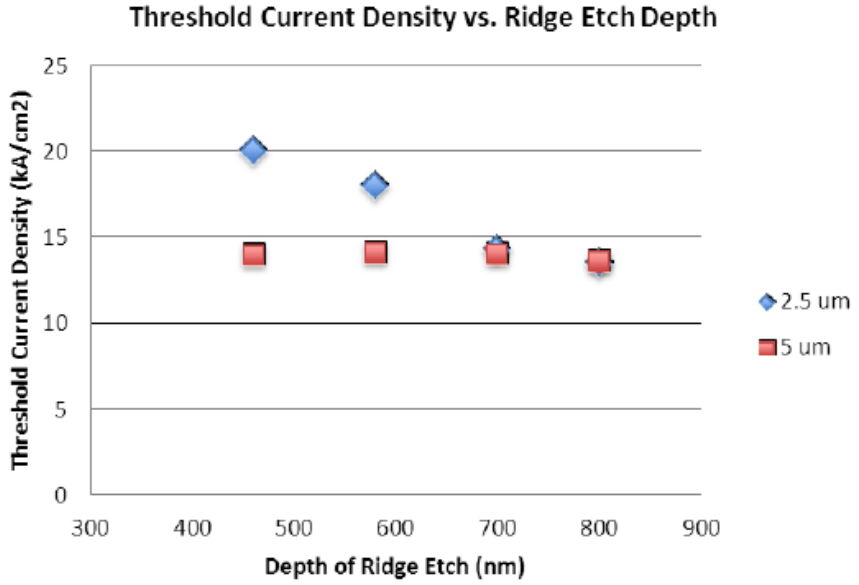

Figure 33 Threshold current density versus depth of ridge etch for 2.5 μm and 5 μm wide ridges. Reprinted with Author's permission

This study was repeated and several *m*- plane LDs having different widths and ridge etch depths have been fabricated. The ridge etch depth was stopped before the active region for both the cases, in particular in one case the ridge was etched shallower (~ 300nm) than the other (~ 500 nm) as shown in Fig. 34 a) and b). As expected, the LDs having the shallower ridge height have shown a higher threshold current density and voltage (Fig. 34 c)

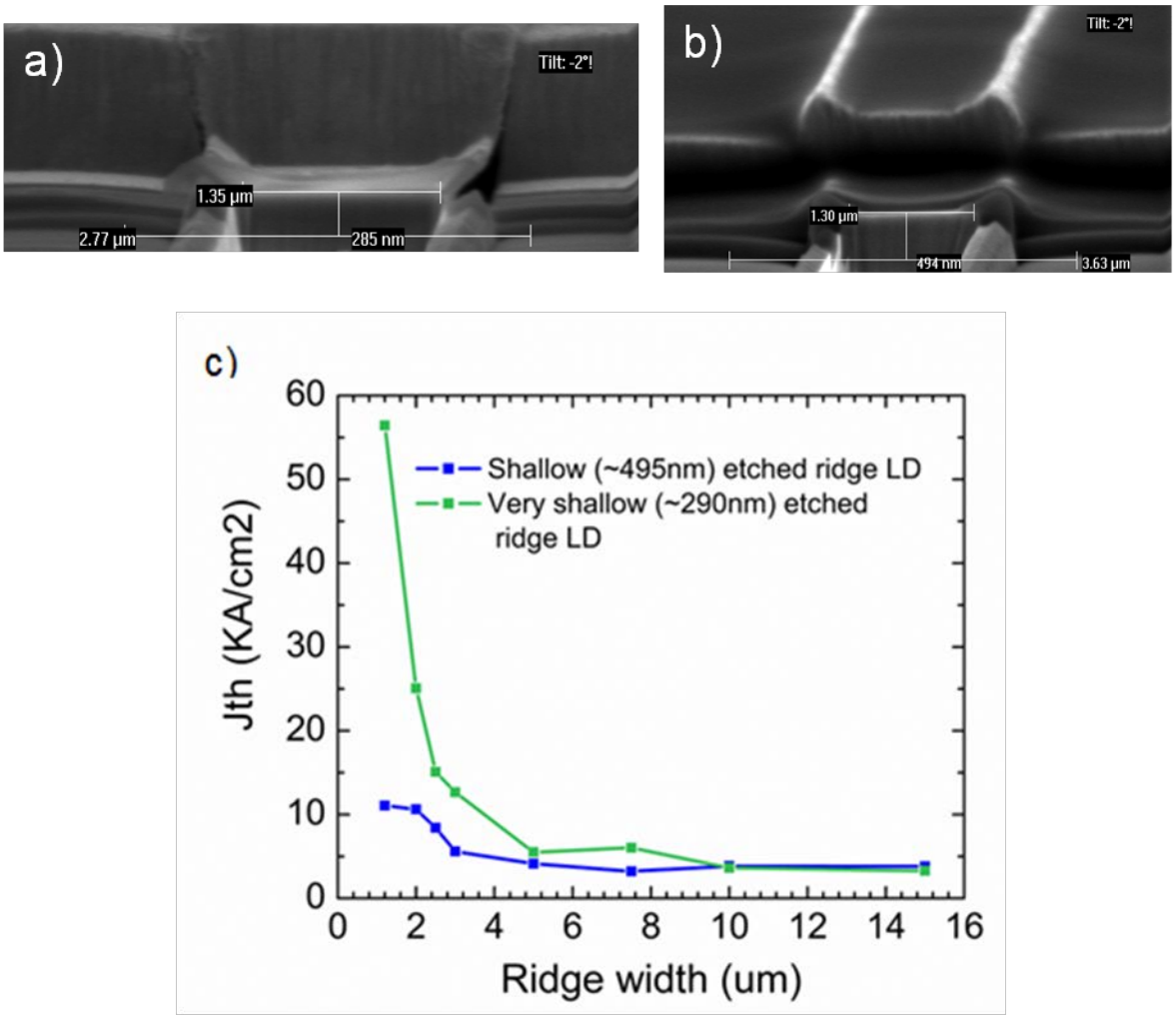

Figure 34 a) and b) SEM images of ridges having different etch depth, c) Threshold current density for ridges having different etch depths and width. The cavity length is 1200 µm

One of the main features of the CA-LD design is the fact that the LD ridge needs to be etched deeply, in particular past the active region, such that the MQW are exposed to the electrolyte during the PEC etching step.

As a consequence, this design is expected to offer the same advantages of the deep etch design and also provide additional benefits as current aperture laser diodes realized in zincblende III-V have shown [8-11].

In particular, compared to a typical shallow etched ridge LD, a CA-LD is expected to have the following benefits:

- Increase of the current confinement and elimination of the typical current leakage pathways

  Current leakage pathway can occur in shallow etch LD as depicted in Fig. 36. This phenomenon can be higher in the AlGaN-cladding free configuration as GaN is in general less resistive than AlGaN and it has been estimated to be as long as 3 μm in 1.8 μm wide ridge [12] and it becomes bigger as the LDs ridge becomes narrower [13].

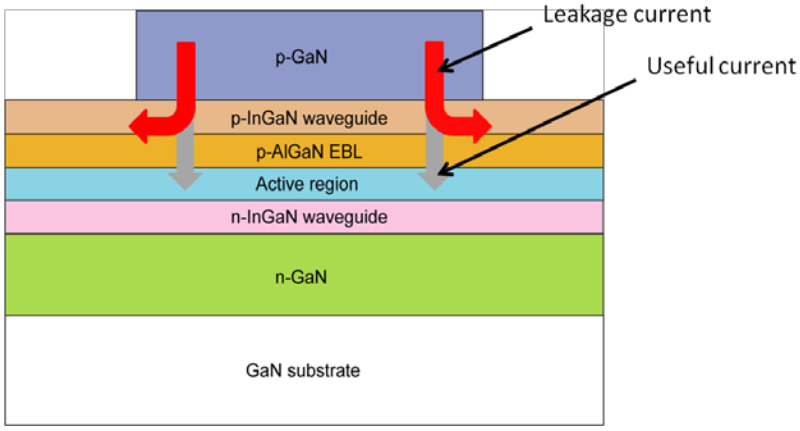

Figure 35 Schematic showing possible leakage pathways

- Reduce the absorption from the unpumped active region to the sides of the ridge

In the case of shallow etch ridge, the current flowing beyond area directly under the ridge can pump the active region without causing the carriers population inversion needed for lasing. Therefore those MQW will not contribute to the positive gain but in fact they will become semiabsorbing or absorbing as shown in Fig. 37.

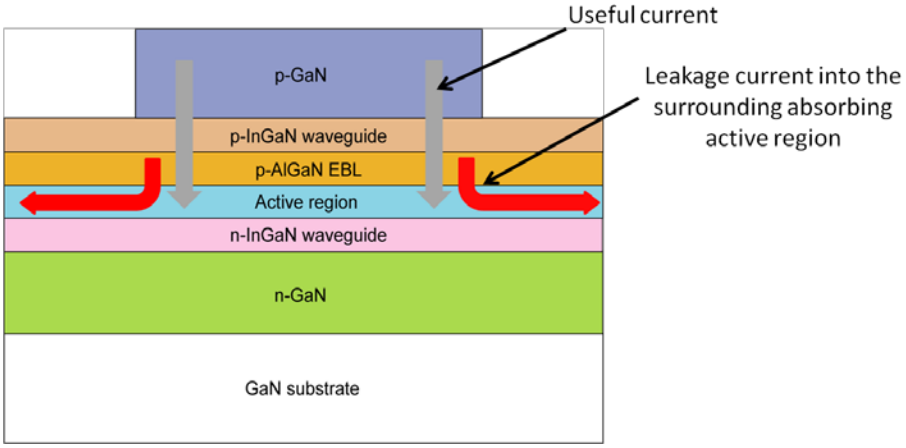

Figure 36 Schematic of leakage current into region beyond the ridge width which becomes semiabsorbing or absorbing

Figure 38 depicts a simulation of the electric field intensity for the shallow etched ridge LD and the deep etch using FIMMWAVE, a commercially available 2D waveguide mode solver.

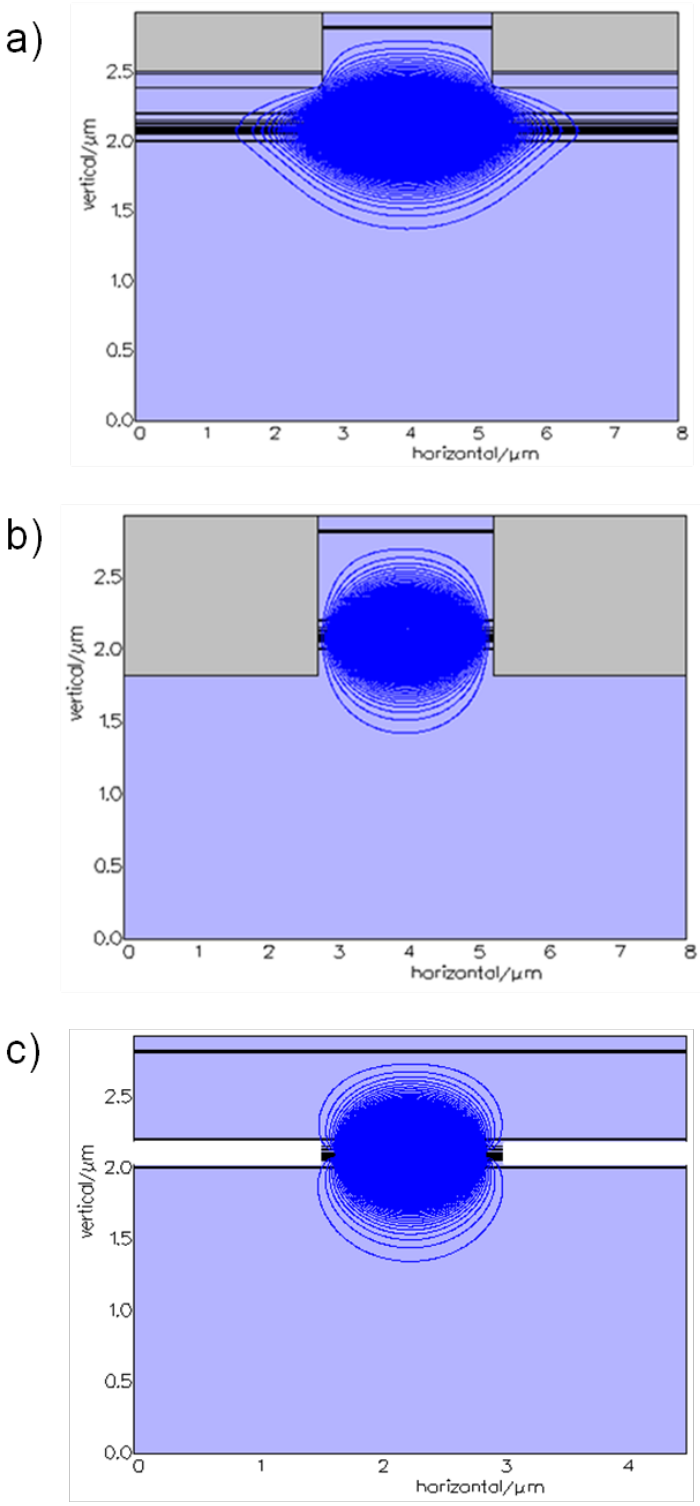

Figure 37 Simulation of the electric field intensity for (a) the shallow etched ridge LD, (b) the deep etch ridge LD and (b) the CA-LD.

Fig. 38 (a) shows that the intensity of the electric field can extend well beyond the area below the ridge and this indicates that a relatively long part of the active region to the side of the ridge can "feel" optical field although it does not receive enough current to produce gain. Assuming an ambipolar carrier diffusion to a lateral distance of 220 nm to either side of the ridge was assumed for the shallow etched ridge laser, this reduces the optical absorption in that region to 750 cm^{-1}. Beyond that diffusion length, the absorption in the unpumped wells[36,37] can be assumed to be 7500 cm^{-1}. By contrast, these losses are not present in the deep etch ridge nor in the CA-LD design since the quantum wells are etched away as shown in Fig. 38 (b) and (c).

The refractive index of the PEC etched current aperture was assumed to be 1, corresponding to perfect air gaps. Results of simulations of average internal losses vs. different diffusion lengths for different ridge etch depths are shown in Fig. 39.

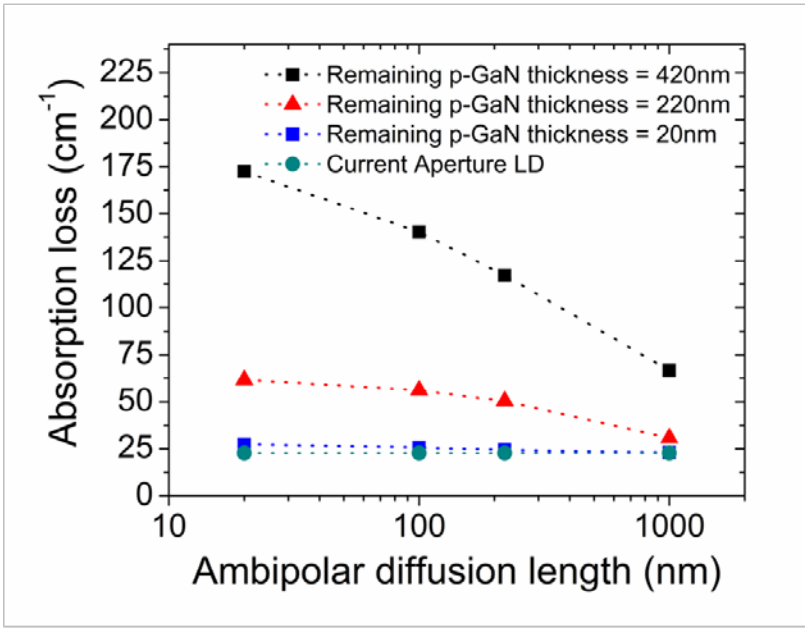

Figure 38 simulations of average internal losses vs ampipolar diffusion lengths for different ridge etch depths

On the other hand, this has a deep impact in the scattering loss: as the electric field interacts with the sidewalls, these need to be as smooth as possible to avoid roughness-induced scattering loss as detailed in Chapter 5.

- Effect on the refractive index: confinement factor change and reduction of the antiguiding factor

The change of the optical mode shape with the ridge etch depth shown in Fig. 38 suggests also that the effective index step Δn between the region below the ridge and the surrounding regions changes as well. The profile shape of the optical mode (and in part also the roughness-induced scattering loss, as shown on Chapter 5) depends in fact on the difference of such effective refractive indexes.

The effective index step does not depend only on the epilayers which the LD is made of but it has a rather complex dependency on several parameters.

$$\Delta n = \Delta n_{eff} + \frac{\partial n}{\partial T} \cdot \Delta T + n_{eff} \cdot \alpha_{thermal} + \frac{\partial n}{\partial N} \cdot \Delta N$$

where the term Δn_{eff} represents the effective index step produced by the different semiconductor, the term $\frac{\partial n}{\partial T} \cdot \Delta T + n_{eff} \cdot \alpha_{thermal}$ represents the change due to temperature ($\frac{\partial n}{\partial T} \cdot \Delta T$) and thermal expansion of the cavity $n_{eff} \cdot \alpha_{thermal}$ and finally the last term represents the change in the effective index as more carriers are injected into the LD [13].

The term $\frac{\partial n}{\partial T} \cdot \Delta T$ is general assumed to be on the order of $10^{-4}/K$ for a LD lasing at 450 nm, it can been estimated that the term $n_{eff} \cdot \alpha_{thermal}$ is $\sim 1.48 * 10^{-5}/K$

assuming a refractive index $n = 2.486$ and a thermal expansion coefficient $\alpha_{thermal} = 5.59 * 10^{-6}/K$ [14].

The index antiguiding term $\frac{\partial n}{\partial N} \cdot \Delta N$ depends on the injected current: the refractive index in the region below the ridge decreases as the injection current increases and therefore also the step index between this region and the regions surrounding, which is responsible for the lateral confinement of the mode, decreases. This effect is called antiguiding and it is particularly pronounced in shallow etch ridge LDs as more current needs to be injected to achieve lasing threshold [15,16].

It is derived from the Kramers-Kronig relation [17] and it is formally defined as the ratio of the imaginary part to the real part of the refractive index. It can also be expressed as function of the differential gain as

$$\alpha \equiv -\frac{dn/dN}{dn_i/dN} = -\frac{4\pi}{\lambda}\frac{dn/dN}{dg/dN} = -\frac{4\pi}{\lambda \cdot a}\frac{dn}{dN}$$

where α is the differential gain, λ the wavelength of the device, n the refractive index, n_i the injected carriers, N the total carrier density.

This parameter is larger at longer wavelengths because the change of gain with carrier density change at the long wavelength is smaller compared with the change of gain at the short wavelength end due to the fact that the density of states at the long wavelength end is mostly filled [18]. For nitride LDs emitting in the UV-green range antiguiding values up to ~4.1 have been measured [19].

3.3 Fabrication process and technology of CA-LD

Reduction of the active region from its top and bottom epitaxial layers have been obtained selectively wet etching the InGaAsP active layer from InP-based structure.

As described in Chapter 2, this has been achieved in the InGaAsP material system by using mixtures of H_2SO_4:H_2O_2:H_2O, $C_6H_8O_7$:H_2O_2:NH_4OH, HCL: H_2O. Fig.40 shows some of these devices.

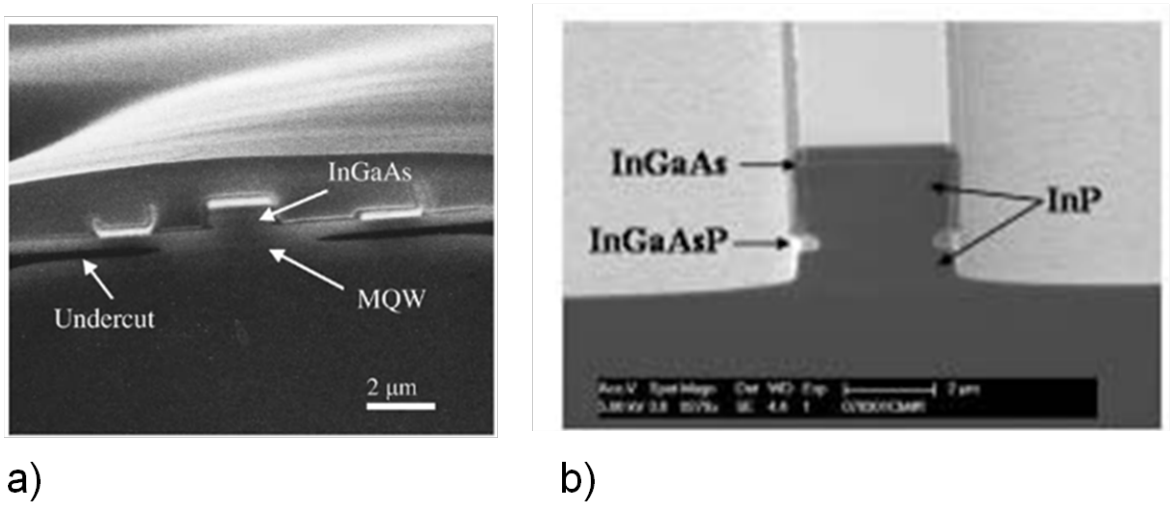

Figure 39 Selective undercut of the active region InGaNAsP strcture

As described in Chapter 2, the Nitrides system lack of a conventional wet etching technique and rely mainly on chlorine-based dry etching methods whose main drawbacks have been described in the previous chapter.

Photoelectrochemical etching (PEC etching) is powerful technique wet etch nitrides and when used in conjunction with dry etching undercut as those obtained in other III-V compounds can be obtained. The following section describes the fabrication process of the

Nitride Current Aperture LD by PEC etching the active region of *m*- plane and 20-2-1 blue LD and its differences with respect to the standard edge emitting LD fabrication process.

3.3.1 Brief summary of Standard edge emitting LD process

The standard edge emitting fabrication process for non c-plane LD at UCSB has been mainly developed by M. Schmitt and R.M Farrell. The flow process schematic is summarized in Fig. 41.

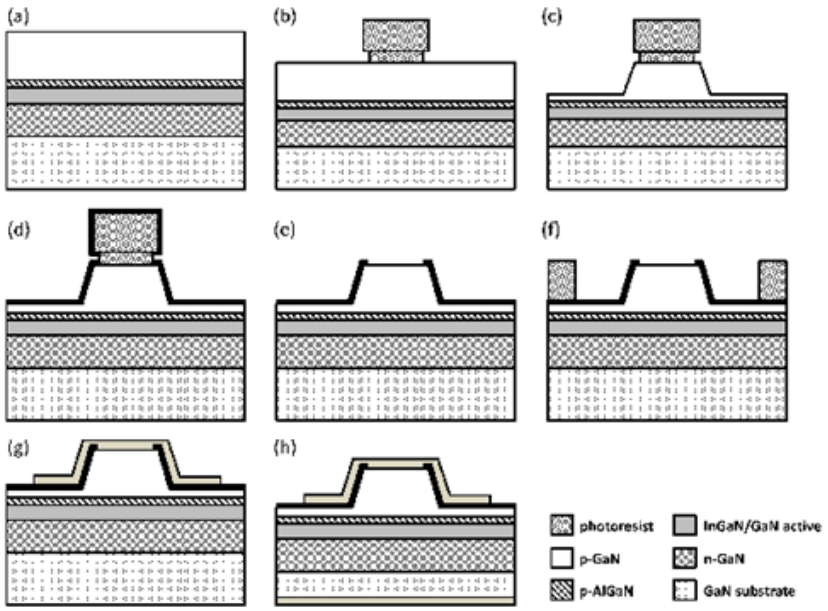

Figure 40 Schematic of the flow process of the standard edge emitting shallow etch LD

This flow process is relatively simple and fast and it allows a turn-around of devices in about 4 days. It consists of the following steps:

- Ridge definition by standard UV lithography (a – b)
- Ridge etch (c)

- Insulator deposition on the ridge sidewall and lift-off of insulator from the top of the ridge (d and e)
- Metal contact depositon on the p- and n-side (f – g)
- Facets etch (and coating) (h)

This process takes advantage of using the same photoresist as mask in two different steps: ridge definition by standard UV lithography and lift-off of the top insulator such that the field insulator remains only on the sidewalls without any additional etching on top of the p-GaN ridge, (self-aligned process).

Unfortunately this key feature is not easily applicable to the CA-LD design and the photoresist can not be used as mask because it would dissolve into the KOH solution during the PEC etch step (the photoresist developers are in fact KOH-based).

As a consequence, a new flow process had to be designed to fabricate the CA-LD.

3.3.2 CA-LD process with undercut unfilled

This fabrication process needs to meet some basic requirements:

- It needs to be compatible with immersing the sample into the KOH solution for several minutes during the PEC etch step
- It needs to include the light-blocking mask to define the final width of the active region as described in Chapter 2
- It needs not to have a dry-etching step on top of the pGaN in order not to damage it.
- It should protect the sidewall of the p-GaN so that these will not be etched during the PEC etching by hole overflowing from the MQW

The fabrication process starts with defining what will be the area of the active region of the final device after the PEC etch. As explained in Chapter 2 this is achieved by masking the active region with opaque metal masks which are intended to block the light causing the PEC etch process to start by generating electrons and holes.

A thick metal layer (Pd/Au 300/5000 Å) was therefore patterned by electron beam evaporation and liftoff after ridges of different length and width have been defined.

Instead of photoresist which would dissolve during the PEC etch step, an insulator layer was used as hard mask to etch the ridge. This layer needs to be thick enough to stand about ~ 10 min of Cl_2-based RIE etching which is used to the etch the LD ridge past the active region such that the active layer can be exposed to the electrolyte during the PEC step.

Initially a thick SiN-based of ~1 μm of SiN was deposited by PECVD at 250 C on top of the bare LD epitaxy after the sample had been activated (650 C for 15 min in air). The SiN was then patterned by standard UV lithography and ICP. Although SiN is a good hard mask, it has a internal tensile stress which is not easy to control, in particular on small samples like the ones processed in this work. As a result, the PEC etched structures were subjected to an internal tensile stress which caused the upward bending and sometimes their breaking when the undercut was being created. Examples of this phenomenon are shown in Fig. 42 (a) and (b).

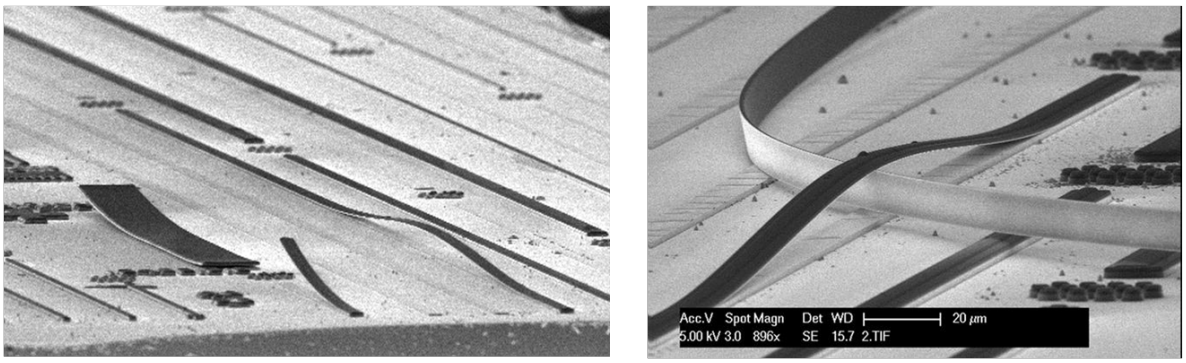

Figure 41 Example of tensile stress caused by thick SiNx hard mask

This issue was addressed by depositing a ~1.5 μm thick low-stress SiNx/SiOy/SiNx multilayer film by Advanced-PECVD at 300 C. Both these insulators are transparent at the light radiation used during the PEC etch (~ 405 nm). The purpose of such stack is to alleviate the possible bending or breaking of the structure by reducing the layer total internal strain, having the SiO_x (SiN_y) an internal (compressive) stress respectively. Such multilayer film has been used in order to compensate for the stress that a thick layer of SiN (or of SiO) would introduce to the structure, in particular during and after the PEC etch. Ridges of varying widths and lengths (aligned on the previously defined metal masks) were defined by a CF_4/CHF_3-based ICP etch of the $SiN_x/SiO_y/SiN_x$ multilayer. These insulator stripes were then used as a hard mask for the subsequent Cl_2-based RIE of the p-GaN. After the etch through the p-GaN, the structure was covered again with a thin $SiN_x/SiO_y/SiN_x$ multilayer (~100 nm) to protect the p-GaN surface from the electrolyte solution. An uncovered p-GaN surface, once oxidized by photogenerated holes overflowing from the QWs, would actually roughen or even etch during the PEC etch step. Next, a 100/5000 Å Ti/Au layer was deposited on the backside of the samples for the PEC etch cathode. Finally, the thin $SiN_x/SiO_y/SiN_x$ multilayer (~100 nm) was etched from the field using a self-aligned process

that relied on the thicker dielectric on top of the ridge and the slow RIE rate of the dielectric on the ridge sidewall. The samples were then etched down to the n-GaN layer, exposing the MQW for the subsequent PEC etch step. Before proceeding with that, the sample was immersed in an HCl solution in the dark for a few minutes to remove the native oxide. The PEC etch was performed by immersing the samples in a 0.1Mol KOH solution at room temperature with no external bias. The light source for generating carriers into the active region was a 405 nm LD with an output intensity of ~200 mW/cm^2 at the sample. These fabrication steps are summarized in Fig. 43

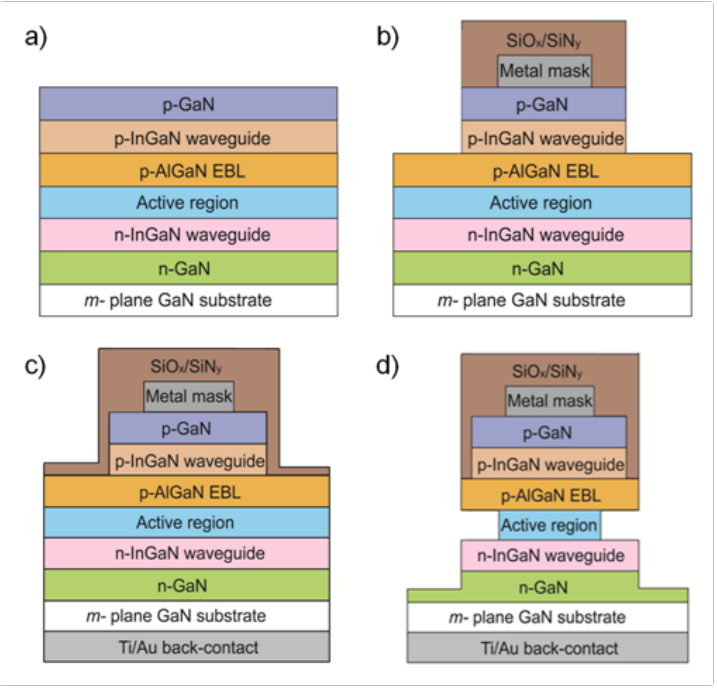

Figure 42 Fig. 1 (Color online) Schematic of the process flow of the LD structure prior to PEC etch. (a) The LD structure after MOCVD growth. (b) The LD structure after depositing an opaque metal layer, depositing a ~1.5 µm thick low-stress $SiN_x/SiO_y/SiN_x$ multilayer, etching the $SiN_x/SiO_y/SiN_x$ multilayer, and etching the p-GaN. (c) The LD structure after depositing a thin $SiN_x/SiO_y/SiN_x$ multilayer (~100 nm) and depositing a 100/5000 Å Ti/Au layer on the backside of the samples for the PEC etch cathode. (d) The LD structure after etching away the thin $SiN_x/SiO_y/SiN_x$ multilayer (~100 nm) and etching down to the n-GaN layer by a self-aligned etching process using the previously defined ~1.5 µm thick $SiN_x/SiO_y/SiN_x$ multilayer mask.

For both structures, ~400 nm SiO_2 was deposited on the sides of the ridge waveguide to act as an insulator, followed by the deposition of 100nm of indium tin oxide (ITO) by e-beam evaporation and finally a stack of 300/10000 Å of Pd/Au was deposited on top of the ridge to form the p-contact. The mirror facets were created by RIE etching. In the case of the sample discussed on Chapter 4, the facets were coated and for some LDs they were etched by Focus Ion beam to improve their smoothness and verticality as described in Chapter 4. The final device is shown in Fig. 44

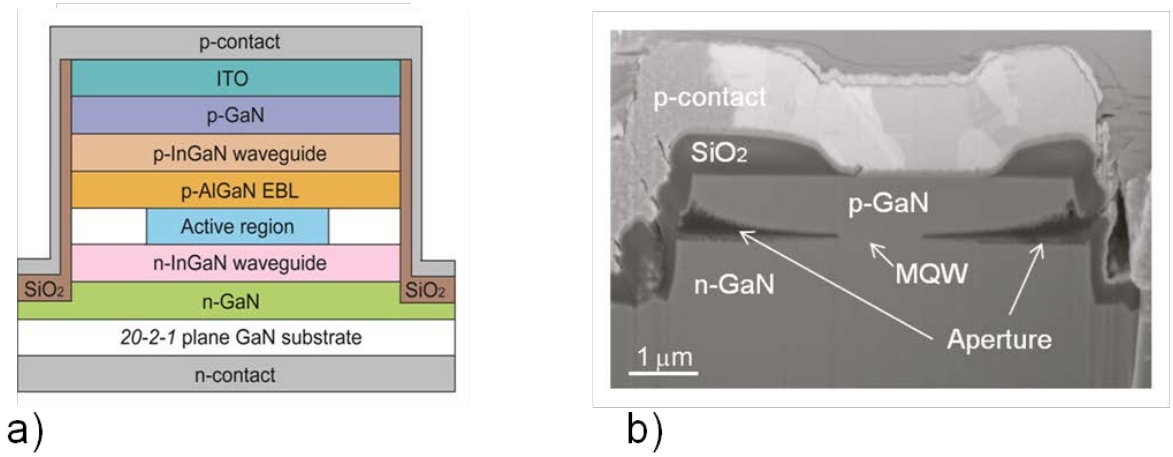

Figure 43 Schematic and FIB/SEM image of a nitride CA-LD fabricated on *20-2-1* crystal plane

3.3.3 CA-LD process with undercut filled

The process described in the previous section has shown good performance and true CW operation was achieved for a ~ 1.5 μm wide active region (~ 4.5 μm wide p-GaN area) laser

bar, as described in Chapter 4. However it suffered from a relatively low differential efficiency.

As explained in Chapter 5, this is can be caused by the roughness-induced scattering loss which depends on several parameters, among which the difference between the effective refractive index of the unetched active region and the PEC etched aperture region, respectively:

$$\Delta n_{eff}(x) \equiv n^2_{eff,unetched} - n^2_{eff,aperture}(x)$$

Typically $\Delta n_{eff}(x)$ is a step function but, in general, the index profile can be distributed, i.e. in CA-LD design it can take into account the tapered shape of the aperture, which is related to the different polarization fields of the crystal planes.

A new fabrication process was therefore designed in order to decrease the step-index $\Delta n_{eff}(x)$ and fill the aperture. This needs to meet the same requirements of CA-LD whose undercut is not filled and it has some additional constraints.

In particular, the insulators used to fill the aperture were deposited by ALD at 300 C, as a consequence the lift-off process used to pattern the SiO2 field insulator can not be used.

Moreover, as the ALD is conformal it is necessary to etch away the thin insulating layer (~ 60-80 nm thick) from the top of the p-GaN. This goal could be achieved easily by wet etching for example by dipping the sample into dilute HF or into BHF. However, this operation needs to be controlled in an extremely precise way since a thin remaining layer of insulator can dramatically increase the operating voltage of the device and even prevent the lasing condition, on the other hand over etching by dipping the sample for a longer time into the HF solution can lead to the etching of the insulating layer deposited inside the aperture.

Dry etching would allow a more precise control of the etch depth without the risk of etching the insulators deposited inside the aperture, however it is necessary to protect the p-GaN surface during this etching operation so as not to cause damage to the *p*- layers.

The fabrication process of the CA-LD with aperture filled is described in Fig. 45. Immediately after the sample has been activated, a ~100 nm thin layer of ITO is deposited by e-beam deposition at 650 C. The ITO is deposited while the sample is being heated because this improve both the transparency and conductivity of ITO.

A thick photoresist is used to pattern stripes of different width and length the ITO layer which is etched by a mixture MHA (20/10/4 sccm) using a RF power of 370 V. The etch is performed into multiple steps – with intervals of 1 min of O2 cleaning at a power of 170 V – to avoid deteriorating the photoresist (in particular the accumulation of carbon-based compounds) which is in fact used for the subsequent immediate etch of the LD ridge past the active region by Reactive Ion Etching (RIE). The sample is then dipped into DI water to break possible Carbon-Chloride residues caused by the RIE etching and N_2-dry. Next, as for the CA-LD with unfilled apertures, a 100/5000 Å Ti/Au layer is deposited on the backside of the samples for the PEC etch cathode. On top of the ridges and on the field, stripes of different length and width are defined by standard stepper lithography and a thick metal layer (Ti/Pt 300/5000 Å) is deposited in order to block the light coming from the top and the light reflected from the rough substrate which helps to degrade the PEC etch resolution as described in Chapter 2. Ti/Pt are used instead of Pd/Au as Ti works as better sticking layer than Pd to ITO and Pt is preferred to Au as it does not sputter during the subsequent dry etch steps so it does not contaminate the etching chamber. Before the actual PEC etch step, the sample is put into the O2 ashing chamber for ~ 30 sec to further clean the sidewall from

possible carbonaceous residues of photoresist, then into an HCl solution in the dark for a few minutes to remove the native oxide. The PEC etch was performed by immersing the samples in a 1 Mol KOH solution at room temperature with no external bias. The light source for generating carriers into the active region was a 405 nm LD with an output intensity of ~200mW/cm^2 at the sample. The sample was then loaded into the ALD to fill the aperture with insulator in order to decrease this step index between the unetched and the PEC-etched region.

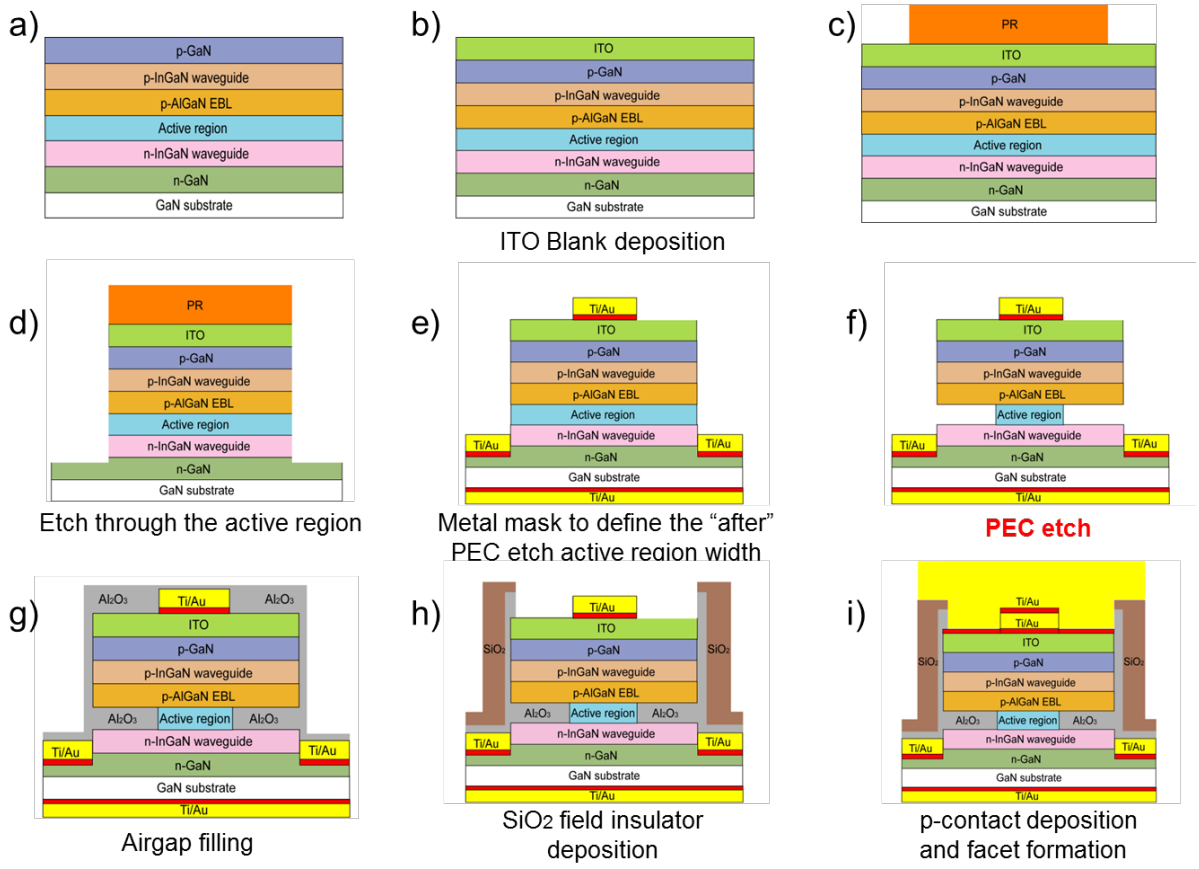

Figure 44 flow process of the CA-LD whose aperture have been filled

Several types of insulators have been tried: HfO_2, Al_2O_3, SiO_2. Although HfO_2 is preferable has it has the highest refractive index of the three (the refractive index at 440nm is 1.466, 1.780 and 2.145 for SiO_2, Al_2O_3 and HfO_2 respectively), filling the gap with HfO2 is hard because it is highly reactive and it tends to clog the aperture once it starts depositing. Fig. 46 shows SEM images of samples which have been covered by HfO_2 but the aperture was not filled.

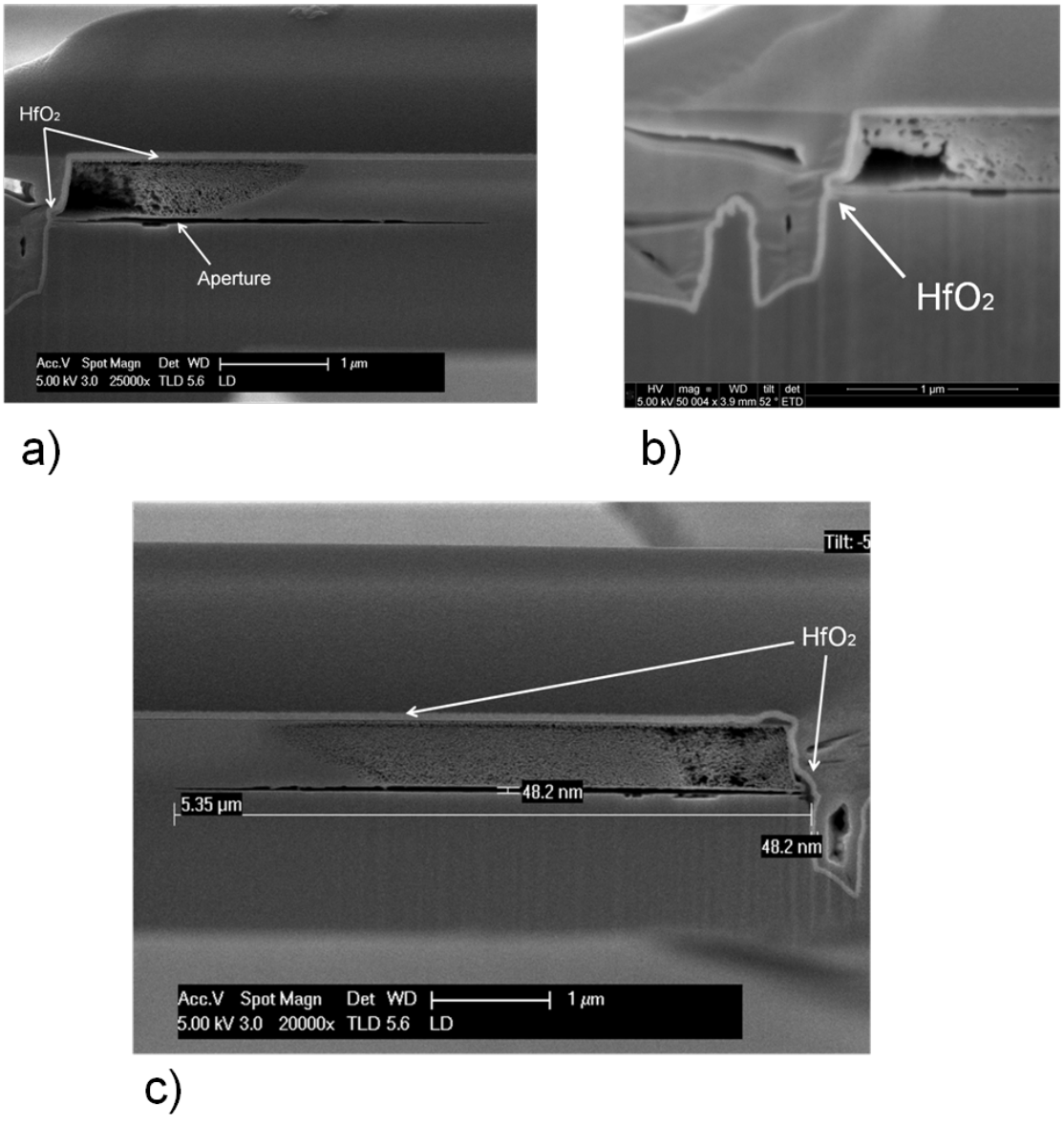

Figure 45 SEM image of CA-LD which have been covered by HfO2. This oxide did not fill the aperture.

By contrast, both SiO_2 and Al_2O_3 provided better results and aspect ratio of ~500 have been filled in this way after carefully choosing the proper pumping and purging time of the precursors as show in the SEM images below.

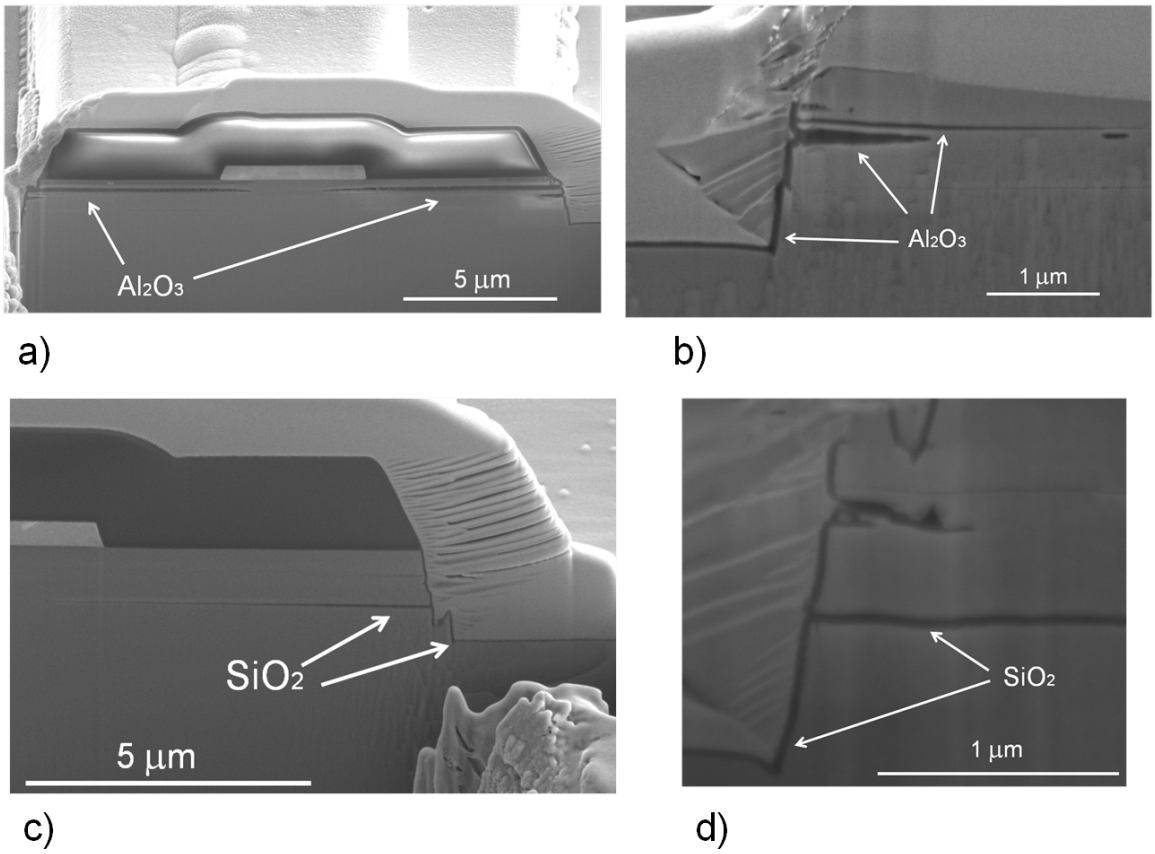

Figure 46 SEM images of CA-LDs whose aperture have been filled by Al_2O_3 and SiO_2

Finally it was tried BCB 4022-35. This photoresist has a refractive index at 440 nm equal to 1.575. SEM images show that it was possible to fill the aperture although it was noted the formation of some bubbles which probably form during the curing step (Fig. 48).

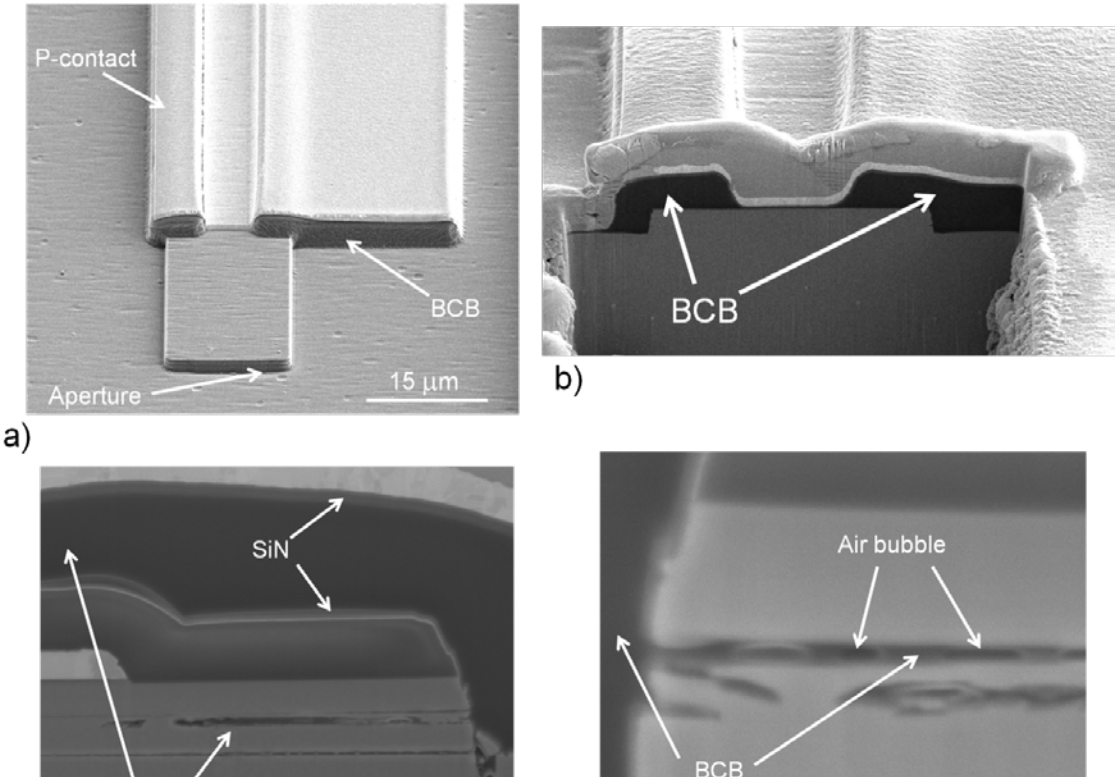

Figure 47 SEM/FIB images of CA-LD whose aperture have been filled by BCB 4022-35

Although from one hand BCB has the advantage of requiring just to be spinned as a common photoresist, it also needs to be cured for several hours at 600 C, so the total processing time of this step is slightly longer than the ALD deposition. Moreover, it is well known that metals usually do not stick well to BCB so it needs to be encapsulated between a SiNy/SiO_x stack. In this way a good metal adhesion of the p-contact was achieved as shown on Fig. 49 (c), however this adds additional complexity to the fabrication. Finally it is not easy to open windows by UV lithography into the BCB and the minimum features width is usually ~3.5 µm as shown in Fig. 49 (a) and (b).

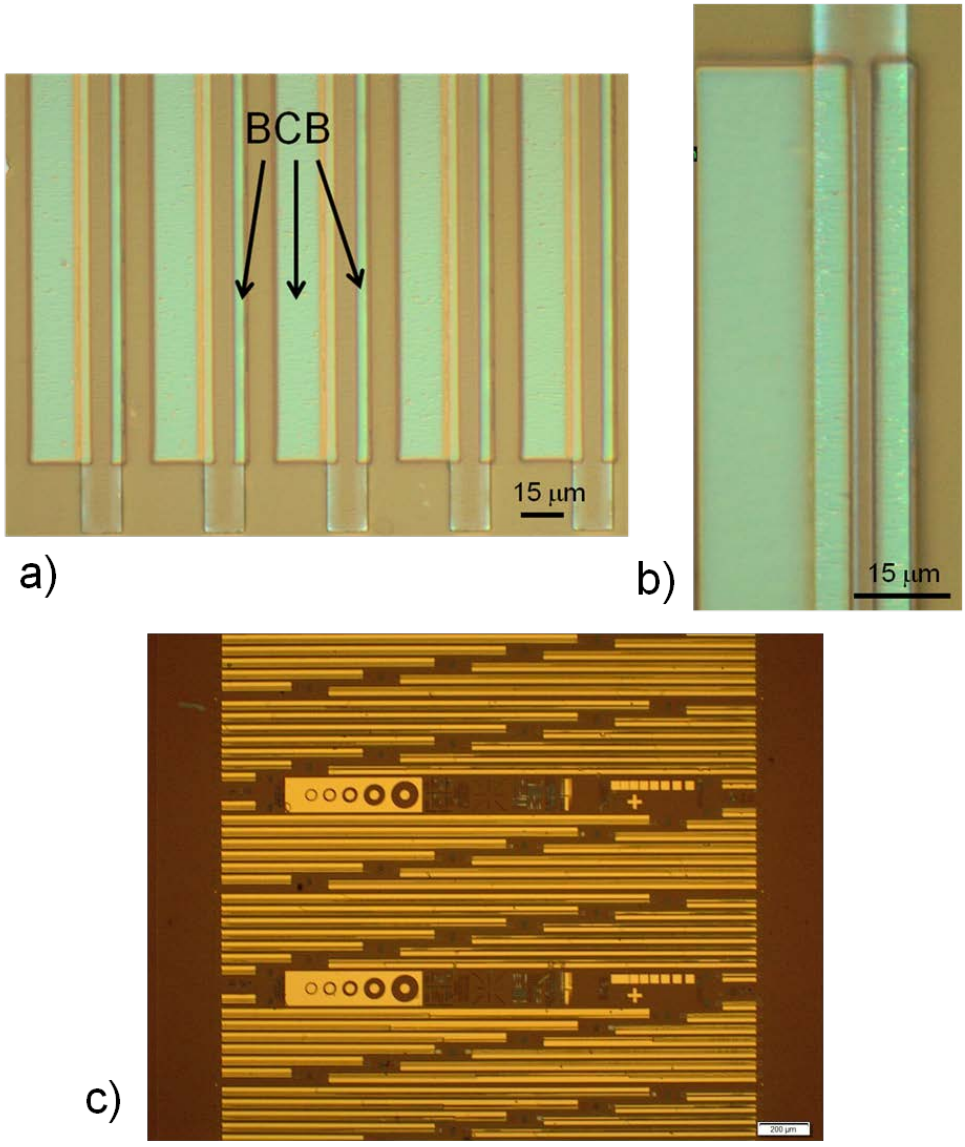

Figure 48 a) and b) BCB 4022-35 on top of the LD ridge and c) optical image showing good metal adhesion after depositing a stack of SiNx/BCB/SiOx

ALD deposited oxide on top of the p-GaN is then dry etched. The pGaN is protected during this etching by the metal mask which are not removed after the PEC etch step and by the ITO layer (~100nm). A thick SiO2 field insulator is then deposited, followed by deposition of p-contact and facets etch by RIE (or FIB). A cross section of the final device is shown in Fig. 50.

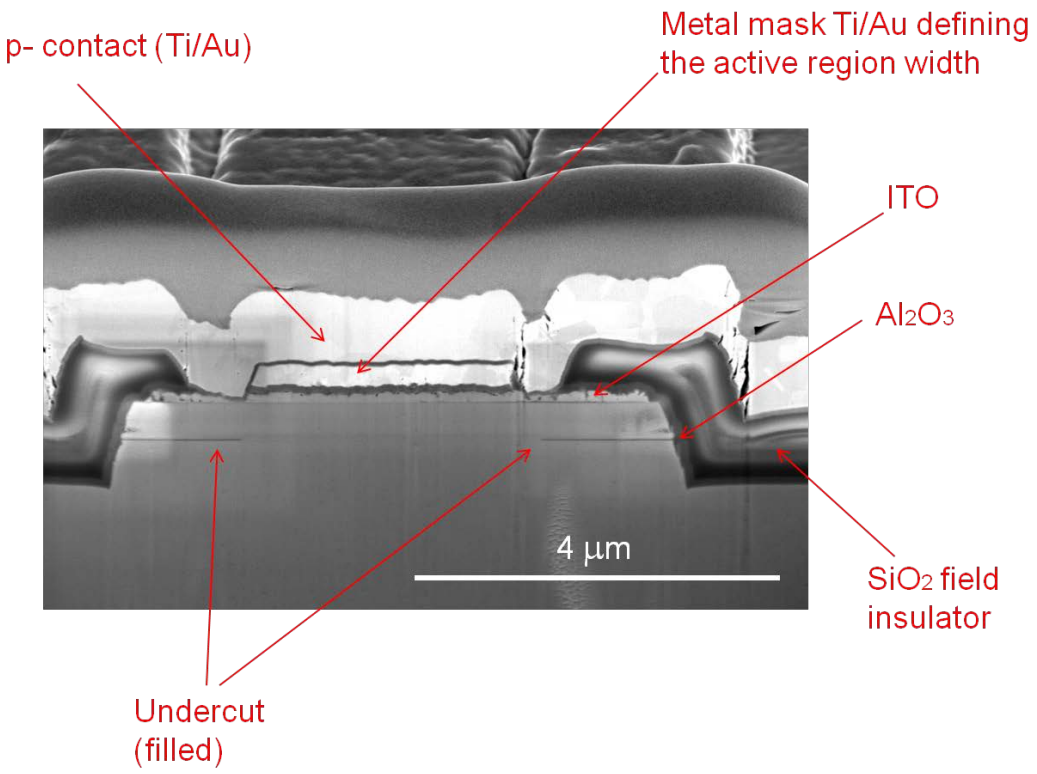

Figure 49 FIB-SEM image of a CA-LD with apertures filled by Al2O3

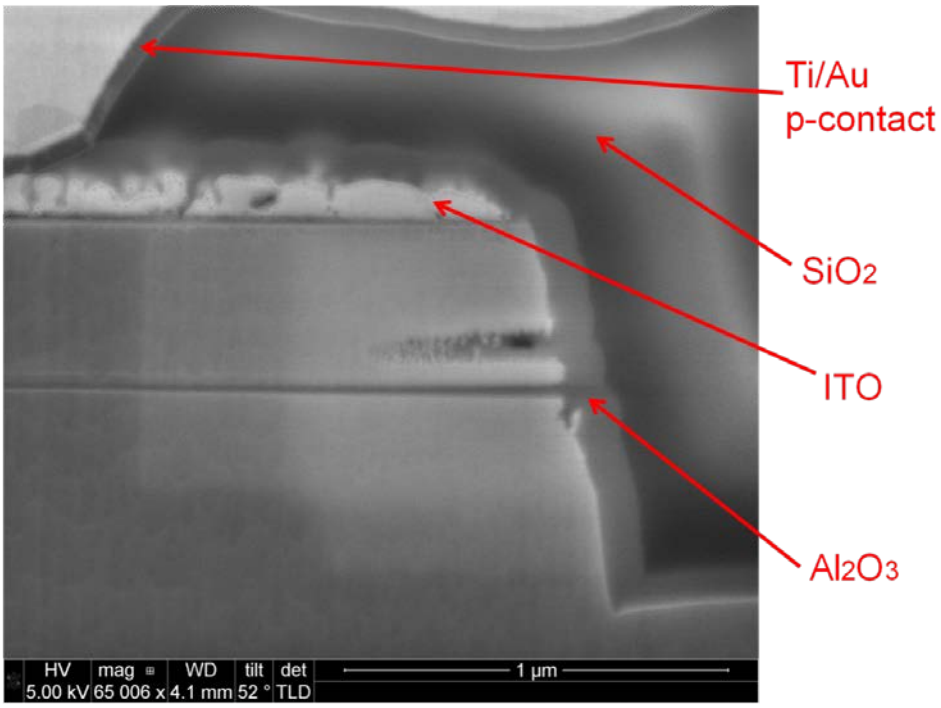

Figure 50 SEM-FIB detail of the aperture filled by Al_2O_3

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Chapter 4

CA-LDs Results and Characterization

In this chapter the results of CA-LDs grown on free-standing *m*- plane (10-10) and *(20-2-1)* bulk GaN substrates provided by Mitsubishi Chemical Corporation (MCC) are presented.

All the InGaN/GaN LD structures were grown by metalorganic chemical vapor deposition (MOCVD). The performance of the CA-LDs was evaluated by comparing it with that of LDs having nominally identical epistructure and active region width.

4.1 Background on basic LD characterization and Laser Facets

A (CA) edge-emitting LD is essentially a Fabry-Perot cavity where the light generated into the active layer (which has an undercut) propagates along the longest direction of the device and bounces back and forth between the two end facets. The portion of the light escaping from the cavity produces the output light of the device. Therefore it is clear that the quality of the laser facets plays a fundamental role in determining the output power, the threshold current density, the differential efficiency and ultimately the extraction of the internal parameters of the device.

In the case of an uncoated LD facet and assuming an angle of incidence for light of zero degree and extremely smooth facets, the facet reflectivity is expressed [1] as:

$$R = \left(\frac{n_{LD,eff} - n_{air}}{n_{LD,eff} + n_{air}}\right)^2$$

where $n_{LD,eff}$ and n_{air} are the effective refractive index of the LD structure and air, respectively.

The refractive index step between the LD structure, as computed by FIMMWave [2], and air is approximately 1.6 at 450 nm, therefore the previous formula predicts a power reflectivity of approximately 18% for an uncoated facet.

The mirror loss at a single facet is averaged across the entire length of the cavity, and is expressed as

$$\alpha_m = \frac{1}{L} ln\left(\frac{1}{R}\right)$$

where α_m has unit of cm-1, L is total cavity length (cm) and R is the power reflectivity.

The mirror loss are linked to the differential efficiency (W/A), by the following formula:

$$\eta_d = \eta_i \frac{\alpha_m}{\langle \alpha_i \rangle + \alpha_m}$$

where $\langle \alpha_i \rangle$ represents the average internal material loss (mainly caused by dopant impurity) and η_i is the injection efficiency. The differential efficiency is also used to express the output power of the LD as:

$$P_o = \eta_d \frac{hv}{q}(I - I_{th}) \qquad (I > I_{th})$$

where P_o is the LD output power (W), η_d the diffential efficiency *h* is the Planck constant, v the frequency, q the electron charge, I and I_{th} the input and threshold current respectively.

These basic parameters of LDs can be obtained by measuring multiple LDs of two different lengths (and same width or in the case of CA-LD design, same active region width), or a single device and apply the cut-back technique (essentially the LD cavity is etched back and LIV characteristics of the resulting shorter LD are measured).

By this way, the following expressions can be derived:

$$\langle \alpha_i \rangle = \frac{\eta_d' - \eta_d}{L\eta_d - L'\eta_d'} ln\left(\frac{1}{R}\right)$$

and

$$\eta_i = \eta_d \eta_d' \frac{L - L'}{L\eta_d - L'\eta_d'}$$

where $\langle \alpha_i \rangle$, η_d, η_i, L, and R, are the average material loss, differential efficiency, injection efficiency, cavity length and reflectivity of the device, respectively, and the prime indicates that these parameters refer to the cavity of different length.

In order to minimize the uncertainty, measurements of LDs of many different length are usually taken. The differential and injection efficiency are related through the following expression:

$$\frac{1}{\eta_d} = \frac{\langle \alpha_i \rangle}{\eta_i ln\left(\frac{1}{R}\right)} L + \frac{1}{\eta_i}$$

Thus the average material loss $\langle \alpha_i \rangle$ is obtained by slope while the inverse of the intercept gives the injection efficiency η_i.

The previous formulas indicate that LDs need to have high quality facets in order to obtain reliable measurements [3]. Unfortunately, LD facets obtained using the common etching techniques are hardly perfectly straight and smooth, moreover they also have a lower reflectivity (whose actual value is often unknown). This not only decreases the overall performance of the device but it can cause a variability from device to device, making the extraction of the LD internal parameters extremely hard to obtain [4].

Multiple dry etching Cl_2-based techniques such as reactive ion etching (RIE), electron cyclotron resonance etching (ECR), magnetron reactive ion etching (MIE), inductively coupled plasma etching (ICP), and chemically assisted ion beam etching (CAIBE) and various kinds of mask (from soft mask with different photoresists to hard mask such as SiO_x, SiN_y, SrF_2) having have been investigated to make good laser facets, however so far none of them have produced satisfactory LD facets. At UCSB, LD facets are usually made by RIE according to the fabrication process described in [5].

The main advantage of this technique is that both the front and back facets of an entire sample can be defined lithographically and etched at the same time. However facets

obtained in this way also present several drawbacks: SEM analysis has revealed striations along the facets surface and not straight facets: generally the angle is ~ 84 degree and it can be even worse if the facets are etched deeper as shown in the following image:

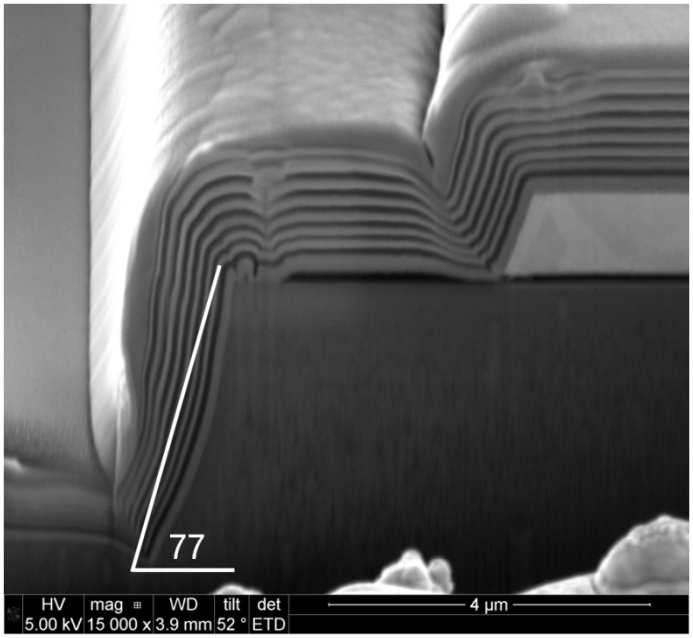

Figure 51 Example of tilted facet of a standard LD. The facet was coated with multiple layers of SiO_2 and TaO_2

Moreover, the facets are often not-parallel: thus the actual facets reflectivity will be different from what it had been designed and actually unknown.

Finally a relatively big part of the substrate remains in front of the device: this interacts with the laser beam and can affect the far field pattern.

Polishing is an alternative technique to produce higher quality facets and smoother facets have been reported by using this method [6]. In addition, it also offers the advantage of maximizing the light collected by the photodetector as this can be placed arbitrarily close to the device to be measured. However, it has the disadvantages of being a slow technique and also it offer a poor yield.

Improvement in the CA-LD fabrication process has led to better facet quality as shown in Fig. 53 (a). However, SEM analysis of facets of several samples have revealed that the yield of this straighter and smoother facets was very poor and in fact almost all of the CA-LD presented usually tilted and not parallel facets, which also had extremely rough and high corrugated surfaces as shown in Fig. 53 (b) and (c). This could be caused by the additional fabrication steps of the CA-LD, it is also possible that a long and wide air gap may play a role during the RIE facet etch.

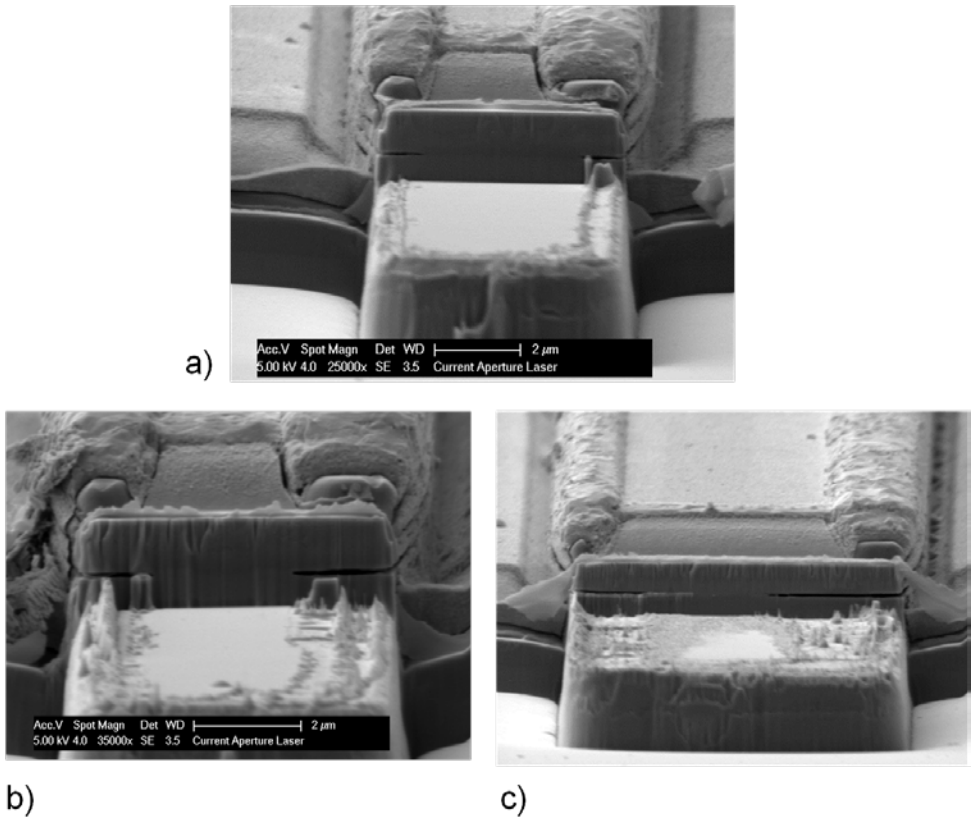

Figure 52 SEM images of RIE etched facet of CA-LD

In order to have better facets, a technique based on Focus Ion Beam (FIB) etch was developed to obtain straight, smooth and parallel facet as shown in Fig. 54.

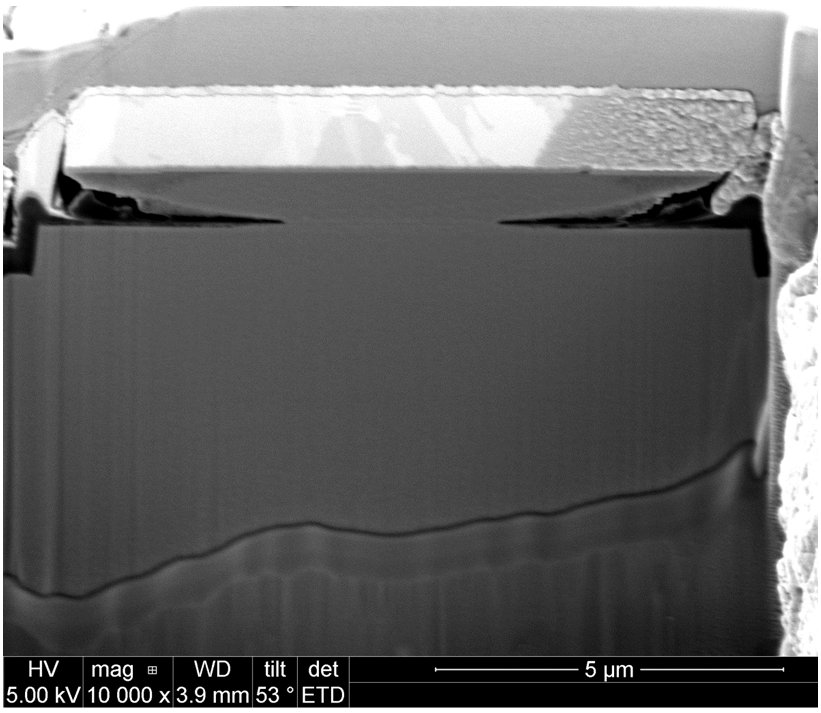

Figure 53 SEM image of a FIB etched facet of a CA-LD

Particular care was taken during the FIB etching in order not to damage the epitaxial structure and to avoid possible short circuit. The improvement in facets quality was checked by comparing the performance of facets of CA-LD obtained by FIB etch with facets obtained by RIE etch. The same device has been tested after the facets were obtained by FIB etch (Fig. 55). Although the device tested is relatively long (1500 mm), the improvement in output power, threshold voltage, threshold current density, more generally, in differntial efficiency is still apparent and an even bigger improvement can be expected for shorter length cavity, where mirror loss plays a more important role. Similar benefits to the performances of standard nitride LDs have also been reported in Ref. [7].

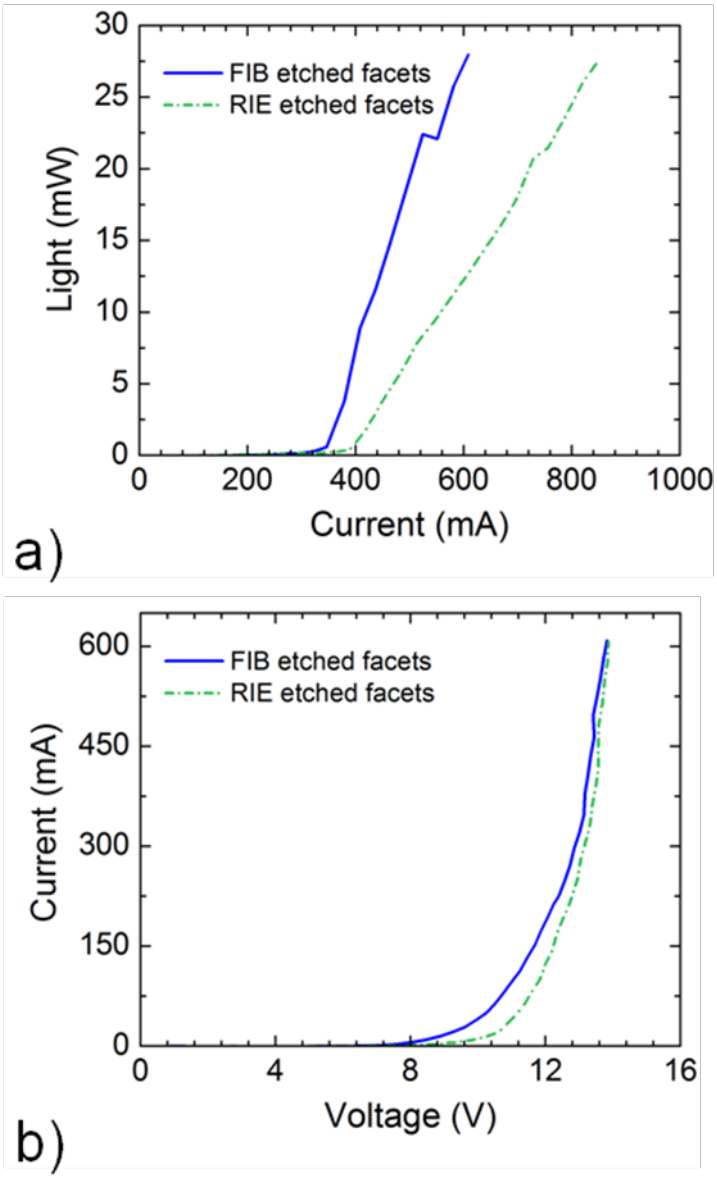

Figure 54 Comparison of (a) LI and (b) IV characteristics of CA-LD of a 1500 μm CA-LD with facets obtained initially by RIE etch (green dashed line) and then they have been FIB-ed (blue line).

4.2 *M*- plane results

CA-LDs and shallow etched ridge LDs were fabricated on *m*- plane. The growth conditions were mainly based on *m*- plane blue LD recipe developed on a different MOCVD reactor by K. Kelchner and described in Ref. [8].

The nominal epitaxial structure of this LD is summarized below:

Layer	Layer Thickness	Layer composition	Doping (cm^3)
n-side			
n-GaN	~ 1 um template	GaN	~ 2e18
InGaN n-waveguide	~ 100 nm	InGaN 0 -> 7 %	~ 5e17
Active region			
4X	6 nm	InGaN (~20%)	UID (~5e16)
	10 nm	GaN	UID (~5e16)
p-side			
EBL			
	~15 nm	AlGaN (~15%)	~1e19
InGaN p-waveguide	~ 100 nm	InGaN 7 -> 0 %	~ 5e17
p-GaN	800 nm	GaN	~1e18
p-GaN (p+)	~8 nm	GaN	~7e18
p-GaN (p++)	~8 nm	GaN	~3e19

Several LDs were fabricated following the CA-LD and the shallow etched fabrication process as described in Chapter 3.

The results presented below refer to LDs having similar active region width (~ 3um). The total *p*- layers width for the CA-LD was 10 um. The reference LD did not have an optimized epitaxial structure and J_{th} was in fact high ~ 14.5KA/cm^2. Although both the devices

manifested relatively poor performance, the CA-LD design has shown nevertheless some benefits: it had a lower J_{th} and in particular a lower series resistance (8.18 Ω for the shallow etch design and 4.81 Ω for the CA-LD) as shown in Fig. 56.

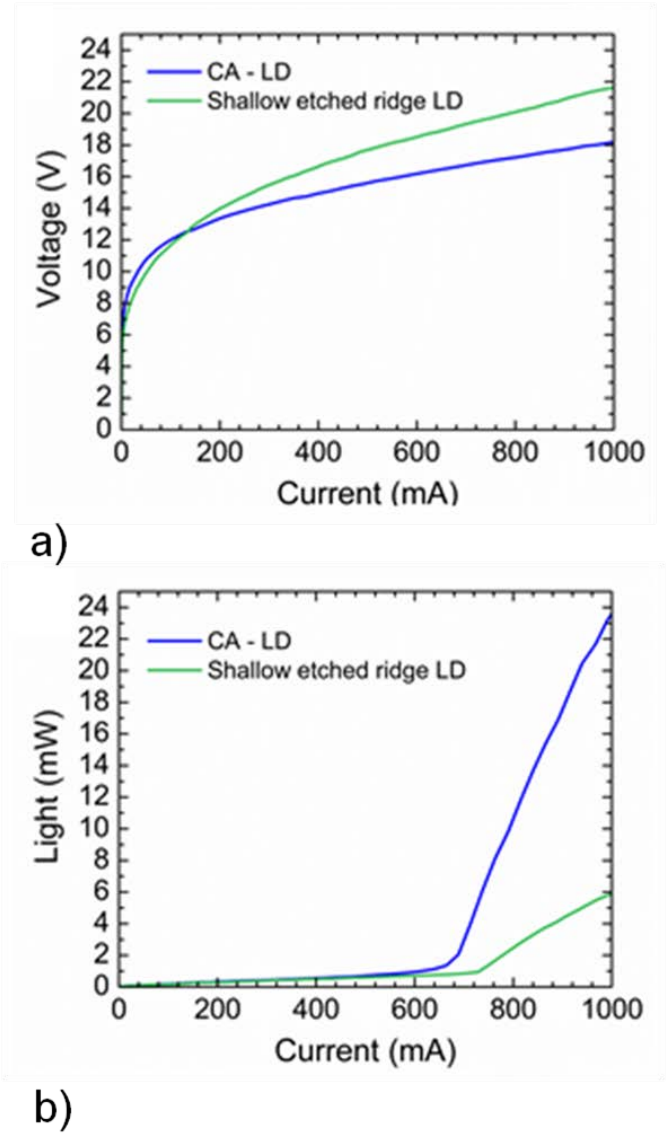

Figure 55 (a) IV and (b) LI characteristics of CA-LD and shallow etch LD having nominally the same epitaxial structure.

4.3 20-2-1 plane results

In this section, the results of CA-LDs grown on *20-2-1* plane are presented. The LD epitaxial structure has been mainly developed by A. Pourhashemi. As reported in Ref. [9], the approximate layers thickness, composition and doping along the growth direction are:

Layer	Layer thickness	Layer composition	Doping (cm3)
n-side			
n-GaN	1 um template	GaN	~1e18
InGaN n-waveguide	10 nm	InGaN from 0-5%	~5e17
	50 nm	InGaN from 5%	~5e17
	10 nm	InGaN from 5-0%	~5e17
Spacer	20 nm	GaN	UID (~5e16)
Active region			
4X	3.5 nm	InGaN (~20%)	UID (~5e16)
	6 nm	GaN	UID (~5e16)
Last barrier	6nm+15nm	GaN	UID (~5e16)
p-side			
Spacer	~10 nm	GaN	~1e19
EBL			
	~6 nm	AlGaN (~15%)	~1e19
	~6 nm	AlGaN (~15% - 0%)	~1e19
InGaN p-waveguide	10 nm	InGaN from 0-5%	~5e17
	50 nm	InGaN from 5%	~5e17
	10 nm	InGaN from 5-0%	~5e17
p-GaN	600 nm	GaN	~5e17
p-GaN (p+)	~8 nm	GaN	~5e18
p-GaN (p++)	~8 nm	GaN	~2e19

Also in this case, a LD wafer was cleaved into two pieces for simultaneous processing in order to assess the performance of the CA-LDs design with respect to the shallow etch design.

The first piece was used to fabricate a shallow etched ridge. The etch depth for the shallow etched ridge LD was ~420nm, i.e. a remnant p-side thickness of ~220 nm, while the second piece was used to fabricate CA-LDs as described in Chapter 3. Differently from the m- plane LDs, in this case a thin ITO layer (~100 nm) was added on top of the p-GaN to improve the performance of the device.

The schematics of the two structures is shown in Fig. 57

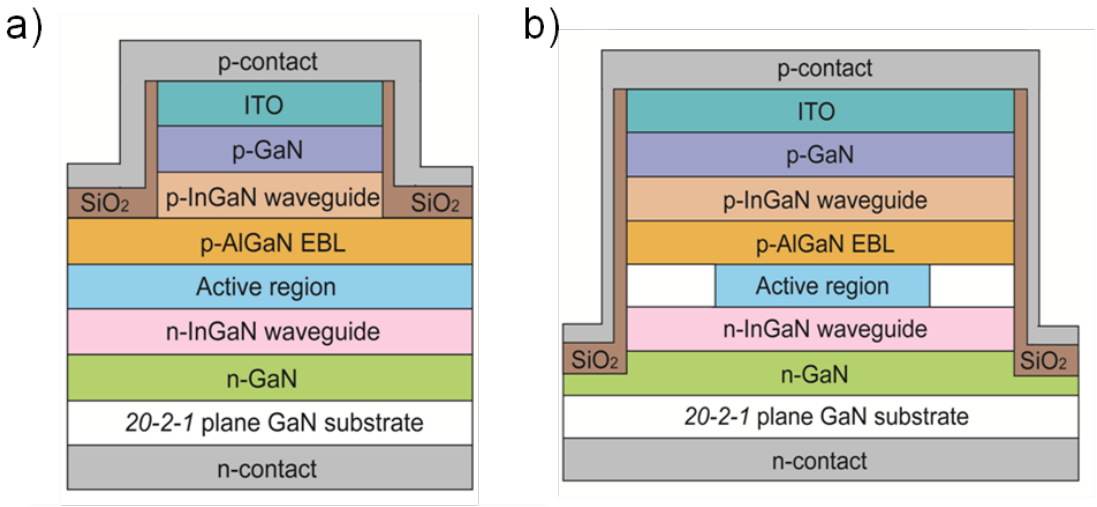

Figure 56 Schematics of (a) shallow ridge waveguide LD and (b) the CA-LD.

Both devices were tested by on-wafer probing under pulsed conditions with a pulse width of 500 ns and a repetition rate of 1 kHz, corresponding to a duty cycle of 0.05%. The optical output power was measured at room temperature (~22.5 °C) from the front mirror facets using a calibrated broad area Si photodetector [10].

Figure 58 (a) shows the current-voltage (*I-V*) characteristics of an 1800 μm stripe length CA-LD and a shallow etched ridge LD. The CA-LD has a p-GaN ridge width of 8 μm with an active region width of ~2.5 μm after the PEC etch step, while the shallow etched ridge LD has both a p-GaN ridge width and an active region width of 2.5 μm.

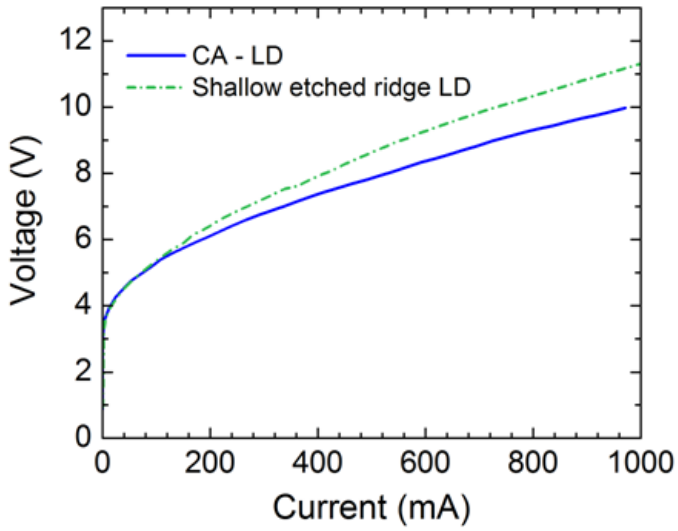

Figure 57 IV characteristics of shallow etch LD (dashed green lined) and CA-LD. The cavity length is 1800 μm and the active region width is 2.5 μm for both the LD. The CA-LD has p- layer of 8 μm width.

As shown in Fig. 58 the series resistance of the CA-LD was lower than that of the shallow etched ridge LD (4.7 and 6.0 Ω respectively), as would be expected for a device with a wider p-GaN ridge and a greater area for forming a p-contact. Figure 59 compares the light-current (*L-I*) characteristics of the two LDs.

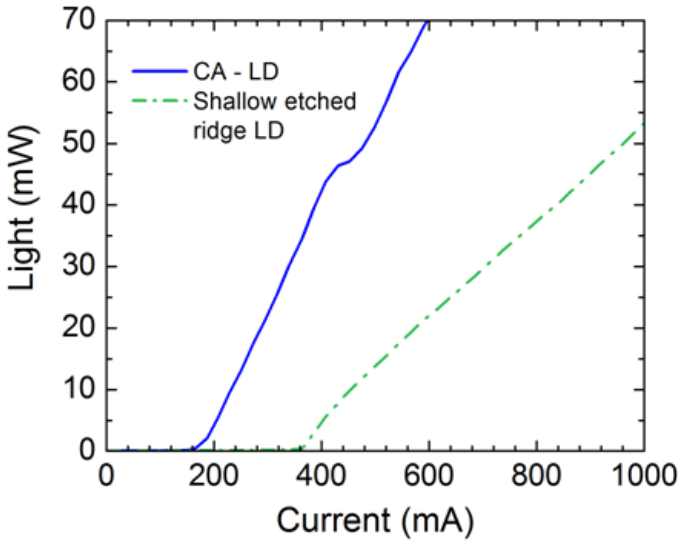

Figure 58 LI characteristics of shallow etch LD (dashed green lined) and CA-LD. The cavity length is 1800 mm and the active region width is 2.5 mm for both the LD. The CA-LD has p- layer of 8 μm width.

The threshold currents (threshold current densities) were 193.2 mA (4.4 kA/cm^2) and 363.4 mA (8.1 kA/cm^2) for the CA-LD and shallow etched ridge LD, respectively. This corresponds to threshold voltages of 6.1 V and 7.6 V for the CA-LD and the shallow etched ridge LD, respectively. The slope efficiencies were 0.13 W/A and 0.07 W/A for this particular CA-LD and the shallow etched ridge LD, respectively. The dependence of the threshold current on temperature was also measured under pulsed operation at 0.03% duty cycle to avoid the effects of self-heating. The change of the threshold current and lasing wavelength was recorded upon a temperature change in the range of 20 – 80 °C. The temperature increase leads to enhancement of Auger recombination, carrier leakage over the heterobarriers and intervalence band absorption effect which tend to increases the threshold current and red-shift the lasing wavelength.

Using the expression: $I_{th} = I_0 e^{T/T_0}$ a characteristic temperature T_o of ~ 126 K and a shift in wavelength of ~0.05 nm/K have been estimated as shown in Fig. 60

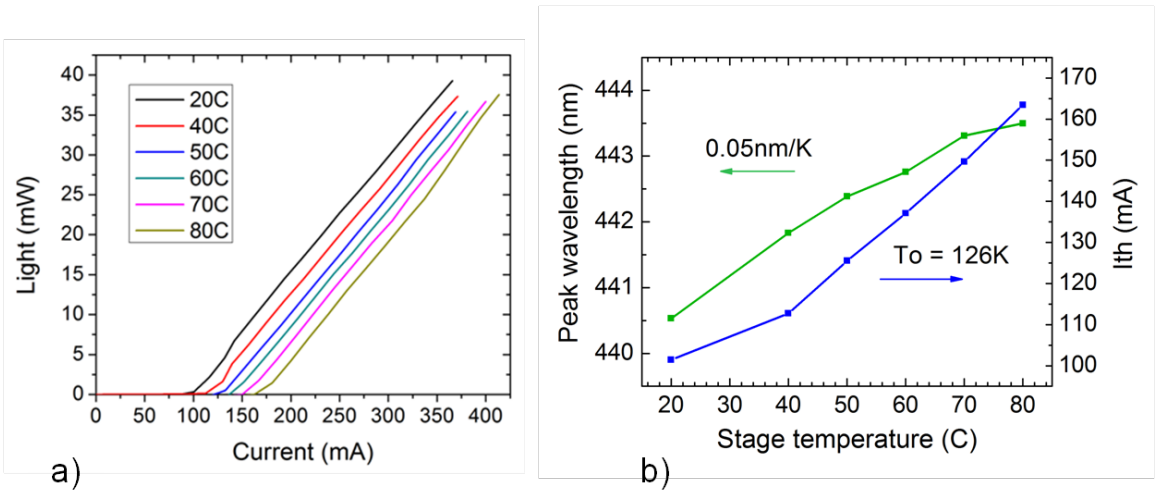

Figure 59 a) shift in threshold current and b) in the emission wavelength with increasing the stage the temperature

By sequentially trimming the cavity length of an initially 1800 μm long CA-LD by focused ion beam (FIB) etching, the main LD parameters have been extracted. Fig. 61 shows the different steps of this procedure.

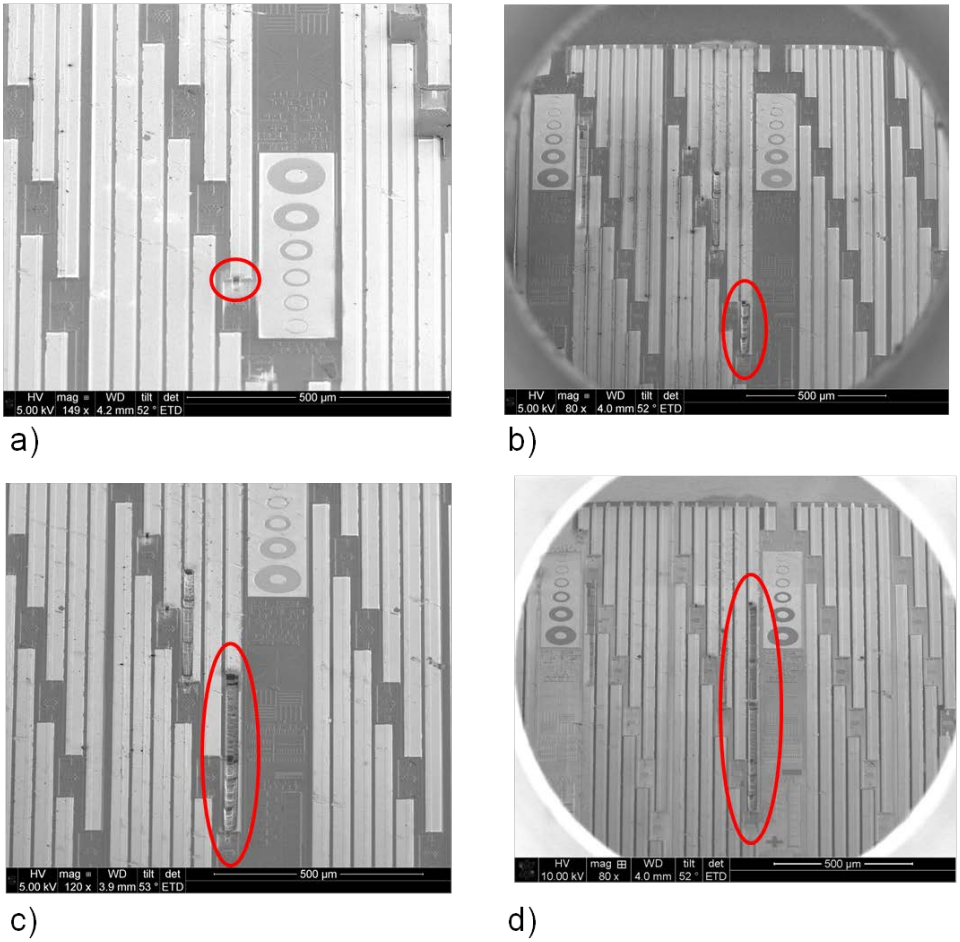

Figure 60 sequentially trimming the cavity length of an initially 1800 [illegible] LD by focused ion beam (FIB) etching.

Assuming that the facet reflectivity R was that of a perfectly-flat vertical facet (~ 20%) and that η_d, η_i and the gain-current relation do not change with FIB polishing, and using the expressions reported in Section 4.1, an injection efficiency of ~ 65% and loss in the order of ~ 100 cm^{-1} were estimated as illustrated in Fig. 62. The injection efficiency value is comparable to that reported in Ref. 11 for an *m*- plane LD and in Ref. 12 for *c*-plane LD.

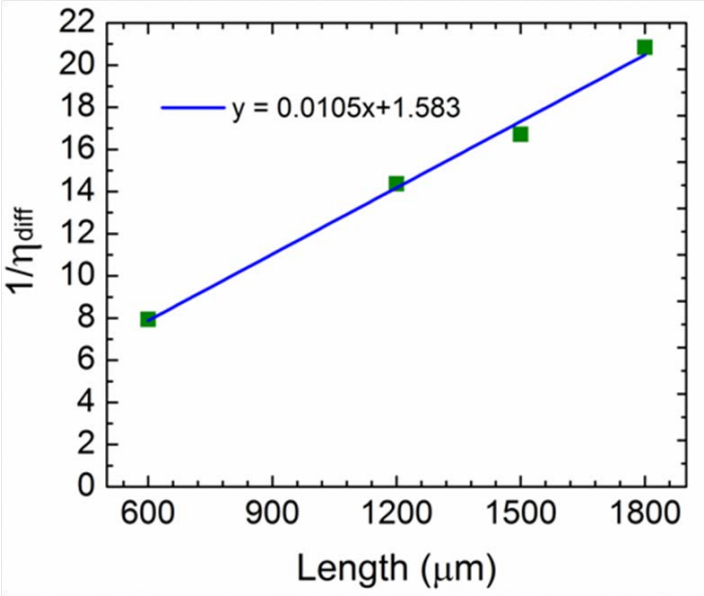

Figure 61 plot of $1/\eta_{diff}$ vs length of a CA-LD whose cavity length was cut-back by Focus Ion beam (FIB).

Such high loss includes both materials loss (estimated to be ~25 cm^{-1} and mainly caused by dopants impurities in particular Mg), free carriers absorption and roughness-induced optical scattering of the remnant PEC etched active region. The quantitative estimation of this last kind of loss is detailed in Chapter 5. Finally, current crowding and current leakage through unetched nanopillars as shown in Fig. 63, and whose possible origin is discussed in Chapter 2, may also contribute to lower the differential efficiency as suggested by preliminary conductive AFM (C-AFM) measurements. This current leakage seems to be very low, however a more in depth analysis is required.

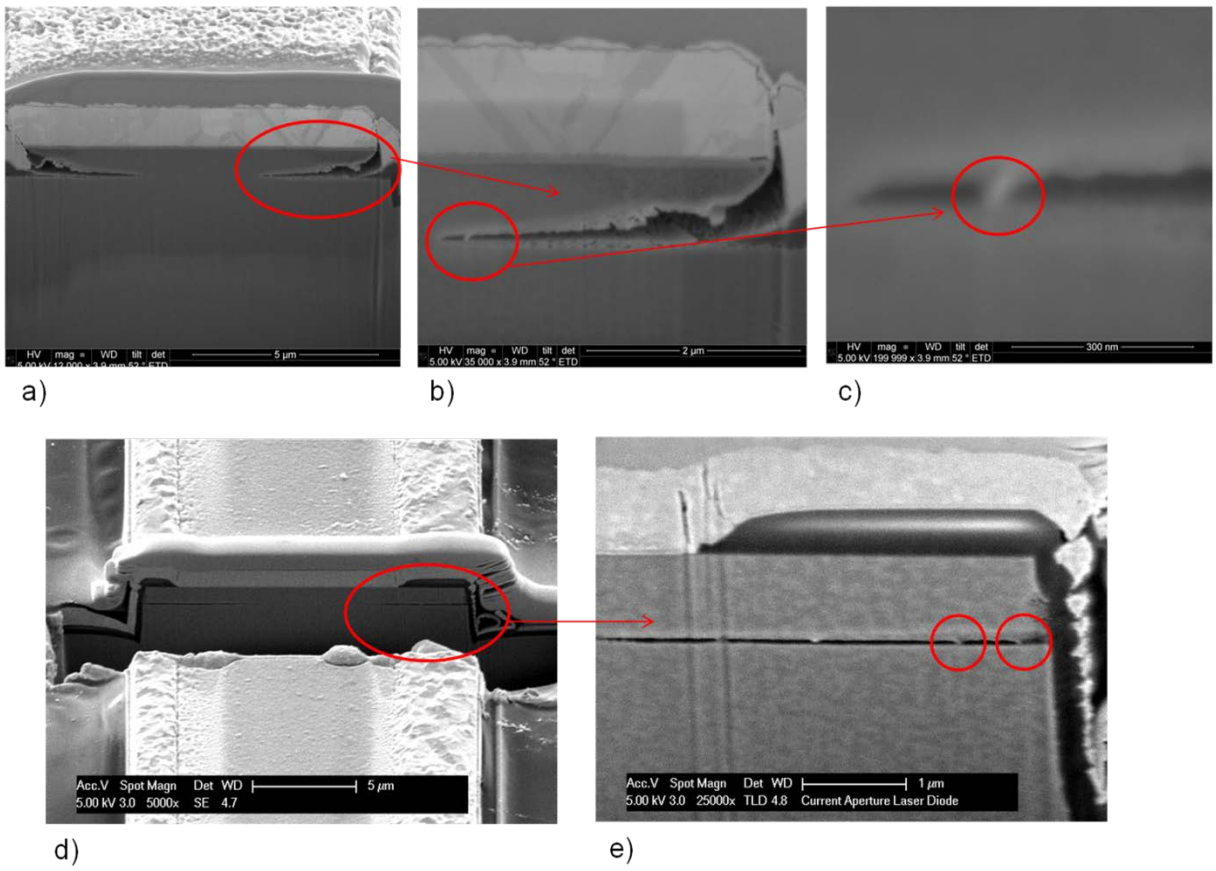

Figure 62 Nanopillars caused by imcomplete PEC etch into the aperture.

Finally, some devices were also tested under CW operation. Figure 6 shows the results of CW operation of a CA-LD with a 1.5 µm active region width below a 4.5µm wide p-contact, after the back facet of this set of devices was coated for high reflectivity (HR) using four periods of alternating quarter-wavelength layers of SiO_2 and Ta_2O_5, and the bar of lasers was soldered to a copper heat spreader. A CW threshold current density as low as 3.6 kA/cm^2 was measured at 5.9 V.

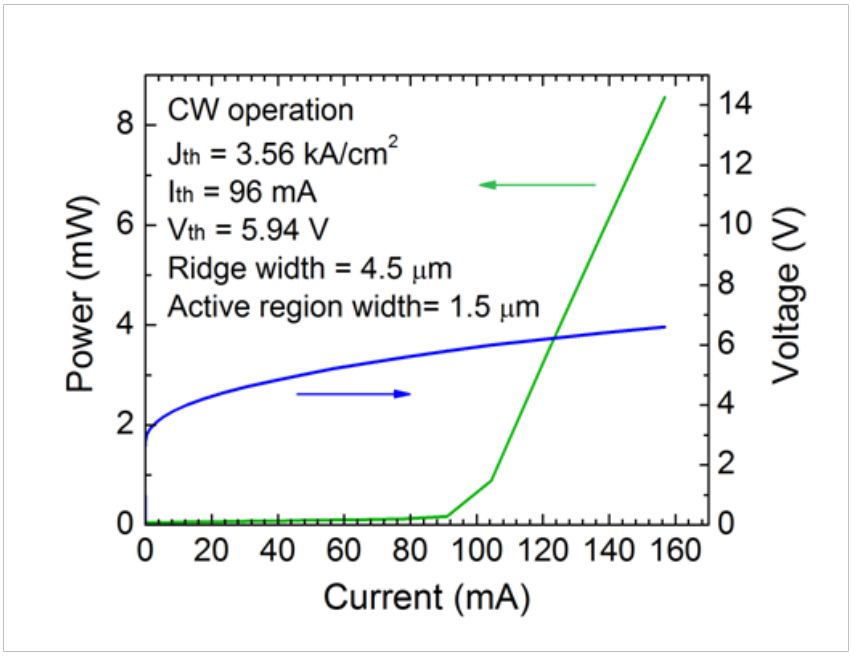

Figure 63 L-I-V characteristics of an 1800 μm long and 4.5 μm wide CA-LD with an approximately 1.5 μm wide active region after PEC etching under CW operation.

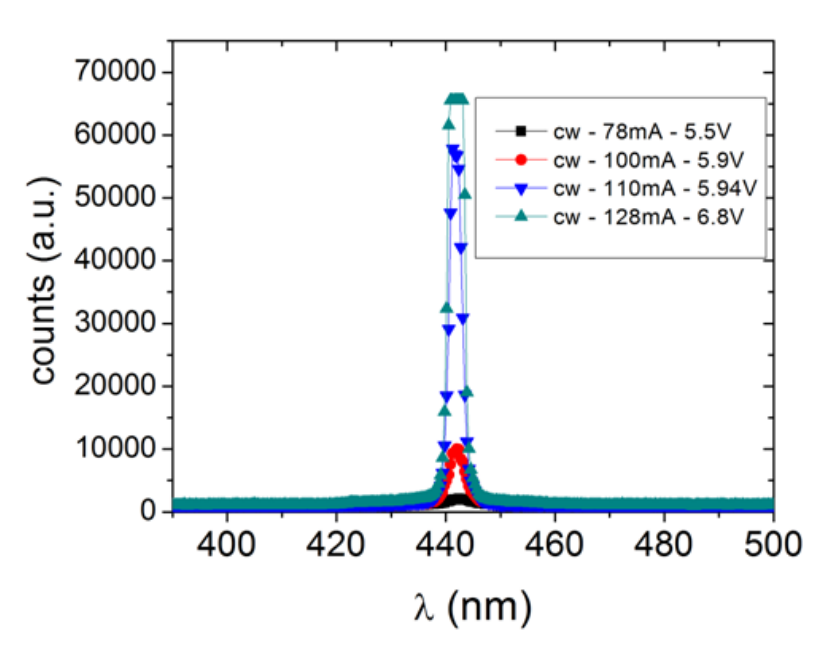

Figure 64 emission spectrum at different injection current showing lasing operation at 442nm

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". . . In that Empire, the Art of Cartography attained such Perfection that the map of a single Province occupied the entirety of a City, and the map of the Empire, the entirety of a Province. In time, those Unconscionable Maps no longer satisfied, and the Cartographers Guilds struck a Map of the Empire whose size was that of the Empire, and which coincided point for point with it. The following Generations, who were not so fond of the Study of Cartography as their Forebears had been, saw that that vast map was Useless, and not without some Pitilessness was it, that they delivered it up to the Inclemencies of Sun and Winters. In the Deserts of the West, still today, there are Tattered Ruins of that Map, inhabited by Animals and Beggars; in all the Land there is no other Relic of the Disciplines of Geography."

On Exactitude in Science, Jorge Luis Borges

Chapter 5

Estimation of roughness-induced scattering losses

5.1 Introduction

One of the main advantage of the CA-LD design is to constrict the current to flow to the center of the lasing mode by laterally and controllably etching the active region.

This offers the advantages of improving the performance of optoelectronic [1] and electronic [2] devices by eliminating current leakage pathways and reducing the attendant dc-rf dispersion, as described in the previous chapters and confirmed by several theoretical and experimental analysis.

In chapter 3 it was described how selective wet etching of the InGaAsP active layer has been used to undercut the active region of InP-based devices and achieve low-threshold and high-speed devices [3-6]. In chapter 2 it was shown that the Photoelectrochemical (PEC) etching can bring similar results in nitride-based LDs [7]. Under appropriate conditions PEC etching allows for a controllable undercut in the lateral direction and being a wet etching technique it does not produce the typical sub-surface damage to the epitaxial structure which dry etching techniques cause. Differently from wet etching, dry etching can also induce high surface roughness, which is generally correlated to corrugations of the photoresist profile and to the etch rate [8], between the waveguide core and the outer cladding. This is undesirable in optoelectronics devices, especially in the case of high-index-contrast (HIC) waveguides employed in densely integrated photonics devices [9].

Although the CA-LD shown in Chapter 4 run in CW operation, it manifested a relatively low differential efficiency which is reflected in the high loss shown in Fig. (however it is also possible the reflection of the light caused by the presence of a relatively long piece of the substrate in front of the facet – had decreased the light collection of the photodetector).

This has pushed to investigate the influence of the roughness along the light propagation direction in PEC etched structure. Fluorescent images have indeed shown that PEC etched structures can have a wide range of roughness as shown in Fig. 66.

This chapter presents an estimation of the scattering modal losses caused by the PEC etch-induced roughness of the active region of the nitride-based CA-LD whose results have been presented in Chapter 4 and it is explained why filling the aperture as described in Chapter 3 can help mitigating these scattering losses and therefore improve the differential efficiency of the final device.

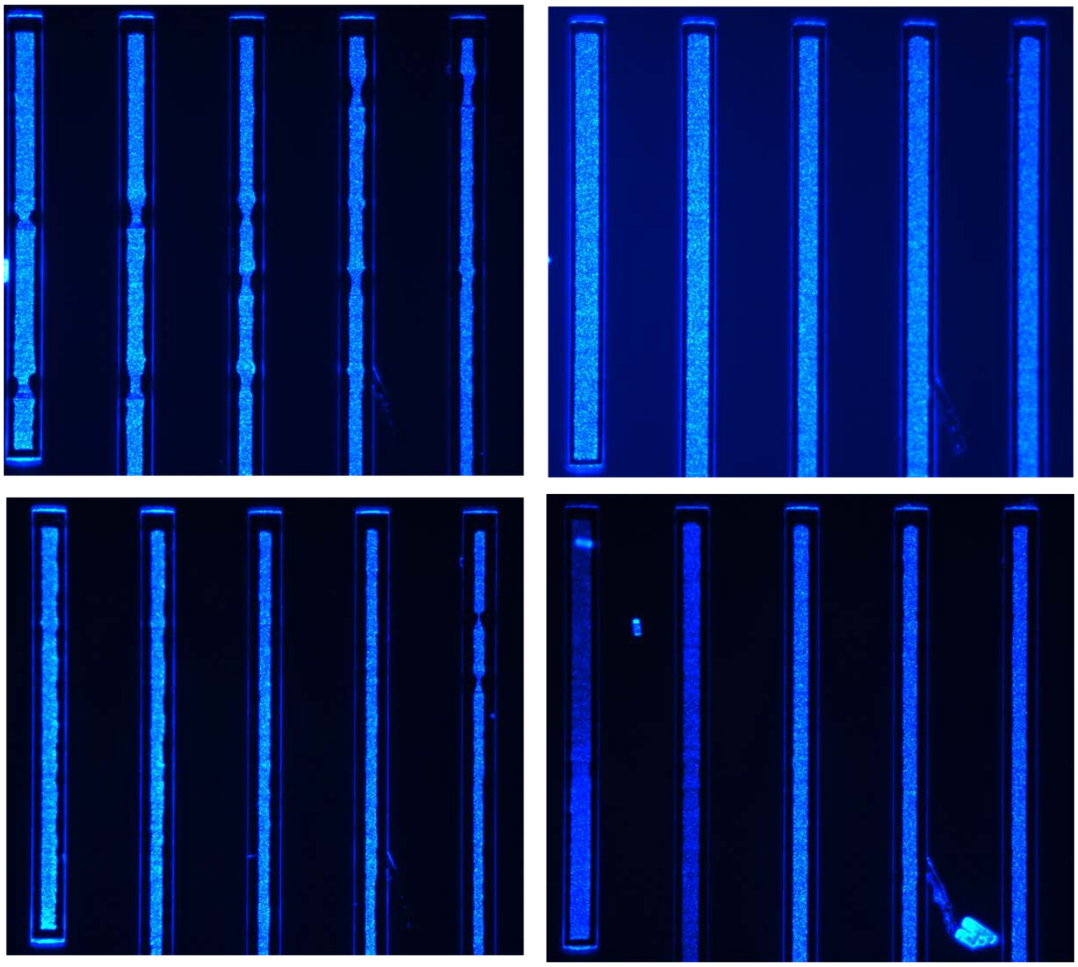


Figure 65 Fluorescent images of PEC etched LDs showing different line edge roughness

5.1 Modeling of roughness-induced scattering loss

Scattering losses are caused by the forward- and back- scattered radiated power of the guided optical mode, whose shape changes continuously along the light propagation

direction because of the continuous change of the beta of the optical mode, $\beta = k_0 \cdot n_{eff}$ due to the sidewall roughness. In the case of LDs, this causes optical scattering loss which can lead to laser mode instability and causes a decrease of the differential efficiency and an increase in the threshold current density of the final device [10] as these depend on the sidewalls roughness according to the following expressions:

- Slope efficiency:

$$\eta_d(\sigma_{rough}) = \frac{1}{q}\frac{hc}{\lambda}\eta_i \frac{\Gamma \cdot \alpha_m}{\alpha_m + \alpha_W + \alpha_{scatt}(\sigma_{rough})}$$

- Threshold current density:

$$J_{th}(\sigma_{rough}) = \frac{\alpha_m + \alpha_W + \alpha_{scatt}(\sigma_{rough})}{g\Gamma}$$

where $\alpha_m + \alpha_W + \alpha_{scatt}(\sigma_{rough})$ are the mirror, material and roughness-induced loss, h is the Planck constant, c the speed of light, q the electron charge, λ the emitted light wavelength, η_i the injection efficiency, g the gain and Γ the confinement factor.

The impact of such losses can be particularly high for short wavelength, low aspect ratio and narrow waveguides because of the stronger overlap of the optical mode with rough waveguide sidewalls. This has been described by theoretical scattering loss models [11,12] and experimentally verified [13-15].

Roughness can occur in any direction of the etched waveguide and it is distinguished in line edge roughness, LER (or line width roughness, LWR), surface wall roughness, SWR, and planar field roughness, PFR, as sketched in Fig. 67.

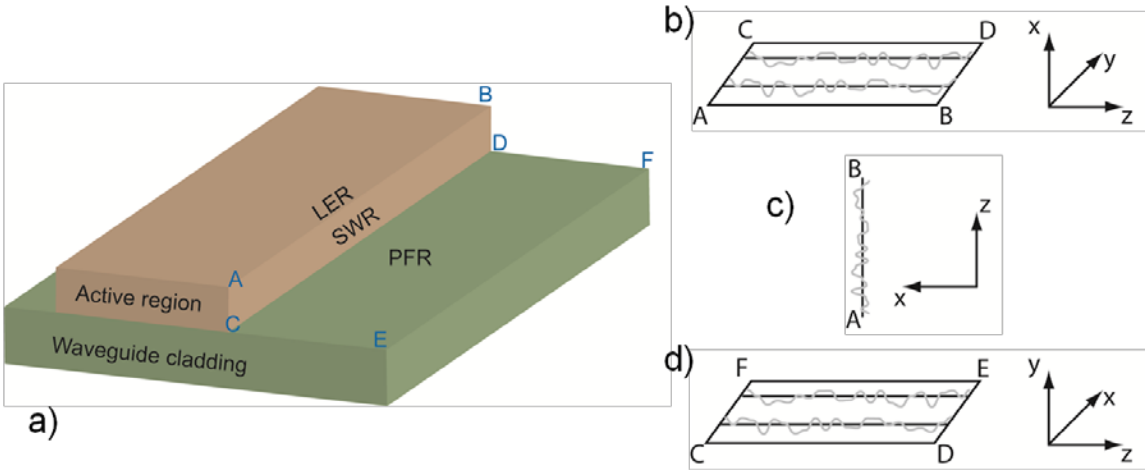


Figure 66 a) Schematic of different kinds of roughness: b) sidewall roughness (SWR), c) Line edge roughness (LER), d) Plane field roughness (PFR).

Usually only line edge roughness (LER) is assumed and all the roughness-induced optical scattering analysis presented in this work will be based on it. LER is modeled as a zero-mean real function $f(z)$: Fig. 68 depicts the case for the CA-LD where the active region represents the core of the waveguide and the PEC etched aperture regions represent the cladding.

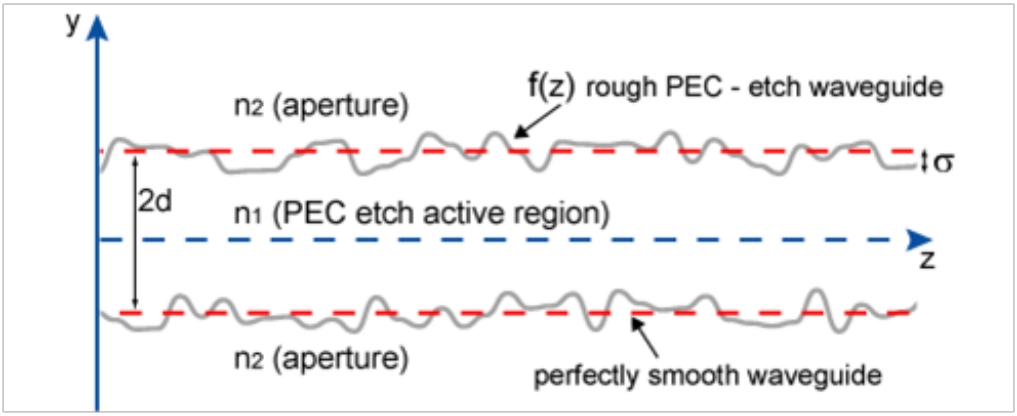


Figure 67 Schematics of LER in the CA_LD

According to the Volume Current Method (VCM) [16], a rough waveguide is modeled as a perfectly smooth and straight waveguide, which does not contribute to the far field radiation, whose contour is wavy and assumed to occur only in one dimension as depicted in Fig. 69

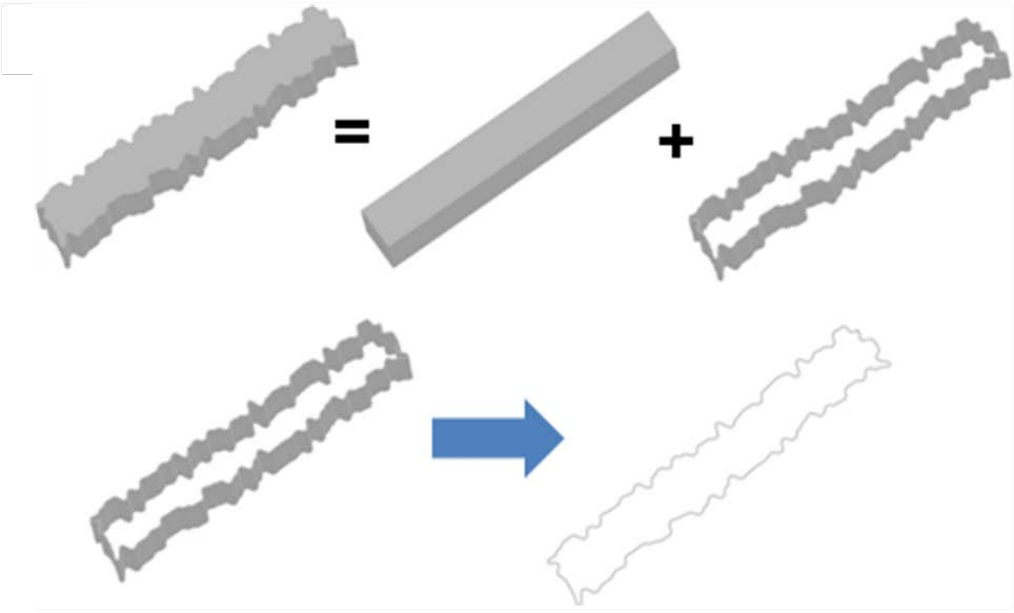


Figure 68 Schematics of the rough waveguide modeling

The wavy 1D contour is associated to a polarization current distribution $\vec{J}(\vec{r})$ which represents the refractive index inhomogeneity at the rough edges [17]:

$$\vec{J}(\vec{r}) = -i\frac{2\pi}{\lambda}\varepsilon_0 \cdot \Delta n_{eff}(x) \cdot \vec{E}_{pol}(x,y)\ \delta(y)\delta(z)$$

where λ is the light propagating wavelength, i is imaginary unit, ε_0 is the vacuum permittivity, δ is the Dirac delta function, $\vec{E}_{pol}(x,y)$ is the electric field, and $\Delta n_{eff}(x)$ is difference between the square of core and cladding effective refractive index. $\vec{E}_{pol}(x,y)$ is assumed to be very similar to that of the perfectly smooth and straight waveguide, and it contains the information on the TE (or TM) polarization of the waveguide. In the CA-LD design, this translates to the difference between the effective refractive index of the unetched active region and the PEC etched aperture region, respectively:

$$\Delta n_{eff}(x) = n^2_{eff,unetched} - n^2_{eff,aperture}(x)$$

Typically $\Delta n_{eff}(x)$ is a step function but, in general, the index profile can be distributed [18], in CA-LD design it can take into account the tapered shape of the aperture, which is related to the different polarization fields of the crystal planes as shown in Fig. 70.

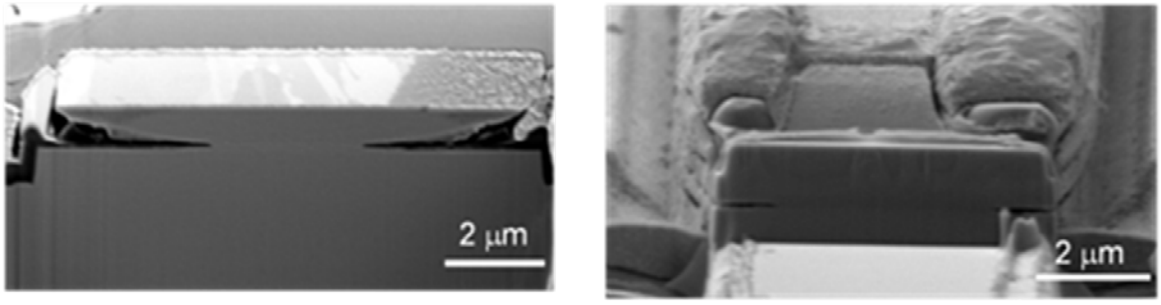


Figure 69 CA-LD fabricated on 20-2-1 and 10-11 (*m*- plane)

In order to apply the VCM to the CA-LD design, it is necessary to decompose the structure in three layers [19] and to estimate the effective refractive index of both the PEC etched and the unetched regions.

Using FIMMWAVE [20], a CA-LD having a width of 4.8 μm and an active region 1.15 μm wide and made of 4 MQW (3.5 nm QW and 6 nm barrier, the first barrier is 21 nm thick) was modeled.

The calculated confinement factor is ~ 4%. The effective refractive index of the slice containing the aperture can be estimated to the first order as:

$$n_{eff,aperture} \approx \Gamma_{aperture} \cdot n_{air} + \left(1 - \Gamma_{aperture}\right) \cdot n_{eff,unetched} \quad (3)$$

where Γ is the optical mode confinement factor, $n_{eff,unetched}$ and n_{air} are the refractive index of the un-etched region and air, respectively. As a result, a CA-LD can be considered similar to a deeply etched ridge LD placed in an environment of refractive index equal to 2.406 as shown in Fig. 71. The two structures have the same beta, whereas the difference in the confinement factor is 0.1%. The step effective index between the unetched and PEC-etched region is estimated to be $\Delta n_{eff}(x) \approx 0.074$.

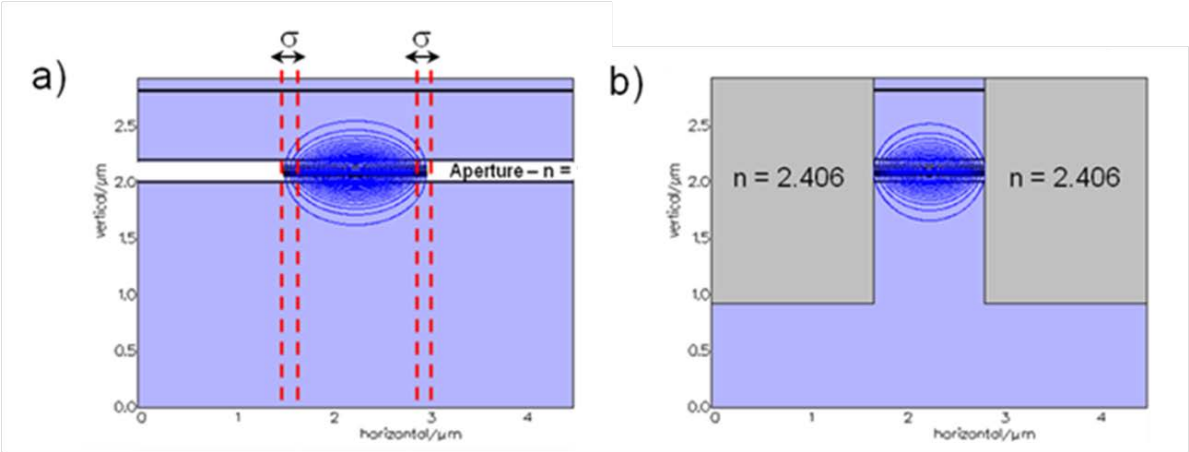


Figure 70 Simulation of the electric field intensity for (a) the CA-LD and (b) deep etched ridge LD.

The far field radiation pattern in 3D can be obtained as the product of a finite height radiating element whose height corresponds to the PEC-etched MQW thickness and an array factor representing its distribution along the waveguide. In this way, both the finite dimensions and the polarization of the actual waveguide are taken into account and a more precise estimation of the scattering losses can be obtained compared to the 2D models [18-20]. These models are essentially all based on the roughness-induced loss expression derived by Payne-Lacey [21] from the work of Snyder and Love. The scattering loss coefficient α from a single side rough edge of a planar waveguide as represented in Fig. 68 is computed as:

$$\alpha_{scat} = \varphi(d)(n_1^2 - n_2^2)\frac{k^3}{8\pi n_c}\int_0^{\pi} \tilde{R}\big(\beta - n_{cl}k_0 cos(\theta)\big)d\theta$$

where $\varphi(d)$ is the modal field evaluated at the waveguide surface, n_1 and n_2 are the core and cladding refractive index, $k_0 = 2\pi/\lambda$ is free space wavenumber, $\beta = k_0 \cdot n_{eff}$ is the guided modal propagation constant with n_{eff} being the effective index of the full structure, and *R* is the edge roughness spectral density function. This model properly applies to 2D slab

waveguides, however it has been used also for 3D case by applying the effective refractive index technique [13,22] eventually with a correction factor [23]. However this procedure has two main drawbacks:

a) it overestimates – up to two orders of magnitude – the scattering loss from etched sidewalls of a ridge waveguide (and therefore the use of correction factors have been proposed to fit the measured loss). Indeed this model does not fully take into account the finite height of the ridge and therefore the finite height of the radiating element.

b) it does not take into account the polarization of the propagating optical field. This has actually to be considered since the roughness is modeled as an antenna which radiates power away from the guided optical mode and the TE polarization scatters differently from the TM polarization.

In the 3D method based on Volume Current Method (VCM) proposed by Barwicz and Haus to compute the roughness-induced scattering loss, the radiated power per unit of length is proportional to the product of the Poynting vector of the polarization current source produced by the refractive index inhomogeneity along the light propagation direction, the line edge roughness power spectral density function (PSD), which is related to the autocorrelation function (ACF) by the Wiener-Khintchine theorem [24] and the difference in effective refractive indices the core-cladding squared $\Delta n_{eff}^2(x)$ and inversely proportional to the emission wavelength of the device. More specifically, the radiated power per unit length can be calculated using spherical coordinates as:

$$\frac{P_{rad}}{L} = \int_0^{2\pi} \int_0^{\pi} \tilde{R}(\beta - n_{cl} k_0 \cdot \hat{r} \cdot \hat{z}) \left(\vec{S} \cdot \hat{r}\right) r^2 sin\theta \; d\theta d\varphi$$

where $\tilde{R}$ is the LER power spectral density function (PSD), n_{clad} is cladding refractive index, β is the guided modal propagation constant, $k_0 = 2\pi/\lambda$ is free space wavenumber, and $\left(\vec{S} \cdot \hat{r}\right)$ is the Poynting vector due to the polarization current source produced by the refractive index inhomogeneity along the light propagation direction, as defined above. As from the Wiener-Khintchine theorem, the LER PSD function is computed by taking the Fourier transform of the autocorrelation function (ACF):

$$\tilde{R}(\Omega) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} R(u) \exp(i\Omega u) \mathrm{d}u$$

The autocorrelation is the cross-correlation of a signal with itself at different points in space or time and it measures the similarity between observations as a function of the space or the time lag between them. In particular it is used to define the correlation length L_c of the rough sidewalls which is obtained by computing the point where the autocorrelation function $\mathcal{R}_x(z)$ of the edge roughness $f(z)$ is defined as decays to e^{-1} of its maximum:

$$\mathcal{R}_x(L_c) = e^{-1} \cdot \int_{-\infty}^{\infty} x(z) \cdot x(z + \delta) dz$$

Roughness values of the PEC etched active region edges were obtained by analysis of fluorescence optical microscope images. Optical fluorescent images of a PEC etched LD are converted to grayscale and then black-and-white using Otsu's method [26]. An edge detection algorithm was then applied to extract the rough edge from the boundary of the

largest connected component of the black-and-white image. The results are shown in Fig. 71. Although optical microscope images can provide very large data sets, which are necessary to have a good estimation of the parameters to be measured, they suffer from low resolution in analyzing very small features. More precise measurements of the remnant PEC etched active region edges features have been obtained by high resolution AFM and SEM images analysis (a pixel on the SEM image corresponds to ~3 nm, the SEM resolution is ~1.2 nm) after removing the p-layers using a FEI Helios 600 dual focus ion beam (FIB).[1]

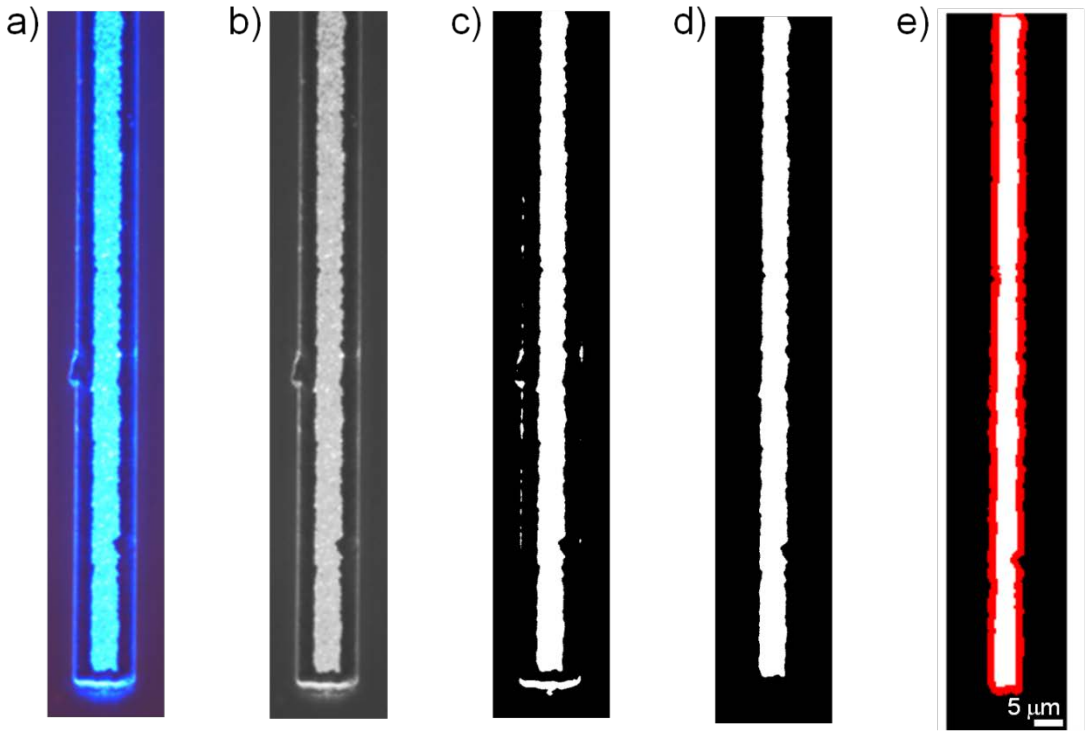


Figure 71 Extraction of rough edge of the remaining PEC etched LD from a fluorescent optical image using the Otsu method.

In order to reduce scalloping caused by the physical sputtering of the FIB and to avoid additional damage, the cuts were performed in multiple steps with the ion beam operating in rastering mode at 30 KeV, and the beam current was varied from 0.46 nA down

to 28pA. The SEM images were recorded at 0.34 and 0.69 nA electron beam currents to increase the contrast of the rough edge to the background grey, using dwell times of 3 μs and 10 μs to enhance the signal-to-noise ratio and avoid distortion. By carefully monitoring the ion milling through the different layers of the structures, the cut was stopped exactly on top of the remnant PEC-etched active region as shown in Fig. 73.

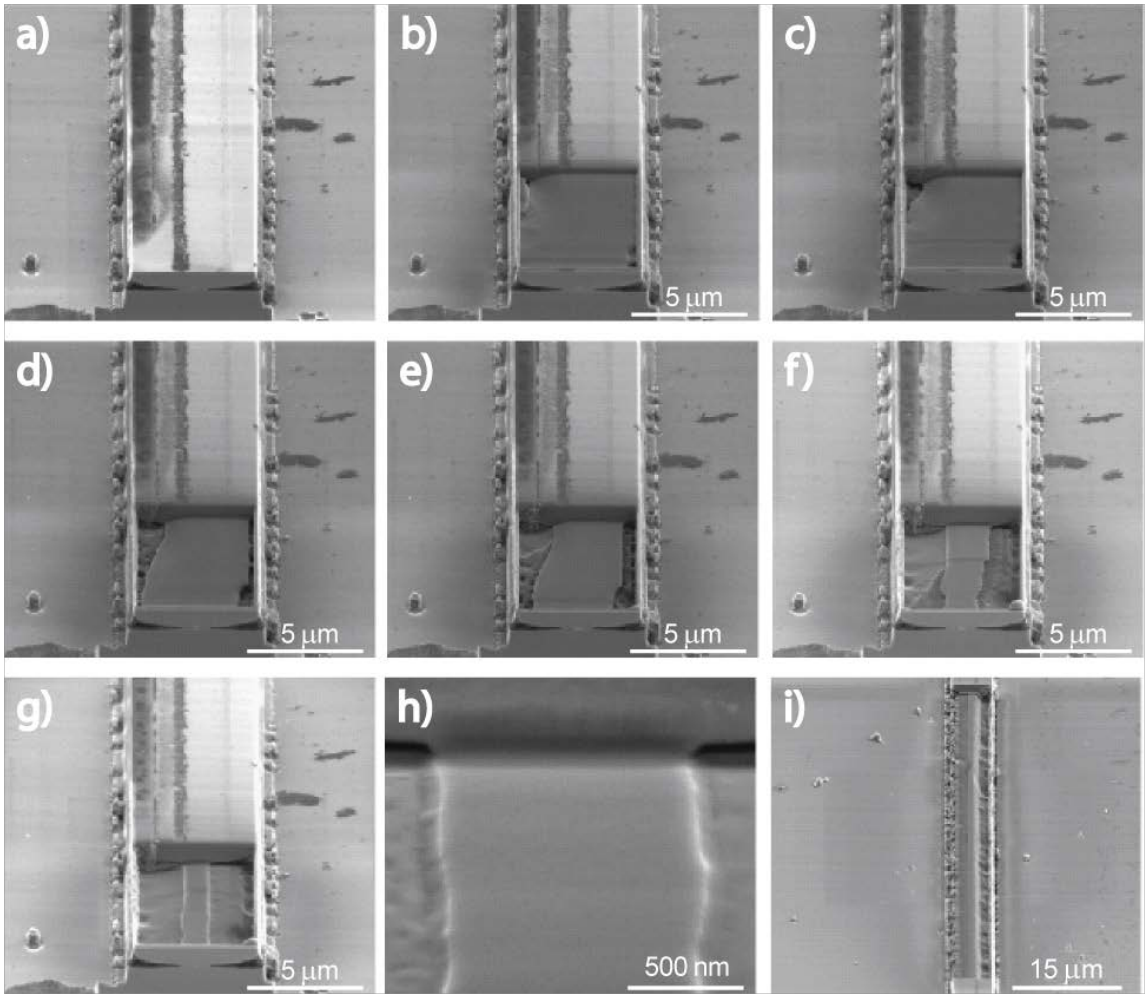
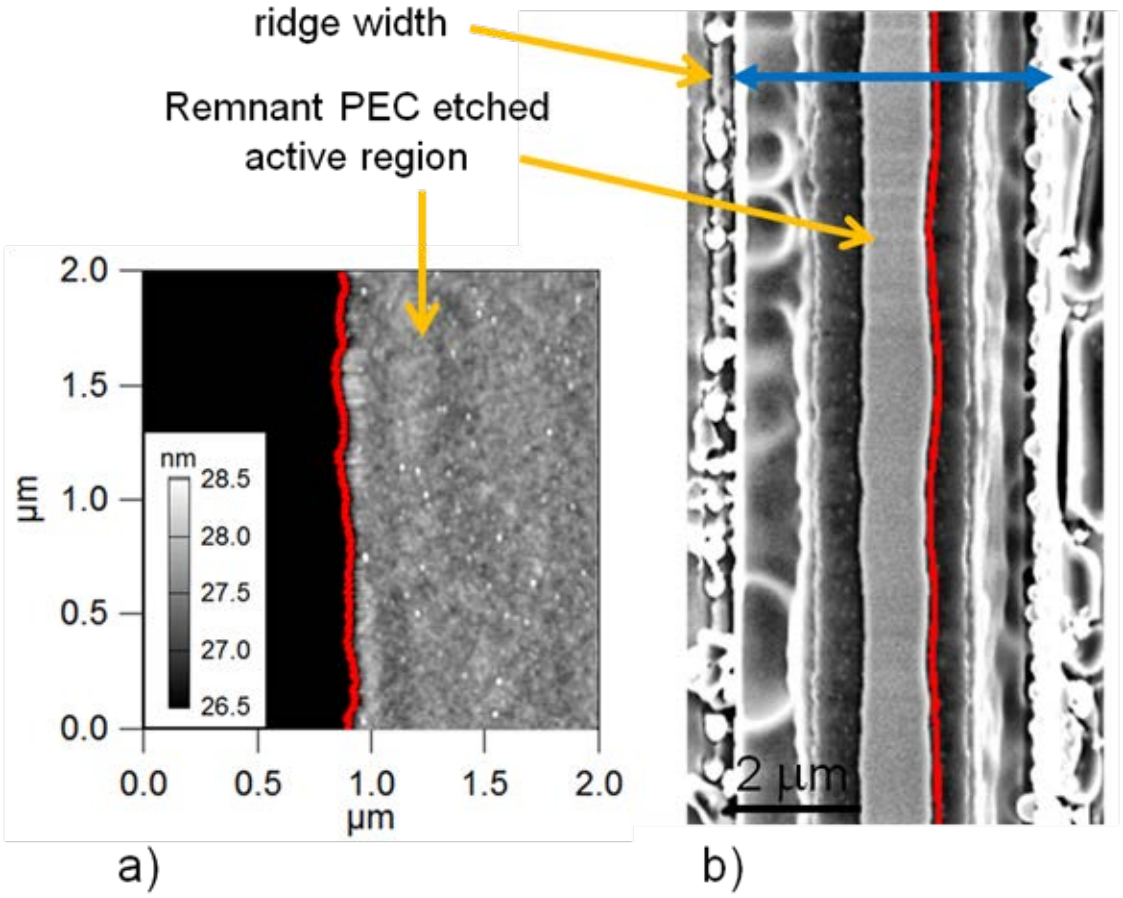


Figure 72 FIB cuts of the p-epilayers of a CA-LD exposing the remnant PEC etched active region.

Statistical analysis was performed on the rough edges after extracting them by using a modified hidden Markov model (HMM)-based algorithm. The trellis was created by

initializing a roughly estimated vertical line, constructing normal lines at each pixel along this line, and symmetrically sampling points on each normal. Observation probabilities of the HMM were designed to favor sharp edges and transition probabilities to ensure a smooth-connected edge. Dynamic programming was applied to estimate the HMM state sequence having maximum a-posteriori probability, and hence, the optimal edge position [25]. Some results of these images processing are shown in Fig. 74 (b) – (h). A similar procedure has been applied to AFM scan images (Fig. 74 (a)). The roughness data obtained from the SEM images are on the same order of magnitude of those obtained by AFM images on a smaller scan.



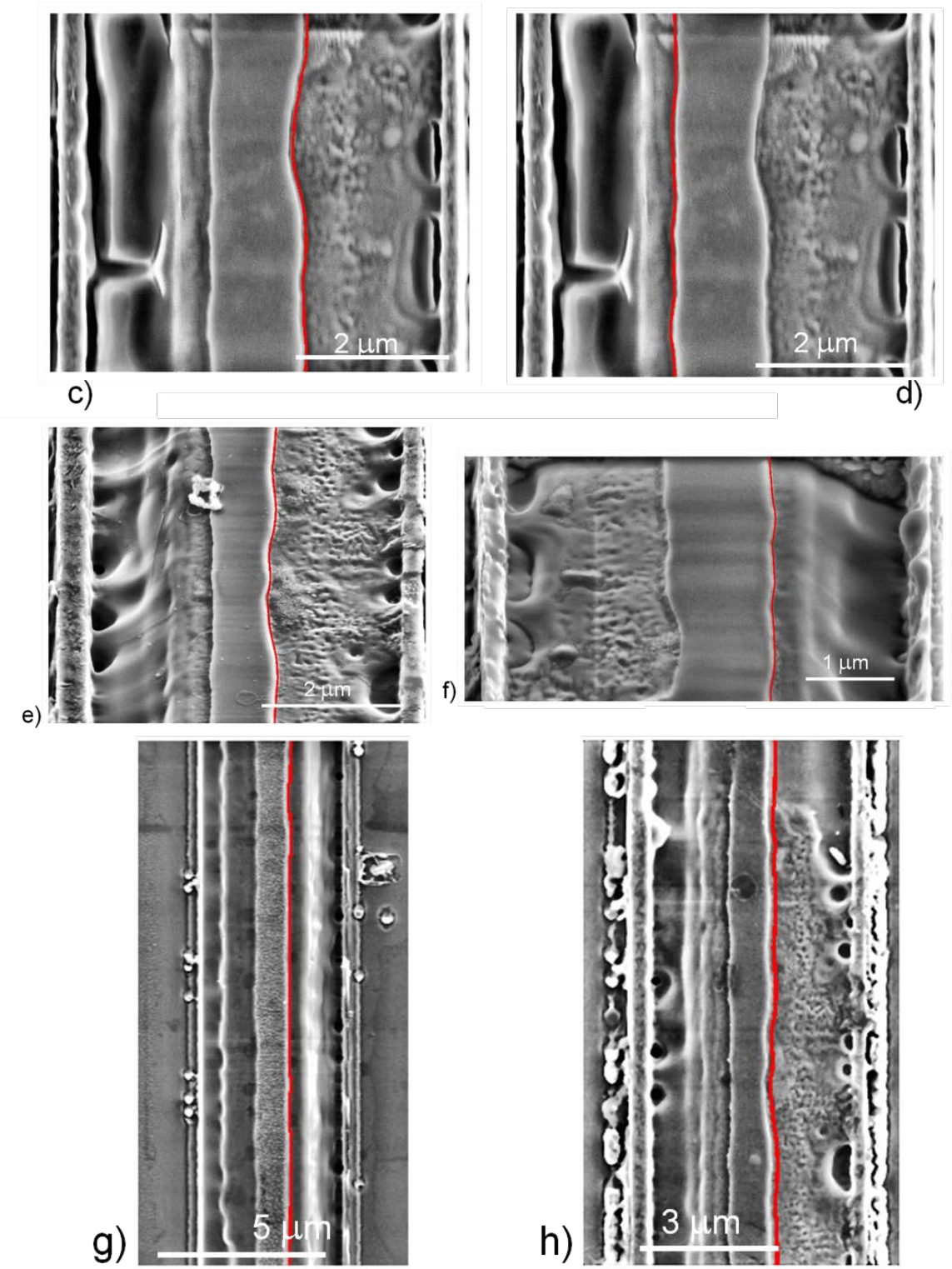


Figure 73 a) – h) Extraction of rough edge of the remaining PEC etched LD from SEM images after removing the p- epilayers by FIB cuts. c) Extraction of rough edge of the remaining PEC etched LD from an AFM image.

Figure 75 shows a plot of loss vs. roughness standard deviation (σ) for different correlation lengths. As expected the losses increase as σ increases. A decrease in L_c leads to a decrease in the scattering losses because a shorter L_c indicates an increase in the higher-frequency component of the roughness PSD, and usually scattering losses are mainly caused by low frequency component corresponding to a slower and wider variations.

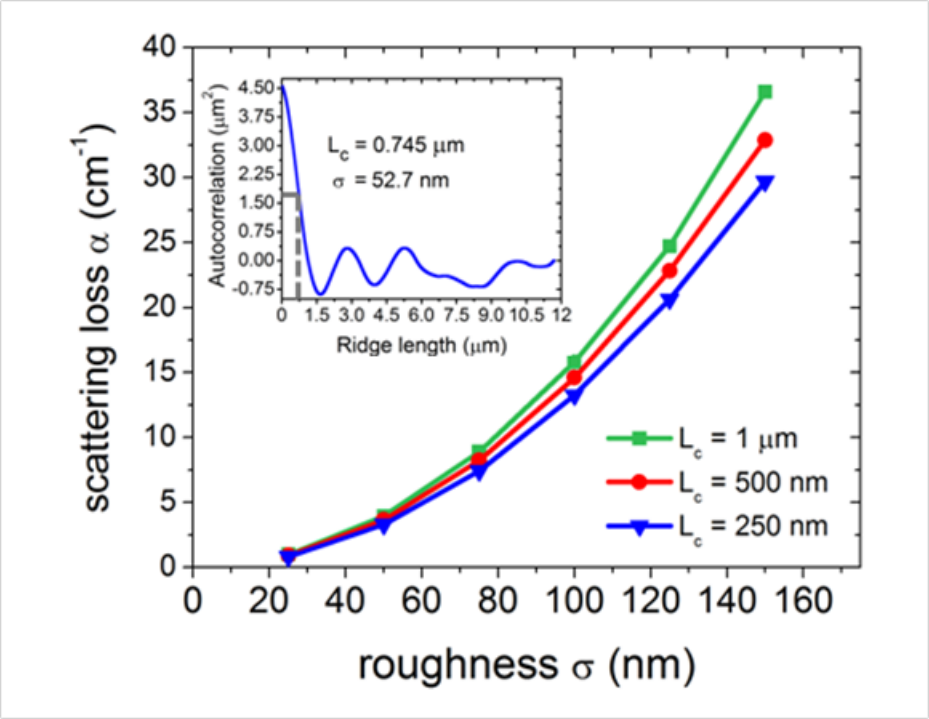


Figure 74 plot of loss vs. roughness standard deviation (σ) for different correlation lengths

The range for L_c and the roughness measured is in the order of ~600 ± 150 nm and ~ 60 ± 20 nm, respectively. This will cause optical scattering losses estimated in the range ~10-15 cm^{-1} for the CA-LD analyzed in Chapter 4. Although relatively high, this value is consistent with other propagation losses of GaN based waveguides reported in the literature [26-28]. Figure 76 shows the fit of the result with a Gaussian and exponential functions, with the first providing a better fit for describing small-scale features [29].

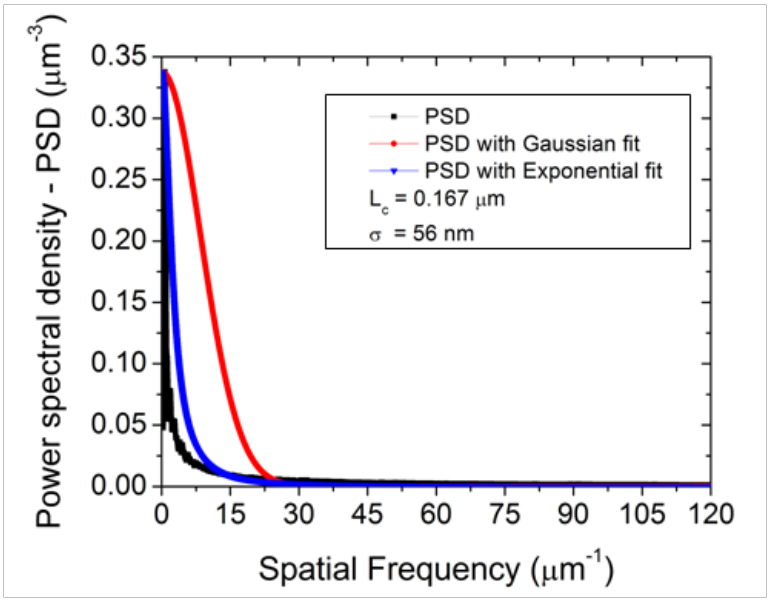


Figure 75 Fit of the PSD of the roughness with a Gaussian and exponential function

The sum of the roughness-induced scattering loss and the estimated materials internal loss, mainly caused by Mg p-doping (~25 cm^{-1}) and free carrier (~2 cm^{-1}) absorption [30] accounts for ~ 40% of the total loss $\langle \alpha_i \rangle$ that we computed by the intercept of the reciprocal of the differential efficiencies η_d versus the cavity length L [31] as shown in Fig. in Chapter 4.

$$\frac{1}{\eta_{diff}} = \frac{\langle \alpha_i \rangle}{\eta_i ln\left(\frac{1}{R}\right)} L + \frac{1}{\eta_i}$$

The missing loss could be attributed to the very irregular and wide bends like those shown in Fig 74 (g) and 3 (h) whose contributions have not been considered into the roughness-induced scattering loss computation presented. Simulations done in FIMMPROP [32], a 3D beam propagation commercial software, indicate that adiabatic change of a perfectly smooth

active region width does not contribute significantly to the radiation loss (Fig. 77 (a)) and ~ 99% of the optical power is transmitted (Fig. 77 (b)).

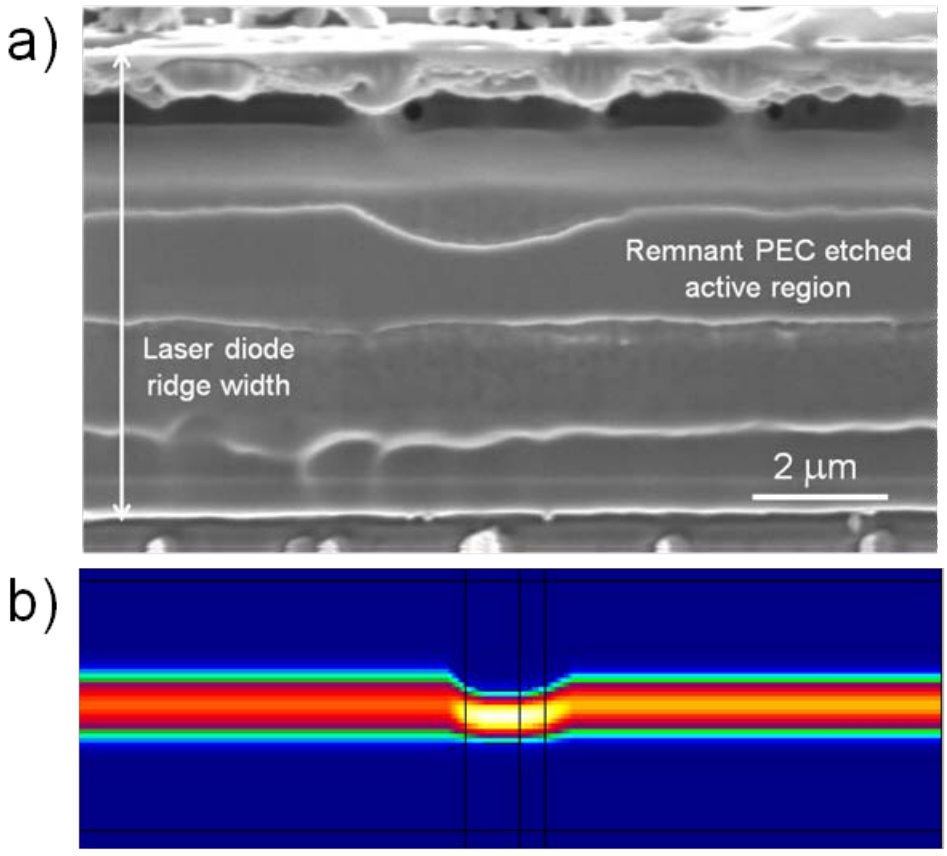


Figure 76 a) Rough edge of the remaining PEC etched LD from SEM images after removing the p- epilayers by FIB cuts showing an adiabatic and wide change in the width of the active region, b) FIMMPROP simulation showing that essentially all the power is transmitted through the two sections of the waveguide

By contrast, if the remnant PEC-etched active region has a very wavy profile as in Fig. 73 (i), the optical losses are more significant; a few defects causing extremely irregular shape as shown in Fig. 78 can account for more than half of the loss measured (Fig. 79)

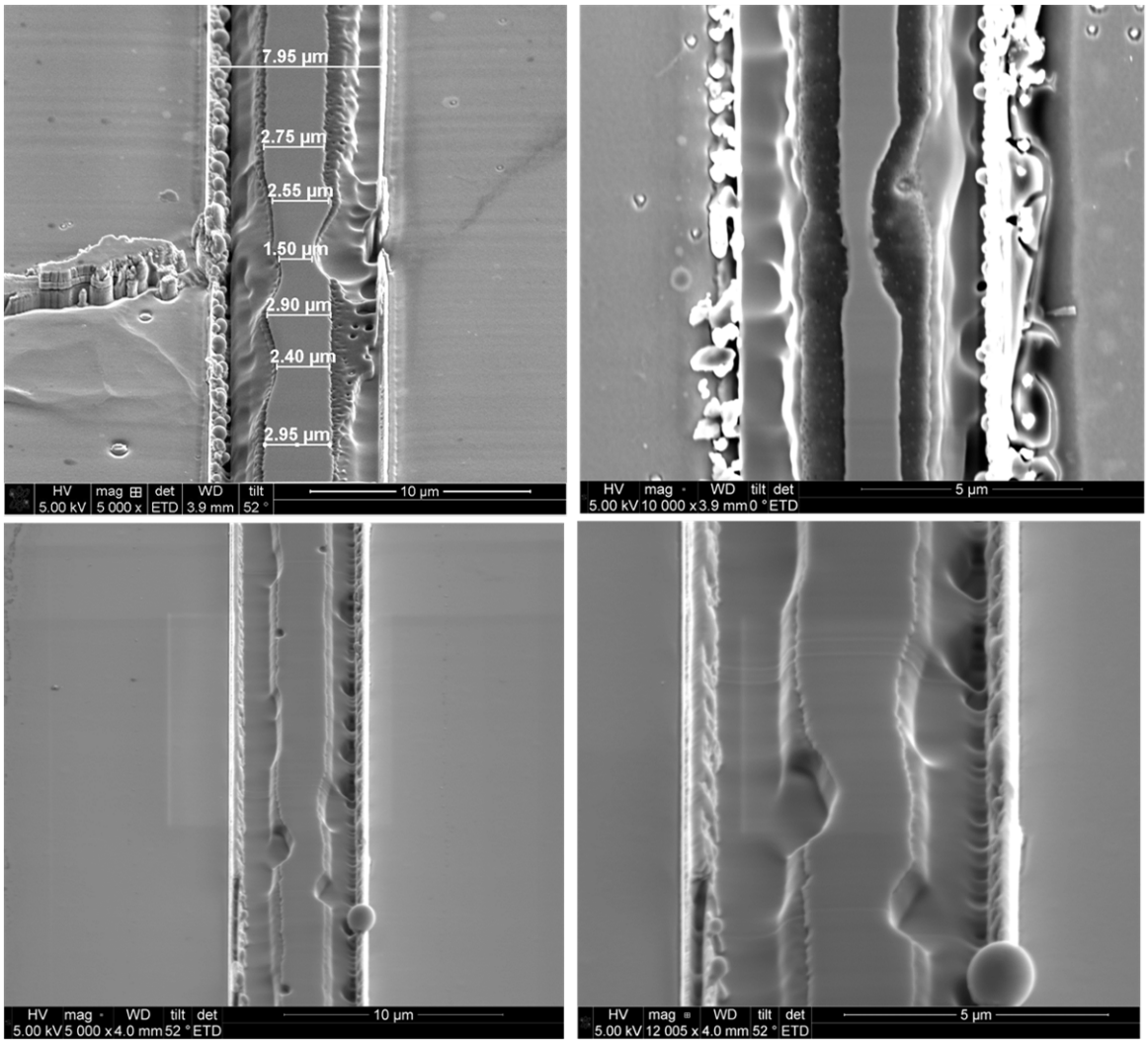


Figure 77 SEM images of CA-LD having a very irregular remnant of PEC etch active region

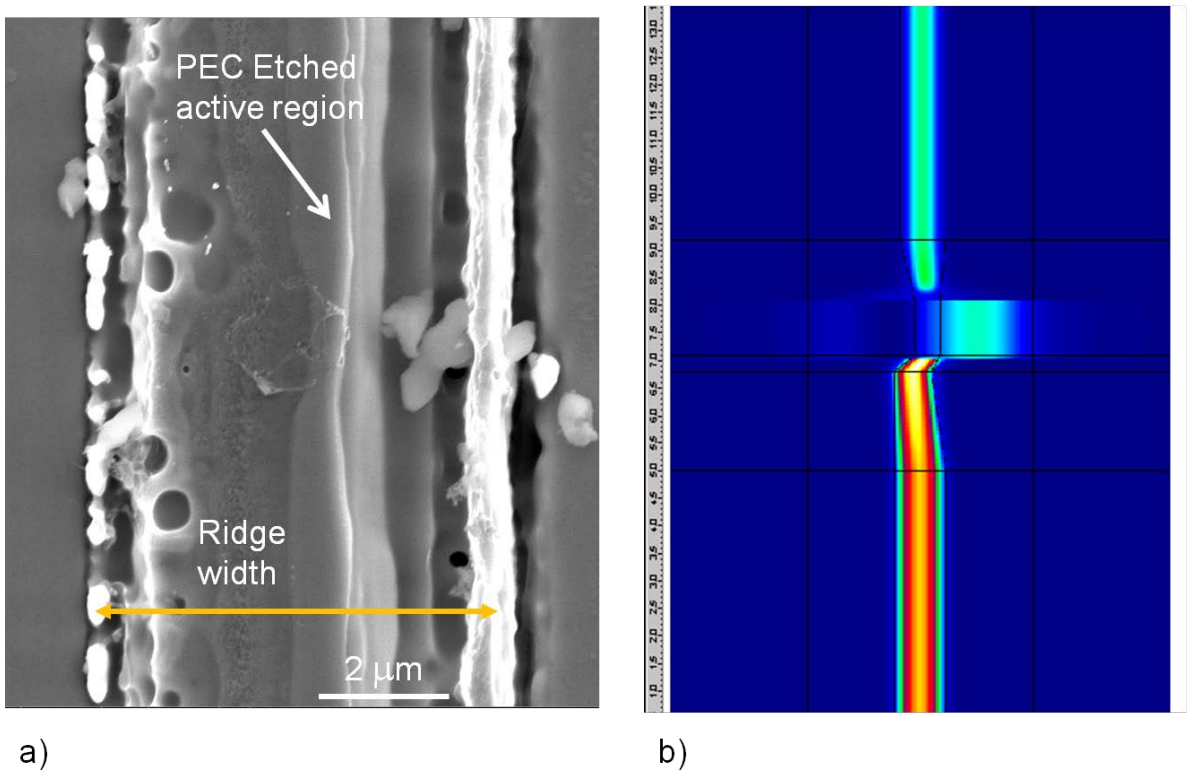


Figure 78 a) PEC etch LD with an irregular bend and b) relative FIMMPROP simulation showing that most of the power is radiated outside the waveguide

In general, if extended defects are not present in the structure, roughness can be greatly reduced by optimization of the fabrication process parameters. In the case of PEC etching, this can be obtained by choosing the more appropriate PEC etch conditions in terms of light intensity, molarity concentration of the electrolyte and stirring speed of the solution. Optimized epitaxial structure on high quality bulk GaN substrates is also essential to obtain smooth PEC etch as this depends on uniform carrier lifetime. Extended defects such as threading and misfit dislocations provide sites for non-radiative carrier recombination and thus they slow or halt the etching as shown in Chapter 2. Finally the roughness-induced scattering loss equation suggests that reducing the refractive index step between the unetched active region and the aperture pec-etched region, for example by filling the airgap

with polymer or oxide, can also help to decrease the scattering loss. Although filling the airgap leads to an increase of the interaction of the guided optical mode with the rough sidewall, the total scattering losses decrease because of their quadratic dependency on the difference between the core and the cladding of the waveguide. Furthermore, this can be beneficial because a widening of the optical mode can help for optical mode discrimination and prevent mode hopping in relatively large waveguides. As shown in Chapter 3, the airgap was filled by using photoresist (BCB 4022-35) and different types of dielectrics (Al_2O_3 and SiO_2). The dielectrics were deposited by atomic layer deposition (ALD) after a careful choice of the pumping and purging cycles of the precursors such that it was possible to fill undercut with aspect ratio exceeding ~500. The confinement factor in the rough edge of the active regions as defined above is 0.0093, 0.0101, 0.0104, 0.0110 for air, SiO_2, BCB 4022-35 and Al_2O_3, respectively. The refractive index at 440nm is 1, 1.466, 1.575 and 1.780 for air, SiO_2, BCB 4022-35 and Al_2O_3, respectively. Overall this should lead to a decrease in the roughness-induced scattering loss.

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Conclusions and future work

In this dissertation it has been presented an edge emitting laser diodes (CA-LD) with photoelectrochemically etched current apertures fabricated on *m*- and *20-2-1* planes emitting in the blue region of the visible spectrum .

As experimentally demonstrated in this work, this design provides several advantages compared to more commonly used shallow etched ridge design. In particular, it offers a lower threshold current density J_{th} and threshold voltage V_{th} and a reduction of series resistance R_s. Moreover, it also promises additional benefits for high-frequency related applications as it suffers from lower parasitic elements which make this device design promising for high-performance LDs. These benefits are more evident in narrow ridge LDs, that is devices whose ridge width is ~ 2.5 μm or less, which allow for single mode operation and are appealing for display applications where high optical mode quality is critical. Indeed, these narrow ridges are very sensitive to ridge etch depth and effects such as current

leakage, absorption of the unetched active region and antiguiding play a more important role in the determination of the threshold parameters than in wide LD ridges. Some of these considerations hold also for wide ridge LDs in case the traditional p-GaN is replaced by an AlGaN/GaN superlattice which helps spreading the current.

Although it had been realized already in mid-80s' in the InGaAsP material system, making a CA-LD in the nitride system present additional difficulties both in terms of growth and fabrication. In particular, nitrides lack of a standard wet etchant and to achieve selective and controllable undercut etching of the InGaN/GaN MQW active region of both *m*- and *20-2-1* LD structure, photoelectrochemical etching has been used and a new fabrication flow process has been designed. In particular, the lateral etch depth was defined by using an opaque metal mask that blocked the light responsible for the generation of carriers needed for the PEC etch process.

A precise control of the lateral etch depth has been achieved by using both these metal masks both on top of the mesa (that is the on top of the LD ridge) and on the field to reduce the amount of light reflected back from the rough surface. KOH (usually in a 1 M concentration) has been used as an electrolyte. It is therefore shown that PEC lateral etching has the potential to define optical and electrical current apertures in III-nitride devices for high-performance optoelectronics devices. In this way CA-LDs with top p-GaN areas that were wider than the active region have been fabricated and it was experimentally demonstrated that CA-LDs have lower threshold current density, threshold voltage and series resistance than shallow etched ridge LDs for an equivalent active region area and nominally identical epitaxial structure. The threshold current density, threshold voltage, peak output power, and series resistance for the CA-LD (shallow etched LD) with a 2.5 μm

wide active region were 4.4 (8.1) kA/cm^2, 6.1 (7.7) V, 96.5 (63.5) mW, and 4.7 (6.0) Ω under pulsed conditions and before facet coating, respectively. CW operation was achieved in a CA-LD with a 1.5 μm active region width below a 4.5μm wide p-contact, after the back facet of this set of devices was coated for high reflectivity (HR) using four periods of alternating quarter-wavelength layers of SiO_2 and Ta_2O_5, and the bar of lasers was soldered to a copper heat spreader. The CW threshold current density was 3.6 kA/cm^2 at 5.9 V.

An estimation of the roughening-induced scattering optical losses caused by imperfect photoelectrochemical (PEC) etching of the active region of a $(20\bar{2}\bar{1})$ InGaN MQW laser diode has been provided. Roughness data were obtained by AFM and SEM images processing of the remnant PEC-etched waveguides after the top p-layers were removed by focused ion beam cuts. Roughness (correlation length) values of ~60 (~600) nm have been measured and these can cause optical loss in the range of ~10 cm^{-1} as estimated by using the 3D Volume Current Method. Larger. FIMMPROP simulations suggest that more irregular bends contribute more significantly to the scattering loss.

In spite of these good results, several improvements can still be made in terms of materials growth, epitaxial layers engineering and fabrication to continuously improve LDs performance and achieve higher wall-plug efficiency which is required to allow the use of LDs for Solid State lighting and replace LEDs.

In particular, it will be important to continuously optimize the profile doping and alloy composition of every layer in order to reduce or eliminate possible sources of loss or obstacles to carriers flow. This should be done in conjunction with the development of a *n*++ layer for a top-side ohmic *n*- contact which will eliminate the voltage drop in the bulk

GaN and optimization of the $p++$ layer, eventually along with the insertion of a tunnel junction layer.

It will be also important to analyze the reliability and lifetime of the CA-LD, in particular to verify that the damages introduced by the RIE etching to form the ridge are effectively removed after the PEC etch.

Optimization of the PEC etch parameters (for example the molarity concentration of the solution, the light source and intensity, the stirring speed and the temperature of the solution), eventually also in different crystallographic orientations, along with improvement in the substrates quality will also lead to a better control of the lateral undercut, to a reduction of the roughness induced scattering losses and ultimately to an overall improvement in the device performance. In addition, it can open up new design possibilities, for example it might be possible to achieve a flip-chip design with different transparent oxide layers (for example ZnO and ITO) which will also allow the re-use of substrates which in turn will lead to a general cost reduction.

Appendices

Appendix A1

Current Aperture LD

Project Step	Equipment	#	Process Step
Remove Indium	Acid Bench	1	Mix 1:3 HNO_3:HCL (aqua regia) heated to 125 °C
		2	Etch sample in aqua regia for 5 min or more , repeat 2×
(Optional) Reactivate	MOCVD lab furnace	3	Reactivate in 15 min at 600 °C (or use RTA N2/O2 for 15 min at 600 °C)
SiNx-SiOy hard mask	PECVD	84	Deposit ~500 nm of SiN followed by ~600 nm of SiO2 and ~400 nm SiNx. (possible in multiple steps and rinse the sample in DI H2O in between)
	Ellipsometer	85	Measure Si Monitor #1 thickness[d]
Ridges Litho	Solvent bench	5	3 min Ace, 3 min Iso, 3 min DI, N2 dry
	PR Bench	6	Dehydration bake on hotplate at ≥110 °C for ≥2 min, let cool 1 min
		7	Spin LOL 2000, 2 krpm, 10 krpm/s, 30s (~250 nm thick)
		8	Clean backside of sample with EBR 100
		9	Bake on hotplate at 190 °C for 5 min, let cool for 2 min
		10	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		11	Clean backside of sample with EBR 100
		12	Soft bake on hotplate 95C for 90s
	GCA 200	13	Load mask PECE-New_Ridge
		14	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		15	Double check the program die size, run "EX RIDGESV4B"
		16	Pass: RIDGES
		17	No pass shift
		18	Expose 0.4 s, focus=0
	PR Bench	19	Post-exposure bake on hotplate at 110 °C for 90 s
	Develop Bench	20	Develop in 726MIF for 75 s (~15 nm/s undercut after reaching 45 s)
	Microscope	21	Inspect (verify ~0.3-0.5 µm undercut on LOL 2000), develop more if necessary
	UV Ozone	22	20 min (~6 Å/min)
	Dektak	23	Dektak RIDGES pad
Hard mask etch	ICP	24	Etch the SiNx-SiOy multilayer stack
	Solvent bench	38	1165 heated to 80 °C for 5+ min
		39	2 min Ace, 2 min Iso, 2 min DI, N2 dry

Ridges Etch	RIE #5	28	Load bare carrier wafer
		29	O2: 50 sccm, 50 mT, 300 W, 10 min, no He cooling
		30	BCL3/Cl2: 20/5 sccm, 10 mT, 15 W, 3min, no He cooling
		31	Cl2: 10 sccm, 5 mT, 200 W, 2 min, no He cooling
		32	Load sample(s) on carrier wafer (no mounting oil)
		33	BCL3: 10 sccm, 10 mT, 100 W, 2 min, no He cooling
		34	Cl2: 10 sccm, 5 mT, 200 W, ~9min (~120 ± 10 nm/min), no He cooling
		35	Soak sample in DI water for 2 min, N2 dry
	Microscope	36	Inspect
	Dektak	37	Dektak RIDGES pad
Litho for masking the active region and the field during PEC-etch	Solvent bench	38	1165 heated to 80 °C for 5+ min
		39	2 min Ace, 2 min Iso, 2 min DI, N2 dry
	PR Bench	40	Dehydration bake on hotplate ≥110 °C ≥2 min, let cool 1 min
		45	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		46	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		47	Clean backside of sample with EBR 100
		48	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	49	Load sample onto one of the black chucks
		50	Flood expose 1 s
	PR Bench	51	Let sample outgas for 5 min (VERY IMPORTANT)[f]
		52	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		53	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		54	Clean backside of sample with EBR 100
		55	Softbake on hotplate at 95 °C for 90 s
	GCA 200	56	Load mask #2 - P-contacts
		57	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		58	Run "EX RIDGESV4B"
		59	Pass: PCONTS
		60	No pass shift
		61	Expose 0.4 s, focus=0
	Develop bench	62	Develop in 726MIF for 60s (~2 µm undercut on OCG825)
		63	30 s x 3 rinse & dump DI, N2 dry
	Microscope	64	Inspect, develop more if necessary
	UV Ozone	65	20 min (~6 Å/min)
	Dektak	66	Dektak CONTACTS pad
Metal mask Dep both on top of the ridge and on the field	Acid Bench	67	Mix 1:1 HCl:DI
		68	Etch sample in 1:1 HCl:DI for 30 s
		69	30 s x 3 rinse & dump DI, N2 dry
	E-beam #3	70	Deposit 200/4500 Å Ti/Pt
	Solvent bench	71	Liftoff in 1165 heated to 80 °C for 45 min (or more if necessary)
		72	Move sample to fresh beaker of 1165
		73	Soak sample in 1165 heated to 80 °C for 10min, agitate with pipette
		74	3 min Ace, 3 min Iso, 3 min DI, N2 dry

	Microscope	75	Inspect, repeat 1165 if necessary
	Dektak	76	Dektak CONTACTS pad
PEC etch	PEII	77	O2 clean (300 mT, 100 W) for 1'
	Packaging lab	78	Mix 1:3 HCl:DI
		79	Dip the sample in 1:3 HCl:DI for 30 s
		80	Dip the sample in 1 Mol KOH solution. Set the 405 LD current to 120mA (or higher) - PEC- Etch for ~30'
	MOCVD lab	81	Inspect how far the lateral etch went under fluorescent microscope
Hard mask removal	Acid Bench	82	Dip the sample into HF for ~1 h
	Ellipsometer	83	Measure any possible resiude of oxide on the sample
Lithography to define apertures into the oxide on top of the ridges and outside the facets	Solvent bench	86	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	PR Bench	87	Dehydration bake on hotplate at ≥110 °C for ≥2 min, let cool 1 min
		88	Spin LOL 2000, 2 krpm, 10 krpm/s, 30s (~250 nm thick)
		89	Clean backside of sample with EBR 100
		90	Bake on hotplate at 190 °C for 5 min, let cool for 2 min
		91	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		92	Clean backside of sample with EBR 100
		93	Soft bake on hotplate 95C for 90s
	GCA 200	94	Load mask SiO2_ridges
		95	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		96	Double check the program die size, run "EX RIDGESV4B"
		97	Pass: RIDGES
		98	No pass shift
		99	Expose 0.4 s, focus=0
	PR Bench	100	Post-exposure bake on hotplate at 110 °C for 90 s
	Develop Bench	101	Develop in 726MIF for 75 s (~15 nm/s undercut after reaching 45 s)
	Microscope	102	Inspect (verify ~0.3-0.5 µm undercut on LOL 2000), develop more if necessary
	UV Ozone	103	20 min (~6 Å/min)
	Dektak	104	Dektak RIDGES pad
SiO2 field insulator deposition	PECVD	84	Deposit ~400 nm of SiO2. (possible in 2 steps and rinse the sample in DI H2O in between)
	Ellipsometer	85	Measure Si Monitor #1 thickness[d]
	Solvent bench		Soak sample in 1165 heated to 80 °C for 10min, agitate with pipette
			3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
ITO deposition	ebeam #2	4	Deposit ~100 nm heated ITO (set the temperature at 650C, actual temperature will be ~290)
ITO Pads Litho	PR Bench	44	Dehydration bake on hotplate ≥110 °C ≥2 min, let cool 1 min
		45	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		46	Spin nLOF2020, 4 krpm, 10 krpm/s, 30 s (~2 µm thick)

		47	Clean backside of sample with EBR 100
		48	Bake on hotplate at 110 °C for 1 min
	GCA 200	56	Load mask #2 - P-contacts
		57	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		58	Run "EX RIDGESV4B"
		59	Pass: PCONTS
		60	No pass shift
		61	Expose 0.176 s, focus=0
	PR Bench		Bake on hotplate at 110 °C for 1 min
	Develop bench	62	Develop in 300MIF for 90s
		63	30 s x 3 rinse & dump DI, N2 dry
	Microscope	64	Inspect, develop more if necessary
	UV Ozone	65	20 min (~6 Å/min)
	Dektak	66	Dektak CONTACTS pad
ITO etch	RIE #2	24	O2 chamber clean (20 sccm) - Set voltage 500 V for 30'
		25	MHA chamber seasoning (4/20/10 sccm). Set voltage 500 V for 20'
		26	Etch ITO using MHA (4/20/10 sccm). Set voltage 375 V for 9'
		27	O2 Clean (20 sccm) - Set voltage 170 V for 1'
Contact Pads Litho	Solvent bench	107	Soak sample in 1165 heated to 80 °C for 10min, agitate with pipette
		108	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	PR Bench	44	Dehydration bake on hotplate ≥110 °C ≥2 min, let cool 1 min
		45	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		46	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		47	Clean backside of sample with EBR 100
		48	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	49	Load sample onto one of the black chucks
		50	Flood expose 1 s
	PR Bench	51	Let sample outgas for 5 min (VERY IMPORTANT)[f]
		52	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		53	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		54	Clean backside of sample with EBR 100
		55	Softbake on hotplate at 95 °C for 90 s
	GCA 200	56	Load mask #2 - P-contacts
		57	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		58	Run "EX RIDGESV4B"
		59	Pass: PCONTS
		60	No pass shift
		61	Expose 0.4 s, focus=0
	Develop bench	62	Develop in 726MIF for 60s (~2 µm undercut on OCG825)
		63	30 s x 3 rinse & dump DI, N2 dry

	Microscope	64	Inspect, develop more if necessary
	UV Ozone	65	20 min (~6 Å/min)
	Dektak	66	Dektak CONTACTS pad
Contact Pads Dep	Acid Bench	67	Mix 1:3 HCl:DI
		68	Etch sample in 1:3 HCl:DI for 30 s
		69	30 s x 3 rinse & dump DI, N2 dry
	E-beam #3	70	Deposit 300/10000 Å Ti/Au
	Solvent bench	71	Liftoff in 1165 heated to 80 °C for 5 hours
		72	Move sample to fresh beaker of 1165
		73	Soak sample in 1165 heated to 80 °C for 10min, agitate with pipette
		74	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	Microscope	75	Inspect, repeat 1165 if necessary
	Dektak	76	Dektak CONTACTS pad
Facets Litho	Solvent bench	77	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	PR Bench	78	Dehydration bake on hotplate at ≥110 °C for 2 min, let cool 1 min
		79	Spin LOL 2000, 3 krpm, 10 krpm/s, 30 s (~200 nm thick)
		80	Clean backside of sample with EBR 100
		81	Bake on hotplate at 190 °C for 5 min, let cool for 2 min
		82	Spin SPR220-3.0, 2.5 krpm, 10 krpm/s, 30 s (~2.7 µm thick)
		83	Clean backside of sample with EBR 100 (very important)
		84	Bake on hotplate at 115 °C for 90 s
	GCA AutoStep 200	85	Load mask #3 - Etched Facets
		86	Load sample onto 2" 500 µm chuck with 180 µm shim with C+ pointing up
		87	Run "EX RIDGESV4B"
		88	Pass: FACETS
		89	Expose 0.65s, focus=0
	PR Bench	90	Bake on hotplate at 115 °C for 90 s
	Develop bench	91	Develop in 726MIF for 75 s
	Microscope	92	Inspect (verify ~0.5-0.7 µm undercut on LOL 2000), develop more if necessary
	PE II	93	20 s, 300 mT, 100 W
	Dektak	94	Dektak FACETS pad
Facets Etch	RIE #5	99	Load bare carrier wafer
		100	O2: 50 sccm, 50 mT, 300 W, 10 min, no He cooling
		101	BCL3/Cl2: 20/5 sccm, 10 mT, 15 W, 3min, no He cooling
		102	Cl2: 10 sccm, 5 mT, 200 W, 2 min, no He cooling
		103	Load sample(s) on carrier wafer (no mounting oil)
		104	BCL3: 10 sccm, 10 mT, 100 W, 2min, no He cooling
		105	Cl2: 10 sccm, 5 mT, 200 W, ~15 min (~100-150 nm/min), no He cooling

	Solvent bench	106	Strip mask in 1165 heated to 80 °C for 10+ min, agitate with pipette
		107	Move sample to fresh beaker of 1165
		108	Soak sample in 1165 heated to 80 °C for 2 min, agitate with pipette
		109	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	Microscope	110	Inspect, repeat with 80 °C PRX if necessary
	Dektak	11	Dektak FACETS pad
N-contact Dep & Liftoff	PR Bench	113	Mount sample upside down on Si wafer with a drop of AZ 4110
		114	Bake on hotplate at 105 °C for >5 min
	E-beam #3	115	Deposit 500/3000 Å Al/Au
	Solvent bench	116	Soak sample in 1165 heated to 80C until sample detaches from Si wafer[h]
		117	2 min Iso, 2 min DI, N2 dry
	Microscope	118	Inspect, repeat 1165 if necessary
Preliminary testing	Test lab	119	Test devices prior to facet coating (optional)
HR Back Facet Coating	Solvent bench	120	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	Gasonics	121	Recipe 7, multiple runs if desired[i]
	E-beam #1	122	Blanket deposit 500 Å of Ge with tilt & rotation on, with Si Monitor
	PR Bench	123	Dehydration bake on hotplate 110C 2min, let cool 1min
		124	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		125	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		126	Clean backside of sample with EBR 100
		127	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	128	Load sample onto one of the black chucks
		129	Flood expose 1 s
	PR Bench	130	Let sample outgas for 5 min (VERY IMPORTANT)
		131	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		132	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		133	Clean backside of sample with EBR 100
		134	Softbake on hotplate at 95 °C for 90 s
	GCA 6300	135	Load mask # 5 - Facet Coatings to coat both facets at once, or mask # 5b HR facet coatings (to coat the back HR mirror only)
		136	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		137	Run "EX RIDGESV4B"
		138	Pass: DBRS (pass shift = 0)
		139	Expose 2.20 s, focus=0
	Develop bench	140	Develop in 726MIF for 60 s (~2 µm undercut on OCG825)
		141	30 s x 3 rinse & dump DI, N2 dry

	Microscope	142	Inspect, develop more if necessary
	PE II	143	30 s, 300 mT, 100 W
	Acid Bench	144	Etch piece of Si Monitor in Hydrogen Peroxide to get etch rate
		145	Etch sample for double the monitor etch time (~60 s)
		146	1 min DI, N2 dry
	Veeco IBD	147	Calibrate the IBD for 45 ° platen angle using facet coating calibration
		148	Load samples
		149	Calculate new dep times to account for field vs facet coverage ratio. Use SiO2 time = 1.59*(calibrated SiO2 time), Ta2O5 time = 2.50*(calibrated Ta2O5 time)
		150	Set number of periods (normally 5–8), run recipe
	Solvent bench	151	Liftoff in 1165 heated to 80 °C for 10+ min, agitate with pipette
		152	Move sample to fresh beaker of 1165
		153	Soak sample in 1165 heated to 80 °C for 2 min, agitate with pipette
		154	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	Microscope	155	Inspect, repeat 1165 if necessary
	Acid Bench	156	Etch sample in Hydrogen Peroxide for double the monitor etch time (~60s)
		157	1 min DI, N2 dry
	Solvent bench	158	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	PR Bench	159	Dehydration bake on hotplate ≥110 °C 2 min, let cool 1 min
		160	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		161	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		162	Clean backside of sample with EBR 100
		163	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	164	Load sample onto one of the black chucks
		165	Flood expose 1 s
	PR Bench	166	Let sample outgas for 5 min (VERY IMPORTANT)
		167	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		168	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		169	Clean backside of sample with EBR 100
		170	Softbake on hotplate at 95 °C for 90 s
	GCA 6300	171	Load mask # 5c - Front facet coatings (if used #5b above)
		172	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		173	Run "EX RIDGESV4B"
		174	Pass: DBRs
		175	Expose 2.20 s, focus=0
	Develop bench	176	Develop in 726MIF for 60 s (~2 µm undercut on OCG825)
		177	30 s x 3 rinse & dump DI, N2 dry
	Microscope	178	Inspect, develop more if necessary

	PEII	179	30 s, 300 mT, 100 W
	Acid Bench	180	Etch piece of Si Monitor in Hydrogen Peroxide to get etch rate
		181	Etch sample for double the monitor etch time (~60 s)
		182	30 s x 3 rinse & dump DI, N2 dry
	Veeco IBD	183	Re-calibrate IBD if it has been more than 2 days since the HR facet coating
		184	Load samples
		185	Calculate new dep times: SiO2 time = (1.59*calibrated SiO2 time), Ta2O5 time = 2.50*(calibrated Ta2O5 time)
		186	Set number of periods (normally 2–3 or AR coating), run recipe
	Solvent bench	187	Liftoff in 1165 heated to 80 °C for 10+ min, agitate with pipette
		188	Move sample to fresh beaker of 1165
		189	Soak sample in 1165 heated to 80 °C for 2min, agitate with pipette
		190	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	Microscope	191	Inspect, repeat 1165 if necessary

Appendix A2

Current Aperture LD with aperture filled

Project Step	Equipment	#	Process Step
Remove Indium	Acid Bench	1	Mix 1:3 HNO_3:HCL (aqua regia) heated to 125 °C
		2	Etch sample in aqua regia for 5 min or more , repeat 2×
(Optional) Reactivate	MOCVD lab furnace	3	Reactivate in 15 min at 600 °C (or use RTA N2/O2 for 15 min at 600 °C)
ITO deposition	ebeam #2	4	Deposit ~100 nm heated ITO (set the temperature at 650C, actual temperature will be ~290)
Ridges Litho	Solvent bench	5	3 min Ace, 3 min Iso, 3 min DI, N2 dry
	PR Bench	6	Dehydration bake on hotplate at ≥110 °C for ≥2 min, let cool 1 min
		7	Spin LOL 2000, 2 krpm, 10 krpm/s, 30s (~250 nm thick)
		8	Clean backside of sample with EBR 100
		9	Bake on hotplate at 190 °C for 5 min, let cool for 2 min
		10	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		11	Clean backside of sample with EBR 100
		12	Soft bake on hotplate 95C for 90s
	GCA 200	13	Load mask PECE-New_Ridge
		14	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		15	Double check the program die size, run "EX RIDGESV4B"
		16	Pass: RIDGES
		17	No pass shift
		18	Expose 0.4 s, focus=0
	PR Bench	19	Post-exposure bake on hotplate at 110 °C for 90 s
	Develop Bench	20	Develop in 726MIF for 75 s (~15 nm/s undercut after reaching 45 s)
	Microscope	21	Inspect (verify ~0.3-0.5 µm undercut on LOL 2000), develop more if necessary
	UV Ozone	22	20 min (~6 Å/min)
	Dektak	23	Dektak RIDGES pad
ITO Etch	RIE #2	24	O2 chamber clean (20 sccm) - Set voltage 500 V for 30'
		25	MHA chamber seasoning (4/20/10 sccm). Set voltage 500 V for 20'
		26	Etch ITO using MHA (4/20/10 sccm). Set voltage 375 V for 9'
		27	O2 Clean (20 sccm) - Set voltage 170 V for 1'
Ridges Etch	RIE #5	28	Load bare carrier wafer

		29	O2: 50 sccm, 50 mT, 300 W, 10 min, no He cooling
		30	BCL3/Cl2: 20/5 sccm, 10 mT, 15 W, 3min, no He cooling
		31	Cl2: 10 sccm, 5 mT, 200 W, 2 min, no He cooling
		32	Load sample(s) on carrier wafer (no mounting oil)
		33	BCL3: 10 sccm, 10 mT, 100 W, 2 min, no He cooling
		34	Cl2: 10 sccm, 5 mT, 200 W, ~9min (~120 ± 10 nm/min), no He cooling
		35	Soak sample in DI water for 2 min, N2 dry
	Microscope	36	Inspect
	Dektak	37	Dektak RIDGES pad
Litho for masking the active region and the field during PEC-etch	Solvent bench	38	1165 heated to 80 °C for 5+ min
		39	2 min Ace, 2 min Iso, 2 min DI, N2 dry
	PR Bench	40	Dehydration bake on hotplate ≥110 °C ≥2 min, let cool 1 min
		45	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		46	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		47	Clean backside of sample with EBR 100
		48	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	49	Load sample onto one of the black chucks
		50	Flood expose 1 s
	PR Bench	51	Let sample outgas for 5 min (VERY IMPORTANT)[f]
		52	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		53	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		54	Clean backside of sample with EBR 100
		55	Softbake on hotplate at 95 °C for 90 s
	GCA 200	56	Load mask #2 - P-contacts
		57	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		58	Run "EX RIDGESV4B"
		59	Pass: PCONTS
		60	No pass shift
		61	Expose 0.4 s, focus=0
	Develop bench	62	Develop in 726MIF for 60s (~2 µm undercut on OCG825)
		63	30 s x 3 rinse & dump DI, N2 dry
	Microscope	64	Inspect, develop more if necessary
	UV Ozone	65	20 min (~6 Å/min)
	Dektak	66	Dektak CONTACTS pad
Metal mask Dep both on top of the ridge and on the field	Acid Bench	67	Mix 1:1 HCl:DI
		68	Etch sample in 1:1 HCl:DI for 30 s
		69	30 s x 3 rinse & dump DI, N2 dry
	E-beam #3	70	Deposit 200/4500 Å Ti/Pt
	Solvent bench	71	Liftoff in 1165 heated to 80 °C for 45 min (or more if necessary)
		72	Move sample to fresh beaker of 1165
		73	Soak sample in 1165 heated to 80 °C for 10min, agitate with pipette
		74	3 min Ace, 3 min Iso, 3 min DI, N2 dry
	Microscope	75	Inspect, repeat 1165 if necessary

	Dektak	76	Dektak CONTACTS pad
PEC etch	PEII	77	O2 clean (300 mT, 100 W) for 1'
	Packaging lab	78	Mix 1:3 HCl:DI
		79	Dip the sample in 1:3 HCl:DI for 30 s
		80	Dip the sample in 1 Mol KOH solution. Set the 405 LD current to 120mA (or higher) - PEC- Etch for ~30'
	MOCVD lab	81	Inspect how far the lateral etch went under fluorescent microscope
Airgap filling	ALD	82	Deposit ~80 nm Al2O3 (or thickness corresponding to the total active region thickness
	Ellipsometer	83	Measure Al2O3 thickness on Si Monitor
SiO2 field insulator deposition	PECVD	84	Deposit ~400 nm of SiO2. (possible in 2 steps and rinse the sample in DI H2O in between)
	Ellipsometer	85	Measure Si Monitor #1 thickness[d]
Lithography to define apertures into the oxide on top of the ridges and outside the facets	Solvent bench	86	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	PR Bench	87	Dehydration bake on hotplate at ≥110 °C for ≥2 min, let cool 1 min
		88	Spin LOL 2000, 2 krpm, 10 krpm/s, 30s (~250 nm thick)
		89	Clean backside of sample with EBR 100
		90	Bake on hotplate at 190 °C for 5 min, let cool for 2 min
		91	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		92	Clean backside of sample with EBR 100
		93	Soft bake on hotplate 95C for 90s
	GCA 200	94	Load mask SiO2_ridges
		95	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		96	Double check the program die size, run "EX RIDGESV4B"
		97	Pass: RIDGES
		98	No pass shift
		99	Expose 0.4 s, focus=0
	PR Bench	100	Post-exposure bake on hotplate at 110 °C for 90 s
	Develop Bench	101	Develop in 726MIF for 75 s (~15 nm/s undercut after reaching 45 s)
	Microscope	102	Inspect (verify ~0.3-0.5 µm undercut on LOL 2000), develop more if necessary
	UV Ozone	103	20 min (~6 Å/min)
	Dektak	104	Dektak RIDGES pad
Al2O3 and SiO2 etch on top of the LD ridge	ICP	105	Etch the SiO2 and Al2O3 on top of the ridge and stop at the ITO
	Acid Bench	106	Dip the sample into BHF for few seconds
Contact Pads Litho	Solvent bench	107	Soak sample in 1165 heated to 80 °C for 10min, agitate with pipette
		108	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)

	PR Bench	44	Dehydration bake on hotplate ≥110 °C ≥2 min, let cool 1 min
		45	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		46	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		47	Clean backside of sample with EBR 100
		48	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	49	Load sample onto one of the black chucks
		50	Flood expose 1 s
	PR Bench	51	Let sample outgas for 5 min (VERY IMPORTANT)[f]
		52	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		53	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		54	Clean backside of sample with EBR 100
		55	Softbake on hotplate at 95 °C for 90 s
	GCA 6300	56	Load mask #2 - P-contacts
		57	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		58	Run "EX RIDGESV4B"
		59	Pass: PCONTS
		60	No pass shift
		61	Expose 2.20 s, focus=0
	Develop bench	62	Develop in 726MIF for 60s (~2 µm undercut on OCG825)
		63	30 s x 3 rinse & dump DI, N2 dry
	Microscope	64	Inspect, develop more if necessary
	UV Ozone	65	20 min (~6 Å/min)
	Dektak	66	Dektak CONTACTS pad
Contact Pads Dep	Acid Bench	67	Mix 1:3 HCl:DI
		68	Etch sample in 1:3 HCl:DI for 30 s
		69	30 s x 3 rinse & dump DI, N2 dry
	E-beam #3	70	Deposit 300/10000 Å Ti/Au
	Solvent bench	71	Liftoff in 1165 heated to 80 °C for 5 hours
		72	Move sample to fresh beaker of 1165
		73	Soak sample in 1165 heated to 80 °C for 10min, agitate with pipette
		74	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	Microscope	75	Inspect, repeat 1165 if necessary
	Dektak	76	Dektak CONTACTS pad
Facets Litho	Solvent bench	77	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	PR Bench	78	Dehydration bake on hotplate at ≥110 °C for 2 min, let cool 1 min
		79	Spin LOL 2000, 3 krpm, 10 krpm/s, 30 s (~200 nm thick)
		80	Clean backside of sample with EBR 100
		81	Bake on hotplate at 190 °C for 5 min, let cool for 2 min
		82	Spin SPR220-3.0, 2.5 krpm, 10 krpm/s, 30 s (~2.7 µm thick)
		83	Clean backside of sample with EBR 100 (very important)
		84	Bake on hotplate at 115 °C for 90 s
	GCA AutoStep 200	85	Load mask #3 - Etched Facets
		86	Load sample onto 2" 500 µm chuck with 180 µm shim with C+ pointing up

		87	Run "EX RIDGESV4B"
		88	Pass: FACETS
		89	Expose 0.65s, focus=0
	PR Bench	90	Bake on hotplate at 115 °C for 90 s
	Develop bench	91	Develop in 726MIF for 75 s
	Microscope	92	Inspect (verify ~0.5-0.7 µm undercut on LOL 2000), develop more if necessary
	PE II	93	20 s, 300 mT, 100 W
	Dektak	94	Dektak FACETS pad
Facets Etch	RIE #2	95	O2 chamber clean (20 sccm) - Set voltage 500 V for 30'
		96	MHA chamber seasoning (4/20/10 sccm). Set voltage 500 V for 20'
		97	Etch ITO using MHA (4/20/10 sccm). Set voltage 375 V for 9'
		98	O2 Clean (20 sccm) - Set voltage 170 V for 1'
	RIE #5	99	Load bare carrier wafer
		100	O2: 50 sccm, 50 mT, 300 W, 10 min, no He cooling
		101	BCL3/Cl2: 20/5 sccm, 10 mT, 15 W, 3min, no He cooling
		102	Cl2: 10 sccm, 5 mT, 200 W, 2 min, no He cooling
		103	Load sample(s) on carrier wafer (no mounting oil)
		104	BCL3: 10 sccm, 10 mT, 100 W, 2min, no He cooling
		105	Cl2: 10 sccm, 5 mT, 200 W, ~15 min (~100-150 nm/min), no He cooling
	Solvent bench	106	Strip mask in 1165 heated to 80 °C for 10+ min, agitate with pipette
		107	Move sample to fresh beaker of 1165
		108	Soak sample in 1165 heated to 80 °C for 2 min, agitate with pipette
		109	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	Microscope	110	Inspect, repeat with 80 °C PRX if necessary
	Dektak	11	Dektak FACETS pad
N-contact Dep & Liftoff	PR Bench	113	Mount sample upside down on Si wafer with a drop of AZ 4110
		114	Bake on hotplate at 105 °C for >5 min
	E-beam #3	115	Deposit 500/3000 Å Al/Au
	Solvent bench	116	Soak sample in 1165 heated to 80C until sample detaches from Si wafer[h]
		117	2 min Iso, 2 min DI, N2 dry
	Microscope	118	Inspect, repeat 1165 if necessary
Preliminary testing	Test lab	119	Test devices prior to facet coating (optional)
HR Back Facet Coating	Solvent bench	120	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	Gasonics	121	Recipe 7, multiple runs if desired[i]
	E-beam #1	122	Blanket deposit 500 Å of Ge with tilt & rotation on, with Si Monitor
	PR Bench	123	Dehydration bake on hotplate 110C 2min, let cool 1min
		124	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		125	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		126	Clean backside of sample with EBR 100

		127	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	128	Load sample onto one of the black chucks
		129	Flood expose 1 s
	PR Bench	130	Let sample outgas for 5 min (VERY IMPORTANT)
		131	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		132	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		133	Clean backside of sample with EBR 100
		134	Softbake on hotplate at 95 °C for 90 s
	GCA 6300	135	Load mask # 5 - Facet Coatings to coat both facets at once, or mask # 5b HR facet coatings (to coat the back HR mirror only)
		136	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		137	Run "EX RIDGESV4B"
		138	Pass: DBRS (pass shift = 0)
		139	Expose 2.20 s, focus=0
	Develop bench	140	Develop in 726MIF for 60 s (~2 µm undercut on OCG825)
		141	30 s x 3 rinse & dump DI, N2 dry
	Microscope	142	Inspect, develop more if necessary
	PE II	143	30 s, 300 mT, 100 W
	Acid Bench	144	Etch piece of Si Monitor in Hydrogen Peroxide to get etch rate
		145	Etch sample for double the monitor etch time (~60 s)
		146	1 min DI, N2 dry
	Veeco IBD	147	Calibrate the IBD for 45 ° platen angle using facet coating calibration
		148	Load samples
		149	Calculate new dep times to account for field vs facet coverage ratio. Use SiO2 time = 1.59*(calibrated SiO2 time), Ta2O5 time = 2.50*(calibrated Ta2O5 time)
		150	Set number of periods (normally 5–8), run recipe
	Solvent bench	151	Liftoff in 1165 heated to 80 °C for 10+ min, agitate with pipette
		152	Move sample to fresh beaker of 1165
		153	Soak sample in 1165 heated to 80 °C for 2 min, agitate with pipette
		154	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	Microscope	155	Inspect, repeat 1165 if necessary
	Acid Bench	156	Etch sample in Hydrogen Peroxide for double the monitor etch time (~60s)
		157	1 min DI, N2 dry
	Solvent bench	158	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	PR Bench	159	Dehydration bake on hotplate ≥110 °C 2 min, let cool 1 min
		160	Spin HMDS, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)
		161	Spin OCG825, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)
		162	Clean backside of sample with EBR 100
		163	Bake on hotplate at 95 °C for 2 min
	MJB-3 (left aligner only)	164	Load sample onto one of the black chucks
		165	Flood expose 1 s

	PR Bench	166	Let sample outgas for 5 min (VERY IMPORTANT)
		167	Bake on hotplate at 95 °C for 2 min, let cool 1 min
		168	Spin 955CM-1.8, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)
		169	Clean backside of sample with EBR 100
		170	Softbake on hotplate at 95 °C for 90 s
	GCA 6300	171	Load mask # 5c - Front facet coatings (if used #5b above)
		172	Load sample onto 2" 500 µm chuck with 180 µm shim with *c*+ pointing up
		173	Run "EX RIDGESV4B"
		174	Pass: DBRs
		175	Expose 2.20 s, focus=0
	Develop bench	176	Develop in 726MIF for 60 s (~2 µm undercut on OCG825)
		177	30 s x 3 rinse & dump DI, N2 dry
	Microscope	178	Inspect, develop more if necessary
	PEII	179	30 s, 300 mT, 100 W
	Acid Bench	180	Etch piece of Si Monitor in Hydrogen Peroxide to get etch rate
		181	Etch sample for double the monitor etch time (~60 s)
		182	30 s x 3 rinse & dump DI, N2 dry
	Veeco IBD	183	Re-calibrate IBD if it has been more than 2 days since the HR facet coating
		184	Load samples
		185	Calculate new dep times: SiO2 time = (1.59*calibrated SiO2 time), Ta2O5 time = 2.50*(calibrated Ta2O5 time)
		186	Set number of periods (normally 2–3 or AR coating), run recipe
	Solvent bench	187	Liftoff in 1165 heated to 80 °C for 10+ min, agitate with pipette
		188	Move sample to fresh beaker of 1165
		189	Soak sample in 1165 heated to 80 °C for 2min, agitate with pipette
		190	3 min Ace, 3 min Iso, 3 min DI, N2 dry (sonicate on very low)
	Microscope	191	Inspect, repeat 1165 if necessary

Appendix A3

Procedure to etch the facets using FIB

This appendix summarizes the procedure to achieve a smooth and vertical etch of LD facets using Focus Ion Beam (FIB).

As shown in this thesis, FIB is an extremely powerful, although relatively slow, technique to pattern device at micro- and nano- scale. The FIB which was used in this work is an FEI dual beam® which allows to image and etch a sample, along with locally depositing material (Pt, in the case of the FIB in question), at the same time.

As it is possible to deposit material with both the electron and ion gun, similarly it is also possible to image the sample with both the electron and ion gun. However, similarly to what happens in the Name of the Rose, the bestseller of U. Eco where whoever reads Aristotle's treatise on comedy, ends up to die (and the death occurs as sooner as the reader reads more pages of the book, because these had been poisoned), it is important to minimize the time used to image the sample (even just for double-checking the eucentric point) with the ion-gun (essentially the longer the user looks at the sample with the ion gun, the more the sample is involuntarily etched, in an uncontrollable way and region extent).

After loading the sample into the chamber and pump it down (the chamber pressure needs to be at least ~2E-5 or lower), the user must look for the eucentric point (that is the point where the ion and the electron gun image the same point on the sample). For that, it is important to

reach a z-height of ~4.5 mm (be careful not to touch the electron nor the ion gun). The sample is then moved of different degrees (start with 5, then 20 and then 52) and its position can be adjusted with the joystick until the eucentric point is achieved (the software will automatically correct the actual height in the meantime). Then a layer of ~1 um of Pt is deposited on top of the ridge – particular care needs to be taken not to create a short between the conductive substrate and the top-side (usually *p*-) contact, by inserting the needle and using a ion beam current of max 0.28 nA and 30KV (select the option "rectangle" in the ion-gun menu). After the needle is removed, the first cut (select the option "regular cut" in the ion-gun menu) can be done with an ion current as high as 6.5 nA (the ion beam can be as high as 21 nA but such high current caused deep damages which can make short across the structure), this is followed but a second cut done using an ion current of 2.8 nA, finally a last cut is done with a current of 96 pA (a cut with a current of 0.28 nA would also work). A refined cut can also be done by selecting the option "cleaning cross section" in the ion-gun menu). The total time needed to achieve a good cut is ~20 min/facet depending on the number of refining cut and on the ion beam current used to cut.

After each of these cuts is finished, it is important to look at the sample using the electron beam – and putting in Idle the ion beam –and make sure that the sample is still at the eucentric point, that is it has not moved too much. A similar procedure can be used to reveal the active region and remove the *p*- epilayers described in Chapter 5.

Appendix A4

Estimation of the optimum width aperture

The main benefits of the CA-LD design operated in DC are represented by a decrease of a) the threshold current density J_{th} (in particular for narrow ridge LD), b) the threshold voltage V_{th} and c) series resistance (R_s), which will overall lead to an increase in the wall plug efficiency (WPE, or Power Conversion Efficiency, PCE) of the device.

The benefit of decreasing the series resistance is related to the wider p-GaN contact area with respect to the active region area, feature which is peculiar to this design and distinguish it from both the shallow and deep etch ridge design, in which the p-GaN has the same area of the active region. Ideally the reduction in series resistance is as higher as the p-GaN is wider, but in practice this is limited to the spreading current length in the p-GaN contact. Although it is expected that this advantage is more apparent for poor p-GaN contact, the CA-LD design will bring some benefits in reducing R_s. even for more optimized p-GaN contact. Indeed, Feezell et al., have demonstrated experimentally this by fabricating an InP-based TJ-CA-VCSEL (*Tunnel Junction Current Aperture VCSEL*, Journal of Quantum Electronics, 42, 5, 2006), where despite the good contact obtained by through the tunnel junction, the aperture provides still benefits to improve the device performance.

One of the main issues in the Nitrides system is the limited p-GaN conductivity (and the relative current spreading) which set an upper bound to the benefits that the CA-LD design can offer for reducing the series resistance.

Although a detailed and accurate modeling of the full structure is not easy to make because of the complex device geometry (and an experimentally demonstration of the optimum aperture width is left as future work), it is presented in this section a simple modeling which show that the optimum aperture width (or undercut) is on the order of ~3 μm for an active region width of 1.5 μm. Beyond this undercut length, the benefits of the aperture decrease and it can actually create some problems in terms of mechanical stability of the device (in particular if the undercut is not filled).

In a rather crude approximation, we can assume the p-GaN as a 2D network of resistor and a metal contact as wide as the active region width as sketched in Fig. 80.

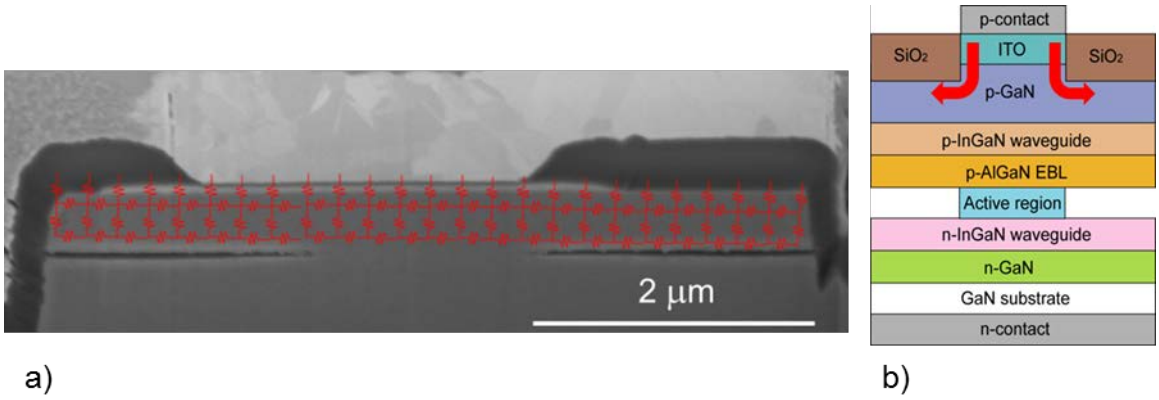

Figure 79 Schematics of a) the 2D resistor network modeling the p-GaN, b) lateral diffusion current path. The length over which the current value drops to 1/e the value of the current which reaches the active region is defined as current spreading length.

In this model, the current spreading length Ls in the p-GaN epilayer can be expressed as the length over which the diffusion current drops to 1/e of the value of the current which goes straight into the active region and it can be computed as :

$$L_s = \frac{4k_BTd}{q\rho J_t w} + \frac{1}{2}\sqrt{\frac{16k_BTd}{q\rho J_t} + \left(\frac{8k_BTd}{q\rho J_t w}\right)^2}$$

where k_BT/q is thermal voltage, J_t the total injected current, ρ, t and w are the resistivity, thickness and (total) width of the p-GaN, respectively.

Fig. 80 shows a plot of the current spreading length vs. half-ridge witdh for different p-GaN resistivity and thickness. The spreading length is longer for thicker and more resistive p-GaN.

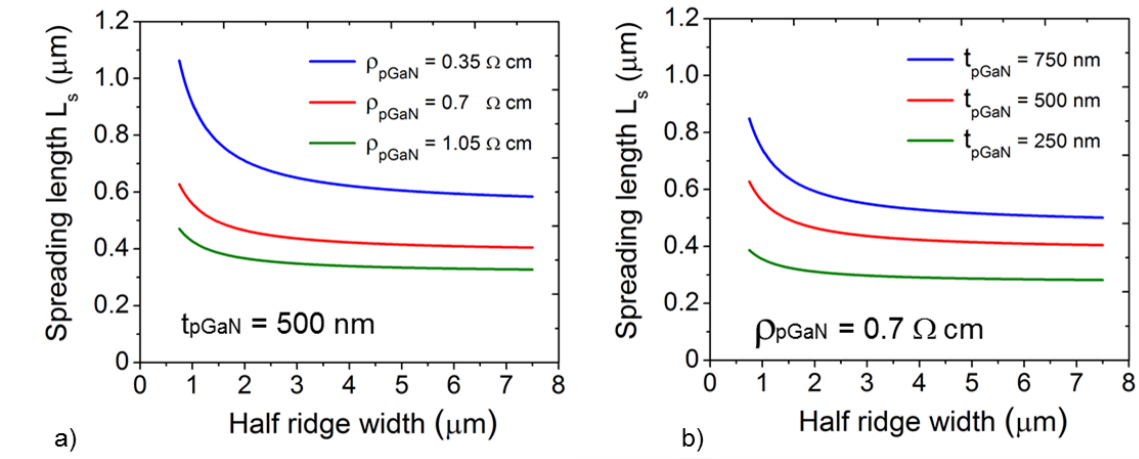

Figure 80 Plot of a) current spreading length vs. half ridge width for different p-GaN resistivity and pGaN thickness of 500 nm, b) current spreading length vs. half ridge width for different p-GaN thickness and pGaN resistivity of 0.7 Ωcm

A more refined modeling has been using COMSOL: the CA-LD has been still been modeled as simple resistor network and in order to estimate the benefits of the aperture the p-GaN and a thin p-GaN contact layer width was varied in the range 1.5 μm up to 10 μm, while the

active region width and the n-GaN bulk were kept at a fixed width of 1.5 μm and 12 μm, as shown in Fig. 81.

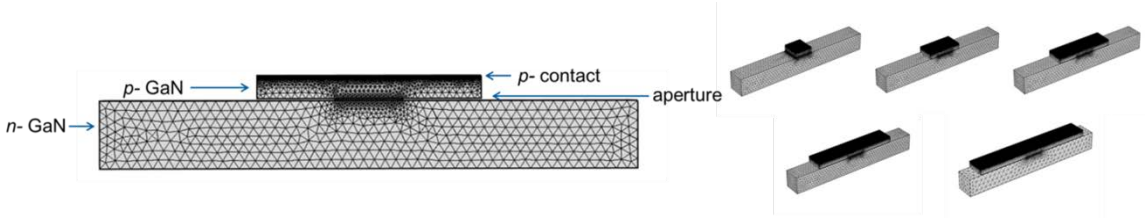

Figure 81 Schematic of the CA-LD modeled in COMSOL

The thickness of the p-GaN contact layer, p-GaN, active region and n-GaN were 20 nm, 500 nm, 50 nm and 1.5 μm, respectively. The length of the bar is assumed to be only 1.5 μm in order to speed up the computation time while maintaining a very fine mesh. The parameters are summarized in the table below:

	Width	Thickness	Length	Resistivity
***p*- GaN contact**	Range 1.5-10 μm	20 nm	1.5 μm	Range: 10 - 2 KΩ/cm
***p*- GaN**	Range 1.5-10 μm	500 nm	1.5 μm	0.33 Ω/cm
Active region	1.5 μm	50 nm	1.5 μm	0.14 Ω/cm
***n*- GaN**	12 μm	1.5 μm	1.5 μm	0.01 Ω/cm

By fixing the input voltage at 1 V and integrating the different current density profiles along a constant line of the p-GaN (Fig. 82), the resistance was estimated for different p-GaN contact width and resistivity (Fig. 83).

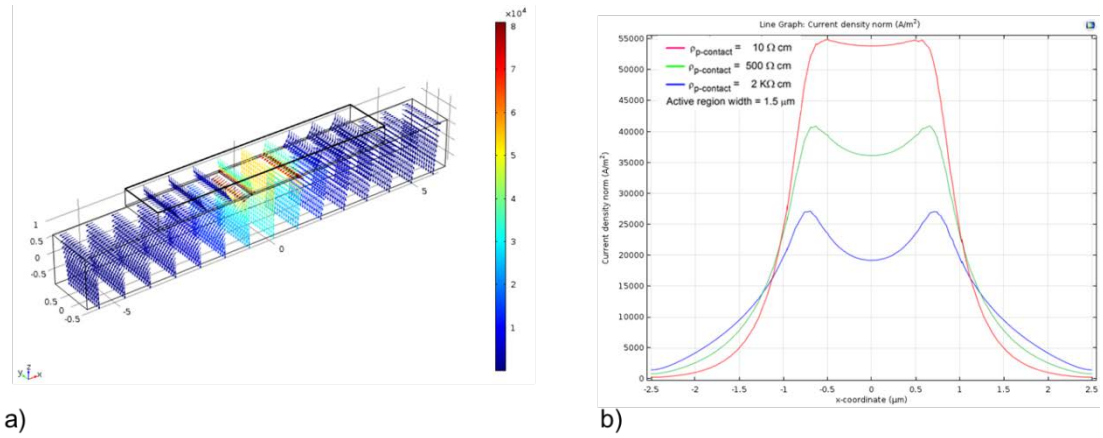

Figure 82 a) 3D and b) 2D current density profile for different p-GaN contact resistivity

Figure 83 shows that the benefits of the CA-LD are most notably for highly-resistive p-GaN contact layers, as it could have been expected; however, it is worth to note that a relative high improvement is also present in case of good p-contact layer. Moreover, after a certain aperture width the contribution to the decrease in R_s becomes negligible.

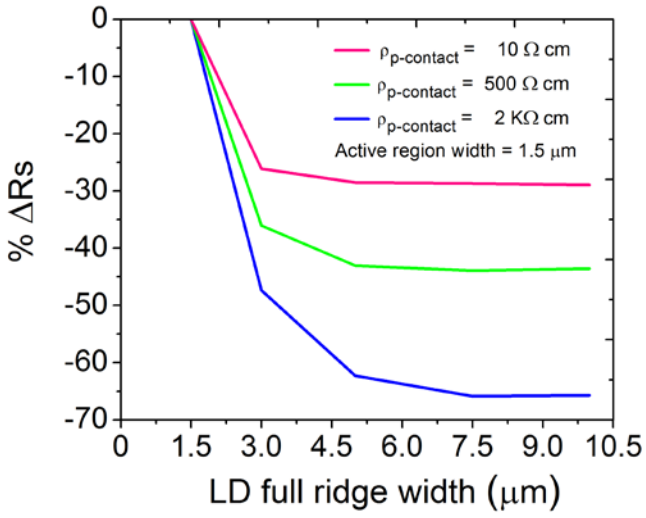

Figure 83 Percentage of change in Rs for different aperture width and different p-GaN contact resistivity