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Epitaxy and Device Design for High Efficiency Blue LEDs and Laser Diodes

A dissertation submitted in partial satisfaction of the

requirements for the degree

Doctor of Philosophy in Materials

by

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December 2016

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“Knowledge and wonder are the dyad of our worthy lives as intellectual beings.”

-Stephen Jay Gould

This dissertation is dedicated to my grandmother, Sylvia V. Perna,

who taught me to uncompromisingly exercise my intellect.

Acknowledgments

I would like to begin my acknowledgments with the mentors who first started me on the path to graduate school nearly 10 years ago. Professor Deborah Gordon was my first research mentor at Stanford. She tapped my deep and lifelong love of nature and insects and guided me and my teammates in a multi-year study in ant ecology that was the foundation for all of my future research experiences. My summer research mentors at NREL, Dr. Todd Deutsch and Dr. John Turner, tugged me toward the physical sciences by giving me a project on materials for photoelectrochemical hydrogen generation. Professor Tom Jaramillo at Stanford took me on as an undergraduate researcher to work on thin film chalcogenides in my senior year and assigned me Zhebo Chen as my graduate student mentor. They were all instrumental in advancing my career into academic research, and I'm grateful to all of them for their mentorship and encouragement.

My good fortune with great mentors continued during my time at UCSB. First and foremost, I thank my advisors Professors Jim Speck and Claude Weisbuch. Claude started me on a project doing ray tracing simulations in the summer before my first year, which proved to be an immensely useful skill during my PhD. Both Jim and Claude assigned me challenging and important projects, held me to a high standard of critical thinking, and maintained lofty expectations for my work and future. I was lucky to also be advised by Professor Steve DenBaars, who helped my projects move forward by offering pragmatic advice and "golden nuggets" of MOCVD brilliance. Professors Shuji Nakamura and Umesh Mishra, who round out my committee, provided enthusiasm and ideas and challenged me with tough questions. Their influence has elevated my work. In addition to my committee, I

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Many students and post docs also provided research mentorship. Christopher Lalau Keraly transferred his knowledge in ray tracing simulations and phosphor characterization methods and continued to be generous with his help even a year after moving on from UCSB. Nathan Pfaff showed me the ropes around the cleanroom and taught me the LED fabrication process. I owe a great debt to Kate Kelchner who taught me MOCVD, *m*-plane materials characterization, and laser processing and with whom I co-authored several papers and shared many good conversations. Joe Nedy can be counted in many categories as my friend, officemate, climbing buddy, and coauthor, and he also stands out as a fantastic mentor who was generous with his time and knowledge. He helped me learn to write Matlab code, discussed laser physics with me at length, and fielded my incessant barrage of questions with patience and thoughtfulness.

My mentees were as wonderful as my mentors. Daniel Myers was basically the best undergraduate intern one could ever ask for, and I'm so delighted that he is also pursuing a PhD. Arwa Saud Abbas and I quickly forged a great connection, and she was important to the success of the CAIBE facet development project.

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Last and most, I thank my family, for nurturing a little girl who liked bugs and chemistry, writing and music, into a surprisingly well-adjusted adult.

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EDUCATION

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> *m*-plane and *c*-plane In/Al/GaN-based light emitting devices, MOCVD (metalorganic chemical vapor deposition), Monte Carlo ray tracing simulations, LED and laser device fabrication

2009-2010: **Stanford Chemical Engineering**, Jaramillo Laboratory, Undergraduate Researcher

> Chemical bath deposition and material characterization of molybdenum disulfide thin films for solar energy conversion

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2007-2010: **Stanford Biological Sciences**, Gordon Laboratory, Undergraduate Researcher

> Animal behavior of native and invasive ant species of Central California

PUBLICATIONS & PATENTS

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2013-2016: Volunteer for **UCSB's ScienceLine Program**
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Abstract

Epitaxy and Device Design for High Efficiency Blue LEDs and Laser Diodes

by

Leah Yvonne Kuritzky

The (Al,Ga,In)N materials system has impacted energy efficiency on the world-wide scale through its application to blue light-emitting diodes (LEDs), which were invented and developed in the 1990s. Since then, cost reductions and performance improvements have brought GaN-based LEDs into the mainstream, supplanting outdated lighting technology and improving energy efficiency.

One of the main challenges that still limits commercial LEDs, however, is "efficiency droop," which refers to the reduction in efficiency as the input current density (and with it, the carrier density) increases. This phenomenon especially plagues high power LEDs, which operate in the current density range of 100-1000 A/cm^2.

Few practical options exist to directly eliminate efficiency droop, however we investigated two complementary approaches to circumvent the phenomenon. The first "high power solution" would employ blue laser diodes as the engine of solid state white lighting in lieu of LEDs. When laser diodes reach the threshold current density for stimulated emission, the carrier density in the active region clamps, simultaneously clamping droop. The wall-plug efficiency of the laser diodes can then continue to rise as input current density increases until another effect (usually thermal) overrides it. The second "low power solution" maintains the blue LED as the solid state lighting engine, but shifts the operation point to low current density (and low carrier density) where efficiency droop effects are negligible and other

thermal and electrical constraints in the device design are alleviated, enabling designs for high wall-plug efficiency. Both approaches to circumventing efficiency droop are likely to find a home in diverse future technologies and applications for lighting and displays.

The challenge to produce high performance blue laser diodes was approached from an *m*-plane epitaxy platform. *m*-Plane is a non-polar orientation of the wurtzite (Al,Ga,In)N, which is free from deleterious polarization-related electric fields in the growth direction. *m*-Plane is a naturally occurring crystal plane with high material gain due to its non-degenerate valence band structure, and thus should be well-suited for laser diode applications. However, *m*-plane blue emission suffers from low indium uptake and broad spontaneous emission linewidth. The use of surface "double miscut" was investigated to improve the local step structure and morphology, resulting in higher indium uptake, narrower linewidth and higher peak power in the blue spectrum.

The complementary challenge to improve the wall-plug efficiency for LEDs at low power operation focuses primarily on improved light extraction efficiency and low voltage operation. The main sources of extraction efficiency losses in typical *c*-plane blue LEDs on patterned sapphire substrates are absorption on the metal contacts, in the current spreading layer and on the metallic reflector, which also doubles as the heat sink. With the relaxed constraints at low power operation, new designs become possible. High light extraction designs were vetted with ray tracing software prior to experimental implementation. The highest demonstrated wall-plug efficiency resulting from these designs was 78.2%, and was accompanied by a greater than unity electrical efficiency (1.03) resulting from thermoelectric pumping, suggesting a pathway for 100% or greater wall-plug efficiency.

Table of Contents

Chapter 1. Introduction to GaN Optoelectronics in the Blue Spectrum

The (Al,Ga,In)N materials system has impacted energy efficiency on the world-wide scale through its application to blue light-emitting diodes (LEDs). This impact on technology and society was recognized by the award of the 2014 Nobel Prize in Physics to Isamu Akasaki, Hiroshi Amano, and Shuji Nakamura. These researchers persevered in their pursuit of this difficult materials system despite the popularity of the competing ZnSe-based system and the widespread scientific opinion that the high dislocation density ($> 10^9$ cm^{-2}) of III-N films would prevent their application to any useful device.[1] Breakthroughs in III-N crystal growth led to the demonstration of high brightness GaN-based blue and green LEDs by Shuji Nakamura in 1993 - 95.[2,3] After those demonstrations, interest in III-N materials grew rapidly, and the ZnSe system was rendered obsolete for light-emitting applications. Since then, cost reductions and performance improvements have brought GaN-based LEDs into the mainstream, supplanting outdated lighting technology and dramatically improving energy efficiency.

As a result of the increased interest in III-N materials since the early 1990s, not only have blue LEDs improved to the point of widespread commercialization, but many new properties of the III-N materials system have been identified, explained and applied to new innovations. The direct, wide band gap of III-N semiconductors makes them promising for solar cell materials[4,5] intended for ultra-high efficiency multi-junction stacks. High frequency GaN electronic devices for power switching applications offer a potential 10% reduction in U.S. electricity demand by replacing entrenched but less efficient silicon

technology.[6] New advances in light-emitting devices have emerged as well, including the expansion of the III-N LED wavelength range to the deep UV[7] and the long red spectrum[8,9] and the development of electrically injected III-N quantum well (QW) laser diodes emitting in the near-UV[10] to the green[11] spectrum. All of these applications have potential in energy efficiency or energy conversion and are expected to positively impact the energy landscape in the 21st century. Continued research aims to bring efficiencies of existing devices to their theoretical limits, while conceiving and developing new applications for nitride materials.

1.1 The III-N Materials System for Optoelectronics in the Visible Spectrum

The binary nitrides cover a wide range of direct band gap energies with E_g = 0.7 eV, 3.4 eV, and 6.0 eV for InN, GaN, and AlN, respectively, which is advantageous for producing a gamut of optoelectronics wavelengths from the infrared to the UV spectra. However, the large mismatch in lattice constants among the binary nitrides (Fig. 1.1) results in highly strained heterostructures with ternary alloys. This strain can lead to defect formation, reduced material quality, and polarization-related electric fields in basal plane growth.

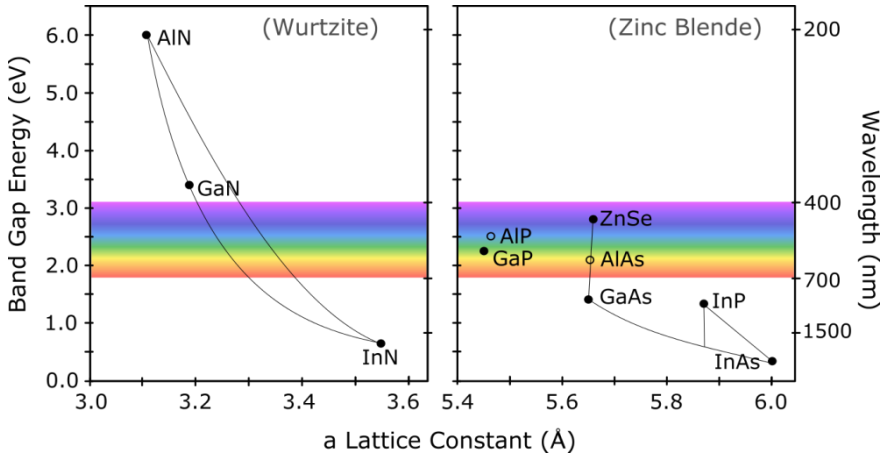

Figure 1.1. Band gap energy vs. lattice constant for III-V and II-VI semiconductors. Open circles indicate indirect band gap materials. InGaN and AlGaN ternary alloys span a large range of lattice constants. Reprinted with permission from [12].

The III-N wurtzite crystal is polar and piezoelectric due to its 6mm point symmetry. Commercial III-N devices are primarily grown on the basal *c*-plane (0001) in the polar **c**-direction by heteroepitaxy on sapphire or SiC substrates. Devices grown on the *c*-plane offer high performance despite the very high dislocation densities (~10^9 cm^{-2}) induced by non-native substrates.[1] However, *c*-plane devices also exhibit polarization-induced electric fields in strained heterostructures that bend the energy bands. This results in separation of the electron and hole wavefunctions in strained $In_xGa_{1-x}N$ QWs (Fig. 1.2) that reduces radiative recombination rates, especially for wide QWs (> 3 nm). This effect is referred to as the Quantum Confined Stark Effect (QCSE),[13,14] and it is exacerbated by increasing strain associated with increasing indium composition for longer wavelength emitters. As a result, low indium content, violet-emitting *c*-plane QW devices have shown higher efficiencies than longer wavelength devices.[15]

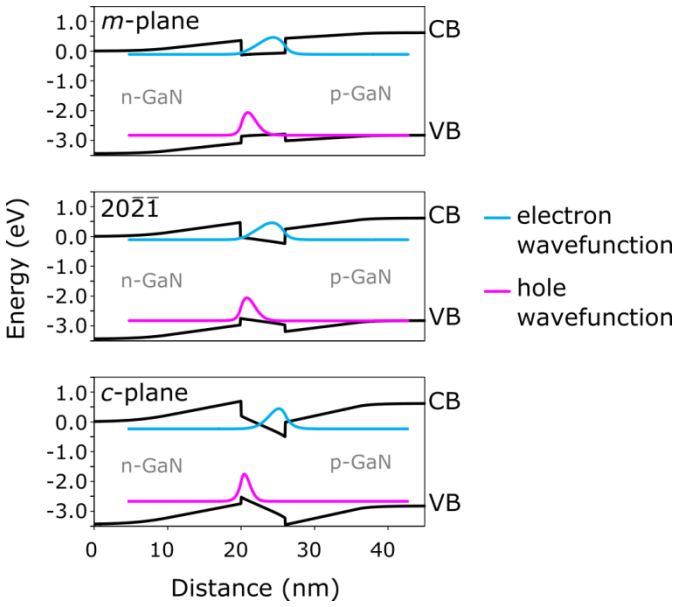

Figure 1.2. Schrodinger-Poisson drift-diffusion simulations of the conduction band (CB), valence band (VB) and electron and hole wavefunctions for LED structures on *m*-plane $(1\bar{1}00)$, $(20\bar{2}\bar{1})$ and *c*-plane (0001) using SiLENSe software package.[16] The simulated structure is a 6 nm $In_{0.19}Ga_{0.81}N$ QW and 10 nm undoped GaN barriers. The QW and barriers are contained in a p-n junction (ND = 3×10^{18}, NA = 5×10^{19}). The structure is simulated at room temperature under a 2.7 V bias. The effect of the applied bias and the internal electric fields on the spatial separation of carrier wavefunctions is shown. The surface is to the right. Reprinted with permission from [12].

Non-basal plane (NBP) orientations of the wurtzite (Al,Ga,In)N crystal (Fig. 1.3) were predicted 15 years ago to eliminate (for nonpolar planes) or reduce (for semipolar planes) the polarization-related electric fields in the growth direction (Fig. 1.2).[17] However, early efforts to perform heteroepitaxy on NBP orientations, for example, *a*-plane GaN epitaxy on *r*-plane sapphire substrates, were unsuccessful due to the high density of extended defects, especially threading dislocations and basal plane stacking faults.[18] In 2006, low dislocation density bulk GaN substrates became commercially available and enabled high quality growth on NBP orientations. This launched a new field of materials research on semipolar and nonpolar surfaces, which has since led to many high performance and long wavelength devices.[9,19–21]

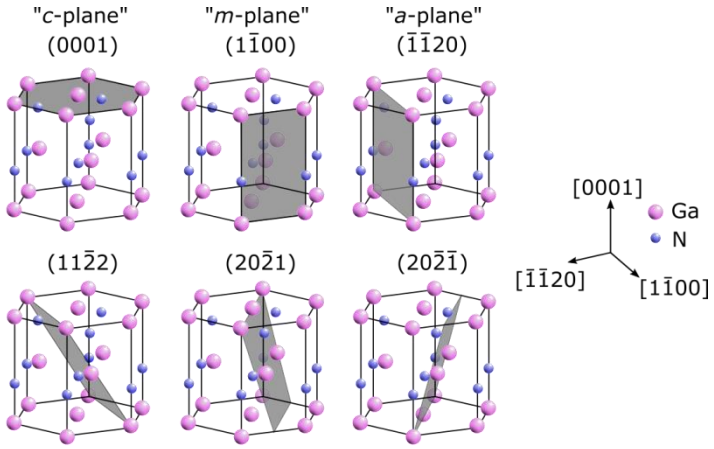

Figure 1.3. The wurtzite crystal structure showing the polar, basal *c*-plane (0001), nonpolar *m*-plane (1$\bar{1}$00), nonpolar *a*-plane ($\bar{1}\bar{1}$20), and semipolar planes of interest for blue and green LDs. Reprinted with permission from [12].

New materials or wavelengths for optoelectronic devices are generally developed for LEDs before LDs due to their simpler structure and the fewer requirements for producing spontaneous emission compared to stimulated emission. LED structures typically require one or more QWs sandwiched within a p-n junction. An electron and/or hole blocking layer (EBL or HBL) may also be included to reduce carrier overflow and improve efficiency. In addition to these LED layers, LD structures require optical confinement. This is usually achieved for edge-emitting III-N LDs with epitaxial InGaN waveguiding and/or AlGaN cladding layers that create a refractive index contrast to confine the optical mode over the gain-producing QWs. Dispersion effects reduce the refractive index contrast for longer wavelength light, so blue and green devices require relatively higher alloy content waveguiding or cladding layers compared to violet devices. The strain associated with these lattice mismatched heterostructures must be managed, especially for long wavelength emitters. Alternatively, quaternary AlInGaN cladding layers that are lattice-matched to GaN may be used.[22,23]

Due to these challenges, direct III-N LDs in the green spectral region (> 515 nm) have only been realized in the past seven years[15,23,24] and have been demonstrated

exclusively on the *c*-plane and semipolar ($20\bar{2}1$) orientations. So far, only spontaneous QW electroluminescence has been demonstrated for direct yellow wavelengths.

By contrast, short wavelength $In_xGa_{1-x}N$ QW LDs are already high performing. Violet *c*-plane LDs with $In_xGa_{1-x}N$ ($x \approx 0.10$) QWs have been commercialized since the early 2000s for optical data storage in Blu-ray Discs. Blue *c*-plane QW LDs have also been commercialized and have seen rapid improvements in output power and efficiency in recent years.[25] Improvements in LD performance, especially in blue and longer wavelengths are important for bringing LD sources to general white lighting applications, where, in certain applications, they have the potential to increase efficiency, reduce costs, and add value compared to LED sources.

1.2. LEDs and Laser Diodes for Solid State White Lighting

Phosphor converted blue LEDs have made dramatic performance improvements over the past 10 years in efficiency and affordability and now provide economic options for many white lighting installations. Their rapid economic payoffs are due to their low electricity consumption and associated operating costs as well as their long lifetimes. One of the main challenges that still limits commercial LEDs, however, is "efficiency droop," which refers to the reduction in efficiency as the input power density increases (Fig. 1.4).

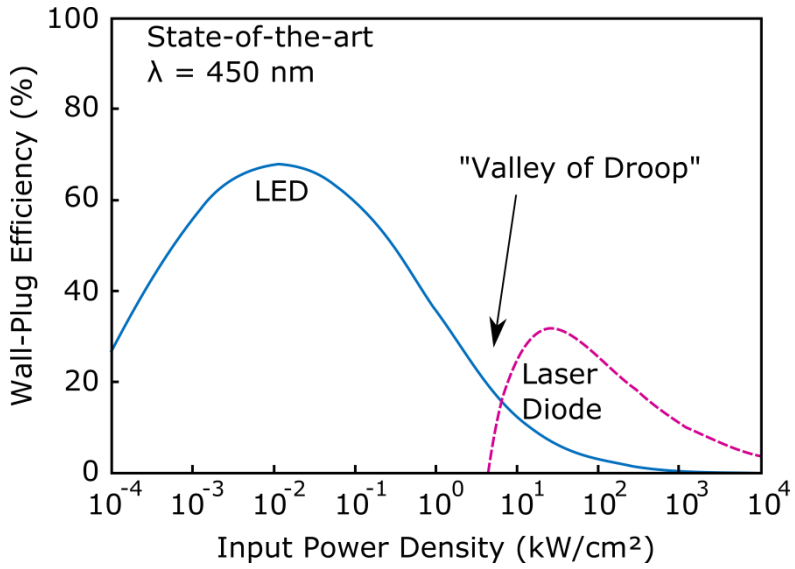

Figure 1.4. State-of-the-art efficiency curves for blue LEDs and laser diodes. The "valley of droop"[26] occurs at medium input power densities where the LED efficiency is strongly reduced by Auger recombination while the laser diode is still below threshold. Figure adapted from [26].

The droop phenomenon occurs primarily by a mechanism of non-radiative Auger recombination.[27,28] Auger recombination is a three particle process and thus is proportional to the cube of the carrier density. In the ABC model,[29] the internal quantum efficiency (IQE) of an LED is given by:

$$\text{IQE} = \frac{Bn^2}{An + Bn^2 + Cn^3}$$

where A, B, and C are the Shockley-Read-Hall, radiative and Auger coefficients, respectively, and n is the carrier density. As such, the Auger recombination term is dominant at high carrier densities (and high current densities) where high power LEDs would operate (J = 100 – 1000 A cm^{-2}).[29]

It was previously thought that Auger recombination should be negligible in wide band gap visible nitride LEDs because a limited number of energy- and momentum-conserving direct transitions are available to accept scattered electrons or holes. An indirect mechanism was eventually described in 2011 in which the Auger process is assisted by momentum

changes due to phonon interactions and alloy scattering.[27] Computational studies showed that this mechanism can predominate for wide band gap materials and that Auger recombination is therefore the primary cause of efficiency droop in III-N LEDs. This was experimentally confirmed by the direct detection of Auger electrons by electroemission spectroscopy in 2013.[28]

Currently, *c*-plane devices utilize thin QWs (< 3 nm), intended to reduce the QCSE. However, the reduced active volume results in exacerbated efficiency droop due to the increased carrier density. As a result, typical blue *c*-plane LEDs reach their peak IQE at very low current densities of 1 – 10 A cm^{-2}. To generate sufficient lumens, a commercial LED bulb must either contain a small number of LEDs operated at high power densities (high brightness per chip, reduced efficiency) or many LEDs operated at low power density (low brightness per chip, near peak efficiency). The former choice incurs the cost of additional heat sinking due to the less efficient chips, and the latter incurs the cost of additional processing and packaging of semiconductor material.

One option for realizing high efficiencies at high power densities, and thus low cost (high lumens/$), is to use LDs rather than LEDs for the blue photon source. Although the peak wall-plug efficiency for state-of-the-art blue LDs is lower (38%)[25] than for blue LEDs (> 70%)[30], the LD peak efficiency occurs at an input power density ($P_{input} \approx 25$ kW/cm^2) that is over three orders of magnitude higher than where the LED peak efficiency occurs ($P_{input} \approx 3$ W/cm^2) (Fig. 1.4).[30] Thus, the brightness per epitaxial area is tremendously enhanced for LDs.

Improvements to blue III-N LD peak efficiency are expected as the technology develops through research and industry learning, just as LED peak efficiency has improved

over the past two decades. The main challenges that currently limit the peak efficiency of III-N blue LDs are the relatively high threshold current densities ($J_{th} \approx 3$ kA cm^{-2})[31–33] and the low differential efficiencies ($\eta_d = 0.5 – 0.65$)[32,34,35] caused by high internal optical losses ($\alpha_i \approx 15$ cm^{-1})[36] compared to more efficient III-V materials systems ($J_{th} < 100$ A cm^{-2},[37] $\eta_d = 0.88$,[38,39] $\alpha_i \approx 1$ cm^{-1} [38,39]).

A low lasing threshold is important for high efficiency because below threshold, the LD emission is primarily spontaneous, and the efficiency is subject to all modes of non-radiative recombination, including Auger recombination and resulting efficiency droop. The efficiency droops significantly as the LD approaches threshold, but above threshold, all spontaneous and non-radiative recombination rates clamp at their threshold values, allowing the LD efficiency to increase to its peak value.

The low conductivity of the p-doped layers also reduces the LD efficiency by increasing the series resistance. The thick optical confinement layers can have a particularly large contribution to series resistance. Innovative LD designs may enable the removal of some p-doped layers to reduce both internal losses and series resistances. The reduced QCSE for NBP orientations may also allow for epitaxial designs with wide QWs, which can provide enough waveguiding to remove the AlGaN cladding layers completely.[40] Additionally, NBP orientations have higher barriers to carrier overflow due to their reduced internal electric fields, which may allow for elimination of the highly Mg-doped EBL, especially for long wavelength emitters which have deep QWs.[41,42]

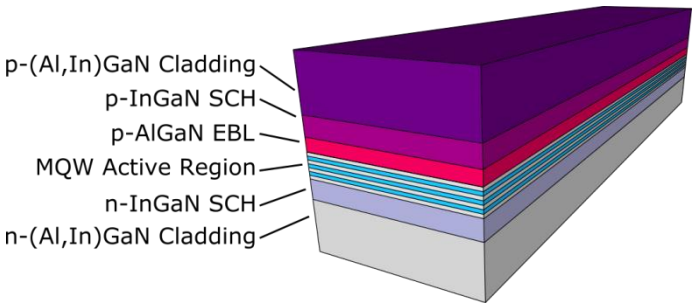

Figure 1.5. A schematic of a LD structure that includes both a high refractive index InGaN waveguiding separate confinement heterostructure (SCH) and low refractive index cladding layers made of GaN, AlGaN, or AlInGaN. The p-type layers including the p-EBL, p-SCH, and p-cladding layers are highly lossy due to the optical absorption associated with high Mg concentrations. The n-side layers are relatively low loss. Reprinted with permission from [12].

Recent reviews assessing the viability of III-N LDs to replace LEDs for solid state lighting suggest the development of NBP orientations to improve projected LD efficiencies.[26,30] In addition to enabling epitaxial structure variations, NBP orientations can reduce or eliminate QCSE and increase the modal gain. These characteristics are expected to reduce threshold current densities, thus reducing the threshold-clamped values of the A, B and C recombination rates and improving LD wall-plug efficiency.

1.3. Opportunities in Non-Basal Plane Orientations for Blue Laser Diodes

Non-basal plane (NBP) research is relatively nascent, apart from early work on non-native substrates which showed highly defective growth and poor luminescence performance.[43] The breakthrough in producing commercial, low threading dislocation density, freestanding bulk GaN crystals by hydride vapor phase epitaxy in 2006 opened up this new research arena Slicing and polishing of *c*-plane GaN boules now gives researchers access to any desired crystal plane. Some of the highest performing semipolar planes that are now available by this method were not previously accessible on any non-native substrates.[44]

In addition to reduced QCSE, the unbalanced biaxial in-plane stress in NBP QWs separates the top two VB energies which leads to anisotropy of the optical gain.[43,45] The top VB (called the CH1 band[43]) has |X⟩ character (dipole parallel to the $[1\bar{2}10]$ for $(h0\bar{h}l)$ planes) and is strongly populated. This leads to polarized emission for NBP LEDs and reduces the VB density of states to enhance gain in NBP LDs.[43] NBP LDs with ridges oriented along the high gain axis should theoretically have higher material gain than *c*-plane LDs.[46] Additionally, the CH1 band has a smaller hole effective mass than the *c*-plane VB.[43] This is expected to reduce transparency currents for NBP LDs.[47]

Theoretically, the nonpolar planes should yield the greatest benefit compared to *c*-plane due to their complete elimination of internal electric fields and their very high polarization ratios (> 95% for *m*-plane LEDs emitting near 520 nm[48]), which indicates strong energy splitting of the VBs. For this reason, much early work focused on nonpolar growth on both hetero- and homoepitaxial platforms, particularly on the nonpolar *m*-plane, which showed several times higher output powers than the nonpolar *a*-plane in early LED comparisons.[49] Theoretical calculations predicted that *m*-plane would yield higher optical gain than *c*-plane or semipolar planes,[46] and this is consistent with experimental measurements of the modal gain in commercial LDs using the Hakki-Paoli method.[47]

Despite these advantages, *m*-plane has proven challenging for wavelengths longer than violet. Broad electroluminescence peaks are observed in the blue spectrum, attributed to non-uniform indium incorporation.[50] New research on miscut *m*-plane surfaces has yielded improvements to electroluminescence quality in the blue spectrum,[51,52] which will be described in detail in Ch. 2, but access to wavelengths > 500 nm is still limited. As the *m*-plane QW wavelength is increased into the cyan spectrum, a precipitous drop in output

power is observed at approximately 490 nm which is concurrent with the formation of a high density of basal plane stacking faults.[53,54] The record longest cw lasing wavelength for *m*-plane is still 499.8 nm, demonstrated at Rohm Corporation in 2008.[20]

1.4. Opportunities to Enhance Wall-Plug Efficiency for Low Power LED Operation

While laser diodes offer a high power option to circumvent efficiency droop, the problem may also be addressed by a low power option by moving the operating point of blue LEDs to their point of peak IQE, which occurs at current densities typically of 1 – 5 A/cm^2. If blue LED designs are optimized for operation at these low current densities, very high wall-plug efficiency becomes possible. The wall-plug efficiency, also known as the power conversion efficiency, describes the optical power out of the device divided by the input power (generally reported for a lab power source directly supplying a DC current). The WPE per electron/hole pair can be expressed as:

$$\mathrm{WPE} = \mathrm{IQE} \times \mathrm{LEE} \times \frac{V_p}{V}$$

where IQE is the internal quantum efficiency, describing the fraction of electrons injected into the LED which generate photons in the active region. LEE is the light extraction efficiency, describing the fraction of photons generated in the active region that are emitted to free space. V is the operating voltage, and $V_p = h\nu/q$ is the photon voltage, where $h\nu$ is the photon energy.

At low current density, low power LED operation, opportunities arise to increase all three components of the WPE. First, the LED may be operated at the peak IQE, eliminating effects of efficiency droop. Second, the LED may be designed with smaller metal contacts, thinner current spreading layers and reduced or eliminated heat sink, which can reduce light

absorption in the chip and increase the light extraction efficiency (topic of Ch. 3). Finally, when the LED is operated at low bias, the effects of ohmic losses are minimized, enabling a low voltage operation. Ch. 4 will discuss the possibility of operating at voltages such that the term V_p/V is greater than unity, as a the result of thermally pumping carriers injected at voltages below V_p. This allows some losses from the IQE and LEE to be recouped and enables ultra-high WPE, theoretically exceeding 100%.

A typical criticism for low current density LED operation is that output powers will be too low to be commercially relevant. However, applications for low-power light emitters already exist, for example for near-eye displays like Google Glass and for many indoor applications. Medium and high power sources can also be imagined that would employ large arrays of relatively dim but highly efficient LEDs. This has become more realistic as semiconductor material costs have dropped and the heat sink has emerged as the most expensive component of a modern LED package.

Both high power blue laser diode and low power blue LED sources will likely be employed in a diverse range of future applications. Both will circumvent modern challenges of high power LED efficiency droop, but will do so in their respective operating regimes. This dissertation discusses advances in epitaxy, device design, processing and packaging for high WPE III-N blue LEDs and LDs.

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Chapter 2. Effects of Surface Miscut on *m*-Plane Blue Emission

2.1. Advantages of Nonpolar GaN

The nonpolar *m*-plane of GaN has several intrinsic advantages over *c*-plane. The *m*-plane is free from internal polarization-related electric fields and the deleterious quantum-confined Stark effect, which reduces the carrier wavefunction overlap in *c*-plane quantum wells (QWs) and necessitates narrow QWs (< 3 nm) for satisfactory radiative recombination rates.[1] In contrast, InGaN *m*-plane QWs may be grown as thick as the critical thickness limit for dislocation glide on inclined *m*-planes or other pyramid planes.[2] Thick QWs reduce the carrier density and, consequently, the Auger recombination rate, which in turn reduces efficiency droop.[3,4]

An additional advantage of InGaN QWs on *m*-plane is the unbalanced biaxial compressive stress which breaks the VB degeneracy and results in the top two VBs having dipole character in the plane of the QW. The energy splitting between the VBs increases with indium content due to the increasing compressive stress within the layer and results in reduced hole effective masses, polarized light emission, and anisotropic material gain in the active region.[5,6] Edge-emitting LDs on *m*-plane can take advantage of the anisotropic material gain by orienting laser ridges parallel to the high gain *c*-axis. Hakki-Paoli measurements for such nonpolar blue LDs show higher differential modal gain than for *c*-plane blue LDs.[7]

Semipolar GaN planes, most notably, $(20\bar{2}\bar{1})$, already demonstrate high performance blue emission. Yet, a major disadvantage of $(20\bar{2}\bar{1})$ and other semipolar orientations of GaN is substrate cost and yield. Most semipolar planes are not naturally occurring during bulk

crystal growth,[8] and $(20\bar{2}\bar{1})$ bulk substrates must be formed by growing along the **c**-direction in a thick boule and then slicing and polishing, which results in small substrates and low boule yield.[9] Nonpolar *m*-plane, however, is a naturally occurring facet in bulk growth, enabling a viable future pathway to boules grown in the *m*-direction and, thus, to large area *m*-plane substrates.

2.2. Challenges in Nonpolar GaN Epitaxy

High performance violet LEDs and LDs on *m*-plane bulk substrates have been reported in literature,[10] but broad spectral emission for blue-emitting InGaN QWs, poor indium uptake, and stacking fault generation in green LEDs and LD structures currently hinder the progress for longer wavelength *m*-plane devices.

Poor spectral characteristics of *m*-plane LEDs and LDs in the blue spectrum include broad photoluminescence (PL) and electroluminescence (EL) emission that is sometimes composed of multiple peaks.[11,12] Some luminescence broadening is expected due to increasing alloy composition in the blue-emitting InGaN QWs and thermalization of higher energy VB states, but excessive broadening or multiple peaks have been attributed to various sources. These include increased occupation of localized states due to random indium fluctuations,[13] QW inhomogeneities,[14], for example, at dislocations[15], or larger-scale regions of variable In content and/or inherent morphological instabilities.[16] Work by Chichibu *et al.* has shown that morphological features and structural quality of the substrate and subsequent epilayer growth have a strong effect on the spectral characteristics of InGaN layers on nonpolar GaN, suggesting that reduced surface roughness may improve the emission quality and uniformity.[12]

Narrow spectral emission often signifies high compositional uniformity of InGaN layers and high crystal quality. Samples with narrow emission spectra also tend to give higher output powers (Fig. 2.1). For a laser diode, a narrower spontaneous spectral emission with a higher peak will lead to higher gain in the lasing mode and may reduce the lasing threshold.[17] Nonpolar *m*-plane has the highest calculated gain of any GaN crystal orientation,[14] so identifying the origin of the excessive luminescence broadening and resolving this issue for blue and longer wavelengths is expected to enhance nonpolar device performance and make it more competitive with the prevailing *c*-plane orientation devices.

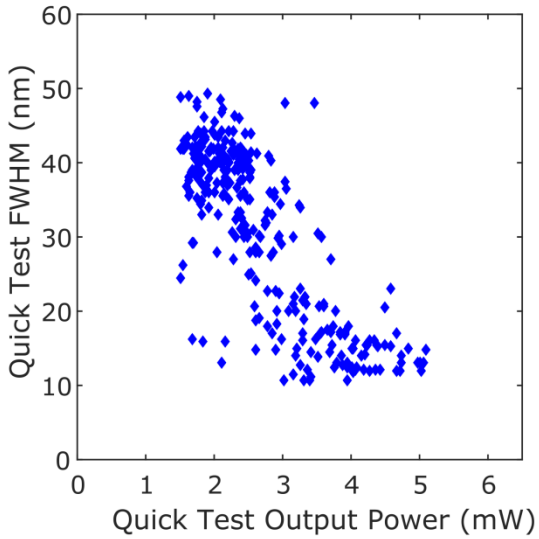

Figure 2.1. Correlation between the linewidth, measured as the full width at half maximum (FWHM) of the spectrum peak, and the output power for *m*-plane LEDs in the violet to cyan spectrum. "Quick test" refers to the EL measurement method in which indium contacts are pressed onto the top (p-contact) and side (n-contact) of the epitaxial wafer post-growth and the backside emission is measured by a silicon detector. The spectral information is collected the topside emission by an optical fiber connected to a Ocean Optics USB spectrometer. The measurements were taken at a current density J = 20 A/cm^2. The Pearson correlation coefficient of this data set is -0.80.

Co-loaded MOCVD growth studies have shown that *m*-plane GaN also suffers from reduced indium incorporation compared to QW structures on *c*-plane and semipolar planes.[18] Thus, InGaN QW and quantum barrier growth on *m*-plane GaN require lower

growth temperatures compared to *c*-plane and semipolar planes to incorporate sufficient indium for QW emission in the blue and green. Lower growth temperatures can lead to increased impurity uptake[19] and formation of defect states in MOCVD growth, including nonradiative centers in the quantum barrier layers.[20] Enhancing the indium uptake of *m*-plane InGaN would allow for higher growth temperatures and reduced point defect concentrations in the active region, which could improve the performance of longer wavelength devices.

2.3. Prior Work on the Impact of *m*-Plane Surface Miscut on Morphology

Early research on bulk *m*-plane substrates showed that the surface morphology is highly sensitive to growth conditions and substrate orientation. The first *m*-plane homoepitaxy by MOCVD on low-dislocation density on-axis bulk substrates exhibited four-sided pyramidal hillock growth. The hillocks results from spiral growth around pinned steps at pre-existing TDs. The pyramidal faces of the hillocks are oriented along principle crystal directions with two *a*-oriented vicinal faces inclined toward the $[11\bar{2}0]$ (**a**) crystal direction, and two *c*-oriented vicinal faces inclined toward $[0001]$ (+**c**) and $[000\bar{1}]$ (–**c**) crystal directions.

These pyramidal faces exhibit distinct step-terrace structures with step heights of approximately 1 monolayer (ML).[21] Fig. 2.2 shows an atomic force microscopy (AFM) image of a typical pyramidal hillock formed during 100 nm of homoepitaxial, unintentionally doped, GaN growth on a nominally on-axis, low defect density, bulk *m*-plane substrate. A single pyramid is outlined to guide the eye and delineate the different facets. Note that straight steps are visible on the *a*-faces of the pyramid in Fig. 2.2 (b) but not the +/–*c*-faces

of the pyramid due to resolution limits of the measurement as well as the AFM scan direction.

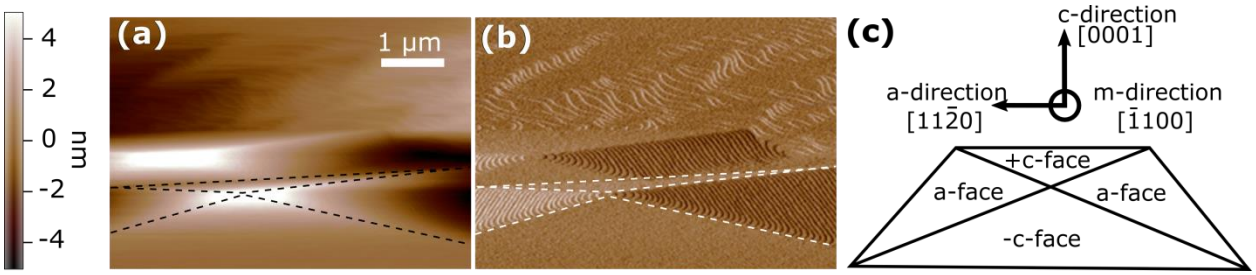

Figure 2.2. AFM (a) height and (b) amplitude image of pyramidal GaN growth on a nominally on-axis bulk *m*-plane substrate. The nomenclature of the four faces of the pyramid is illustrated in (c). Adapted from [22] with permission.

Atomic force microscopy (AFM) revealed that the *c*-oriented faces of the pyramid have a higher step density and larger slope angles than the *a*-oriented faces, with the +*c*-oriented face having the highest step density. [23] Although originating from TDs of the underlying substrate, the size and density of the hillock pyramids has some dependence on MOCVD growth conditions of the GaN template, such as the use of H_2 or N_2 carrier gas.[24]

Intentional miscut of the bulk *m*-plane GaN substrate in small angles toward the **-c**-direction or **a**-direction promote step flow growth which outcompetes spiral growth, resulting in hillock-free surfaces.[21,23] A substrate miscut of –1° toward [0001] (equivalently stated as 1° toward [000$\bar{1}$]) became the *m*-plane "standard" miscut at UCSB.[21,25,26] This miscut is referred to as the "–1° **c**-miscut" for brevity.

LD devices grown on -1° **c**-miscut substrates showed narrower PL emission, more uniform device performance, and higher device yield compared to devices grown on co-loaded on-axis substrates.[26] The high average threshold current densities of the LDs on the

on-axis substrates with pyramidal surface features were attributed to broad spectral emission and compositional non-uniformities of the InGaN layers leading to reduced gain.

2.4. Emission Characteristics of InGaN SQWs on Miscut *m*-Plane

The –1° **c**-miscut suppresses hillock formation on *m*-plane and improves LD performance compared to devices grown on on-axis *m*-plane. However, even the -1° **c**-miscut *m*-plane still exhibits low indium uptake[18] and broad luminescence linewidth in the blue spectrum compared to *c*-plane (Fig. 2.3).[11,22,27]

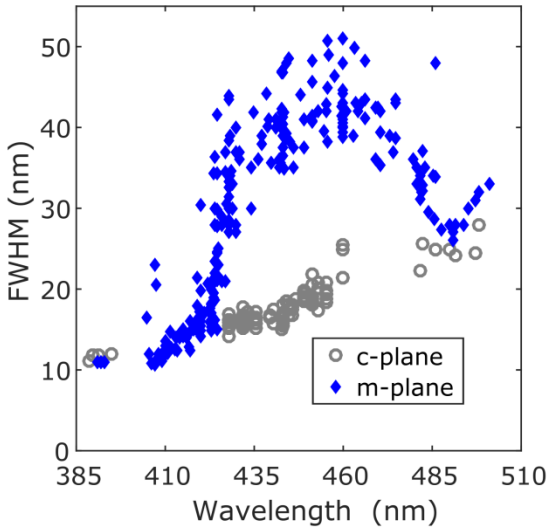

Figure 2.3. Quick Test EL linewidth (FWHM) vs. wavelength for *c*-plane and –1° **c**-miscut *m*-plane samples. Linewidths at 450 nm (blue emission) for *m*-plane often exceed 40 nm, whereas *c*-plane has linewidths ~ 20 nm at the same wavelength.

We aimed to understand the impact of small angle substrate on the emission wavelength and linewidth for nominally *m*-plane InGaN single quantum wells (SQWs). All growths in this study used bulk *m*-plane substrates provided by Mitsubishi Chemical Corporation (MCC) with a TD density on the order of 5 x 10^6 cm^{-2}.[9] Growths were performed by MOCVD at atmospheric pressure with V/III ratios in excess of 3000 and in N_2

carrier gas.[24] The epitaxy consisted of an unintentionally doped (UID) GaN template layer approximately 1.9 μm thick, grown with trimethylgallium (TMG) and ammonia (NH_3) precursors at a growth rate ~8 Å/s and susceptor temperatures ranging 1020 to 1100 °C. The template was followed by a 20 nm UID GaN barrier grown in triethylgallium (TEG), and InGaN SQW ~7 nm thick, grown using TEG and trimethylindium (TMI) precursors at temperatures ranging 775 to 795 °C, capped with a ~4 nm UID GaN barrier layer in TEG. All growths were co-loaded and grown simultaneously on nominally on-axis bulk substrates, -1° **c**-miscut substrates and 0.5° toward the $[11\bar{2}0]$ **a**-direction (referred to as 0.5° **a**-miscut for brevity).

Morphology was analyzed using optical microscopy with a Nomarski filter and polarizer for contrast and atomic force microscopy (AFM) with 20 μm × 20 μm scan areas. Emission characteristics were characterized by room temperature photoluminescence (PL), using excitation from a He-Cd laser line at 325 nm and monochromatic cathodoluminescence (Mono-CL) using a Gatan MonoCL4 system with spot size of 3 μm and acceleration voltage of 5 kV.

2.4.1. Surface Morphology

Optical microscope (OM) images are shown in Fig. 2.4 (a)-(c) for SQW samples grown on three *m*-plane miscut substrate orientations: (a) on-axis *m*-plane, (b) -1° **c**-miscut, and (c) 0.5° **a**-miscut. The on-axis sample showed a high density of shallow pyramidal hillock features elongated along the **a**-direction, similar in shape and density to those found in previous studies under similar growth conditions.[21,23] Both miscut samples showed relatively smooth surfaces in OM, free from pyramidal hillock features. The substrate with

miscut toward the **a**-direction also displayed some sparse pit-like features, visible in Fig. 2.4 (c).

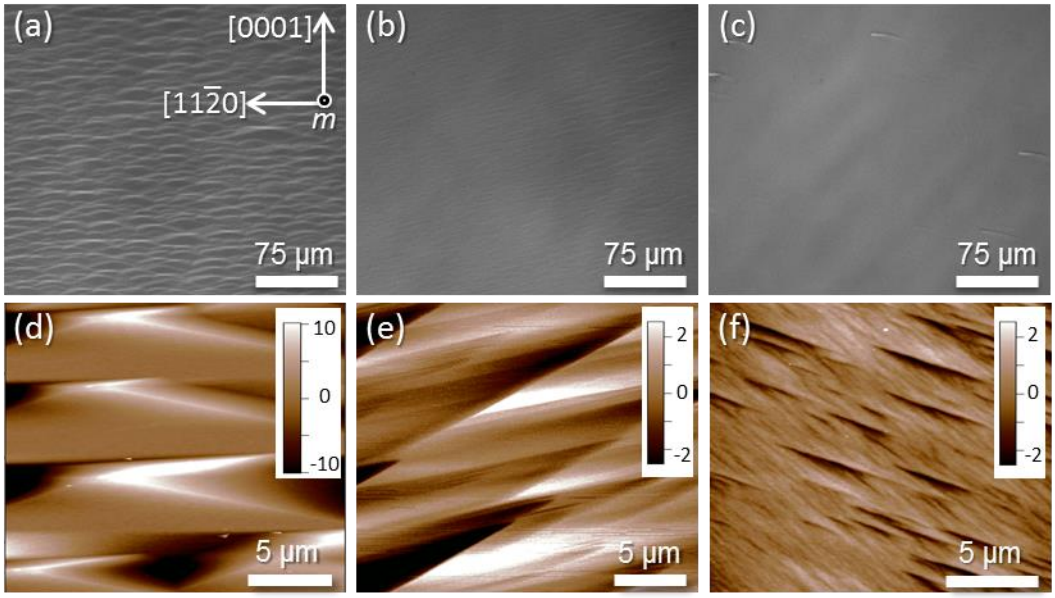

Figure 2.4. Optical microscope images taken with a Nomarski filter for SQW samples grown on *m*-plane substrates oriented nominally (a)on-axis, (b) -1º **c**-miscut, and (c) 0.5º **a**-miscut. AFM height retrace images for substrates orientated (d) nominally on-axis *m*-plane, (e) -1º **c**-miscut, and (f) 0.5º **a**-miscut. Height scales are in nm. Note the difference in height scale bars for (d) versus (e) and (f). Adapted from [11] with permission.

Height retrace images by AFM are shown in Fig. 2.4 (d)-(f) for the on-axis, -1° **c**-miscut, and 0.5° **a**-miscut, respectively. The height of the pyramidal hillock features on the on-axis sample exceeds 20 nm. Diagonal striated features were visible in AFM scans for both miscut samples, with RMS roughness values ranging from 0.3 nm and 2 nm depending on location of the scan.

2.4.2. SQW Emission Properties

Photoluminescence (PL) spectra for the on-axis, -1° **c**-miscut, and 0.5° **a**-miscut *m*-plane samples are plotted on a log scale in Fig. 2.5. The peak wavelength of the on-axis

sample was 424 nm with a secondary PL peak at 480 nm. The spectrum had an overall linewidth FWHM = 25 nm. The -1° **c**-miscut sample had a similar peak emission at 423 nm, but a narrower FWHM = 20 nm, correlating with previous studies that showed improved spectral emission uniformity on miscut *m*-plane substrates.[26] The 0.5° **a**-miscut sample emitted at a longer peak wavelength of 467 nm, indicating increased In incorporation on this miscut. The spectrum had a secondary peak at 428 nm and a broad FWHM = 38 nm.

The width of the dominant, longer wavelength spectral peak of the 0.5° **a**-miscut sample was attributed to the typical broadening often observed for *m*-plane QWs in the blue spectrum (Fig. 2.3).

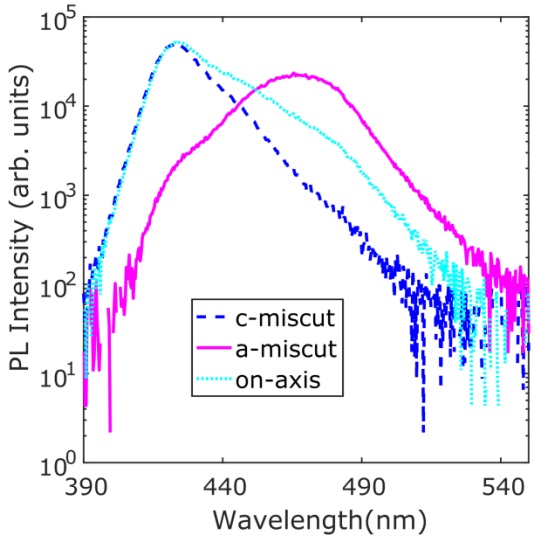

Figure 2.5. Room temperature PL with a 325 nm HeCd excitation source for SQW samples grown on on-axis, -1° **c**-miscut, and 0.5°-**a**-miscut *m*-plane substrates. Note the secondary emission peaks visible on the on-axis and **a**-miscut samples. Adapted from [11] with permission.

Mono-CL images were taken for the three samples at wavelengths of 425 nm (Fig. 2.6 (a)-(c)) and 465 nm (Fig. 2.6 (d)-(f)). For the on-axis sample, the pyramidal hillock features were clearly visible. The +/-*c*-oriented faces of the pyramidal hillocks dominated

emission at the shorter 425 nm wavelength (Fig. 2.6 (a)), while the *a*-oriented vicinal faces dominated emission at the longer 465 nm wavelength (Fig. 2.6 (d)). This suggests that the dual peaked emission shown in Fig. 2.5 can be attributed to vicinal surfaces with different emission wavelengths that appear on morphological features.

The -1° **c**-miscut sample emitted at 425 nm in mono-CL (Fig. 2.6 (b)), consistent with the peak PL emission (Fig. 2.5). However, this sample also has diagonal striations emitting at 465 nm, shown in Fig. 2.6 (e), which could be the cause of the shoulder in the PL spectrum.

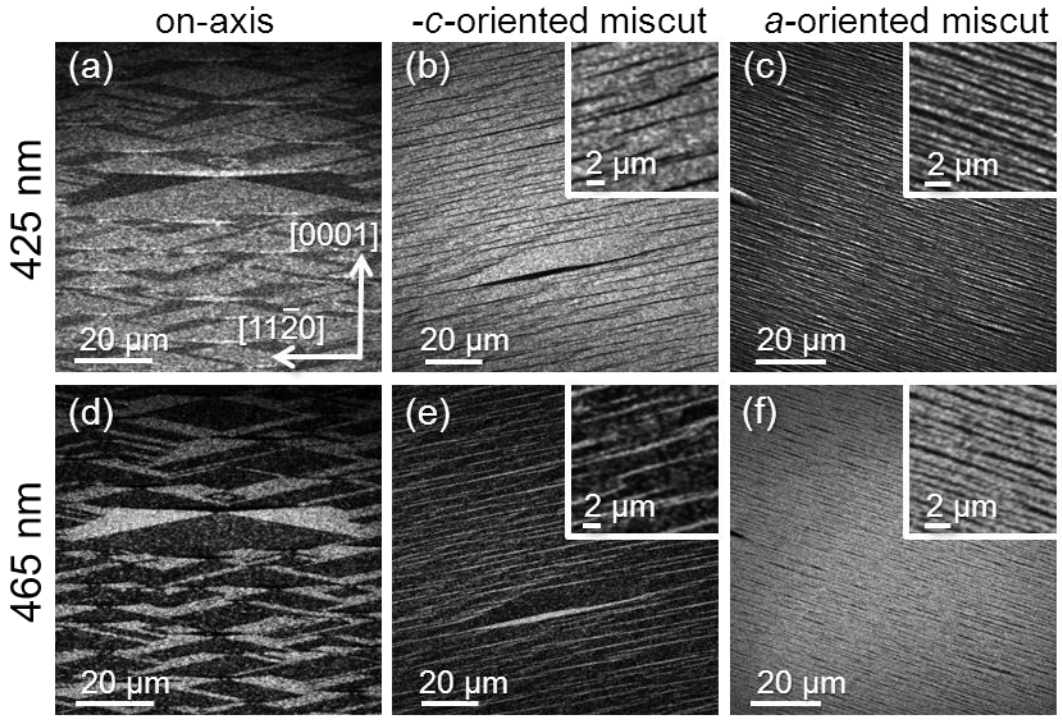

Figure 2.6. Mono-CL images at a center wavelength of 425 nm for co-loaded SQW growths on (a) on-axis, (b) -1° **c**-miscut, and (c) 0.5° **a**-miscut *m*-plane substrates. Mono-CL images with a center wavelength of 465 nm are shown in (d) -(f), respectively. Higher magnification images are shown in the insets of the miscut samples. Reprinted from [11] with permission.

The SQW on the 0.5° **a**-miscut appeared brighter in the longer wavelength 465 nm mono-CL image than the 425 nm image (Fig. 2.6 (f)), which is consistent with its PL emission peak of 467 nm (Fig. 2.5). This sample also had small striated features emitting at

425 nm, as shown in Fig. 2.6 (c), which may cause the short wavelength shoulder in the PL spectra.

2.4.3. Discussion

These growth series demonstrate that small changes in miscut angle of bulk *m*-plane substrates can have a large impact on morphology, emission wavelength, and spectral shape. The pyramidal hillock features of the on-axis *m*-plane substrates showed distinctive differences in Mono-CL emission wavelength on the **a**-oriented and **c**-oriented faces, leading to dual wavelength emission, apparent in the PL spectra. This suggests that consequences of surface miscut, including the step density (a function of the miscut magnitude) or the step-edge orientation (a function of the miscut direction) could impact the In incorporation.

The emission from regions with similar step orientations are similar despite expected differences in terrace width spacing with increasing substrate miscut. The SQW emission wavelength on -1° **c**-miscut substrates was found to correlate with the emission wavelength from the -*c*-faces of the on-axis pyramidal hillocks. This is true despite the higher expected step density on the intentionally miscut surface. Likewise, SQW emission wavelength from the 0.5° **a**-miscut correlates with that of the *a*-faces of the on-axis pyramidal hillocks. Thus, the data suggests that the step-edge orientation has a greater impact on the resulting emission characteristics than the step density. Vicinal steps on *m*-plane GaN are highly anisotropic due the wurtzite crystal structure, which may impact growth kinetics and In incorporation efficiencies at exposed step edges of different orientations.[28]

2.5. Stable Vicinal Step Orientations of *m*-Plane GaN

In the SQW study discussed in section 2.5, both the -1° **c**-miscut and the 0.5° **a**-miscut fully suppressed the pyramidal hillock formation, however they still exhibited diagonal striations that were visible in AFM. These striations were associated with non-uniformities in indium incorporation, visible in monochromatic cathodoluminescence imaging, which also resulted in broad PL emission for both miscut orientations.[11] That study is now taken further to understand the morphological evolution and step structure of *m*-plane homoepitaxial films grown on co-loaded bulk substrates with orientations nominally on-axis, -1° **c**-miscut, and 1° **a**-miscut.

All growths in this study were performed by atmospheric pressure MOCVD on bulk *m*-plane GaN substrates from MCC. Three miscut orientations were co-loaded: nominally on-axis, -1° **c**-miscut, and 1° **a**-miscut. Actual miscuts in the (**c**, **a**) directions were (-0.21°, 0.04°), (-0.87°, 0.01°), and (-0.26°, 1.01°), respectively. In separate studies, the vendor specific miscut was verified with high resolution X-ray diffraction (typically within 0.01° of the specified value).[29]

Unintentionally doped (UID) homoepitaxial GaN template layers were grown with standard growth conditions in N_2 carrier gas,[24] with TMG and NH_3 as group III and V precursors, respectively, and at a susceptor temperature of 1100 °C. The templates were grown for four different times to study the morphological evolution: 30 seconds, 2 minutes, 10 minutes and 39 minutes. These times correspond to layer thicknesses of approximately: 25 nm; 100 nm; 500 nm; and 2 μm, respectively, based on growth rates estimated from separately grown samples measured by X-ray diffraction.

The surface morphology for each sample was analyzed with an Asylum MFP-3D AFM in tapping mode with scan sizes ranging from 0.64 μm^2 to 900 μm^2. Height images are included, which map the changes in AFM tip height across the sample, a measure of surface morphology. Amplitude images are also included, which map the magnitude of deflection in the AFM tip as it interacts with the surface, as this more clearly shows the vicinal step features.[30]

2.5.1. Template Evolution of On-Axis *m*-Plane

The morphological evolution of UID GaN template layers grown on nominally on-axis *m*-plane substrates are shown in Fig. 2.7. These images show the evolution of characteristic spiral hillock features for increasing GaN thickness.

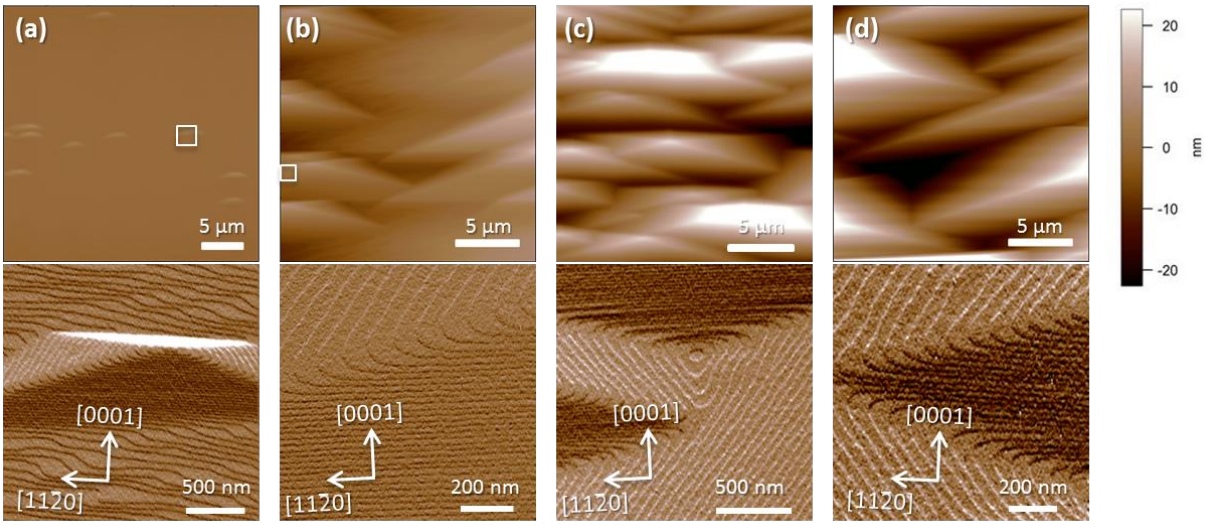

Figure 2.7. AFM images for homoepitaxy on nominally on-axis *m*-plane substrates. The upper panels show large area (400-900 μm^2) height images for film thicknesses of approximately (a) 25 nm, (b) 100 nm, (c) 500 nm, and (d) 2 µm. The lower panels show small area (1-4 μm^2) amplitude images of (a) early hillock formation for 25 nm film; (b) detail of the *a*- and -*c*-face edges of a pyramid for 100 nm thick film, (c) defect-free depression between hillocks for 500 nm thick film, and (d) intersection of *a*- and –*c*-faces. Reprinted from[22] with permission.

Figure 2.7 (a) captures the beginning of hillock formation after 30 seconds of GaN template growth. The hillock density in this AFM image is ~$6x10^5$ cm^{-2}, which is the same order of magnitude as the reported TD density of the bulk *m*-plane substrates.[31] The approximate dimensions of the hillocks at this stage are 5 nm tall, 3 μm wide in the **a**-direction and 1 μm wide in the **c**-direction. The RMS roughness of the hillock-free areas of the surface is 0.5 nm and is composed of meandering steps with line directions approximately along the **a**-axis, where the line direction is defined as parallel to the step edge. The lower panel of Fig. 2.7 (a) shows that the hillock-free surface exhibits regions where the step orientation has mixed **a**- and +/–**c**-components of the line direction (henceforth described as *a*+*c* or *a*–*c* step directions), where the **a**- and **c**- components are not necessarily equal in magnitude

The preferred vicinal step orientation on the –*c*-face is the **a**-direction as expected, but the *a*-faces appear to prefer step direction with **a** and **c** components, rather than a pure **c**-direction steps. The steps on the *a*-faces have an *a*+*c* step direction, oriented approximately 40° from the **c**-axis. The angle of the *a*-face steps corresponds to a ratio of approximately 1.25 for the **a**-component to the **c**-component of the line direction. Steps on the *a*-faces are straight with evenly spaced terrace widths, indicating stable step flow in this *a*+*c* direction.

For thicker template layers, the hillocks grow larger and the aspect ratio of the hillocks remains unchanged. After two minutes (~100 nm) of growth, the hillocks expand to nearly 20 μm in length in the **a**-direction, as shown in Fig. 2.7 (b). AFM line scans (not shown), give average terrace widths of the *a*-face and –*c*-face steps of approximately 80 nm and 25 nm, respectively, and the approximate slope angles are 0.2° and 0.5°, respectively.

The step orientations are shown in more detail in the lower half of Fig. 2.7 (b), which highlights the *a*-face (top) and –*c*-face (bottom) of a hillock feature.

The sample surface exhibits laterally separated regions of *a*-faces with wide terrace widths and shallow slope angles, and +/–*c*-faces with short terrace widths and steeper slope angles. The intersections of *a*-face and *c*-face steps between hillocks form defect-free triangular depressions, shown in the small area (1 - 4 μm^2) scans of Fig. 2.7 (c) and (d). These results indicate that the relative step orientations and terrace widths on the hillock faces remain stable throughout film growth.

2.5.2. Template Evolution of -1° c-miscut *m*-plane

Previous studies demonstrated that vicinal step flow resulting from a -1° **c**-miscut suppresses formation of the pyramidal hillocks that are characteristic of on-axis *m*-plane homoepitaxial growth.[21,23] Despite the absence of pyramids, the emission spectrum from InGaN QWs grown on this miscut can still exhibit broad linewidth, sometimes double-peaked, in the blue spectrum. The emission characteristics have been at least partially attributed to variable indium incorporation at shallow diagonal striations that emerge in template growth, as discussed in Section 2.4.[11]

Here, we describe the morphological evolution of diagonal striations in homoepitaxial UID GaN template layers grown on -1° **c**-miscut *m*-plane substrates (Fig. 2.8).

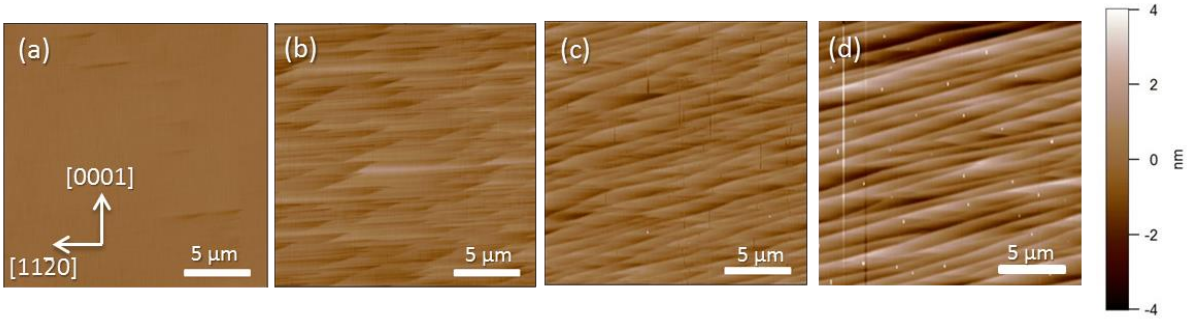

Figure 2.8. Large area (400 µm^2) AFM height images of GaN grown on -1° **c**-miscut substrates with nominal film thicknesses of (a) 25 nm, (b) 100 nm, (c) 500 nm, and (d) 2 µm. Shallow grooves in the thin film (a) propagate into diagonal striations in the thicker films (b)-(d). Reprinted from[22] with permission.

Thin template growths (Fig. 2.8 (a)) exhibit shallow disperse grooves. In thicker films, diagonal striations appear on the surface, as shown in Fig. 2.8 (b)-(d). The RMS roughness of the 2 µm template in Fig. 2.8(d) was 1.23 nm for a 900 µm^2 scan. Smaller area AFM images (~40 µm^2) reveal that the diagonal striations are composed of thin kinked regions of the step flow with monolayer high steps with an *a+c* line direction. On the remainder of the surface, however, the steps have an **a**-direction (Fig. 2.9). Extrinsic perturbations at the substrate surface such as defects, impurities or roughness may be responsible for the nucleation of striations.

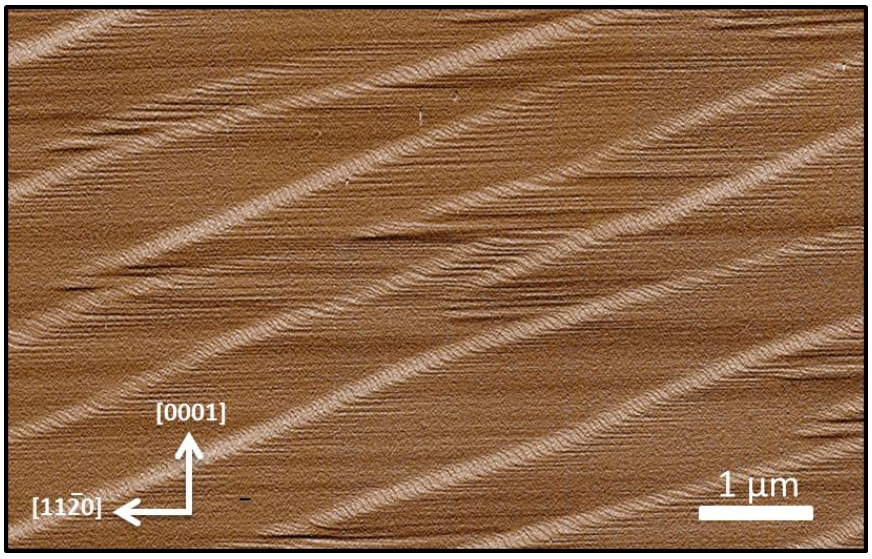

Figure 2.9. Amplitude AFM image of the surface morphology showing striations after approximately 100 nm of growth on -1° **c**-miscut *m*-plane substrates. Reprinted from[22] with permission.

Typically, a step flow region with high curvature, such as one of these striated regions, will straighten out as growth proceeds due to the line tension in the step. However, these striations appear to propagate over the substrate surface without straightening for thicker films, forming elongated regions where the steps align in an *a*+*c* orientation as shown in Fig. 2.9. The striations may be stabilized by a stable *a*+*c* step orientation.

Stable progression of striations is also shown for templates grown on similar substrate miscuts under different growth conditions, which reveal the presence of 'frustrated spirals'. A frustrated spiral is formed by the initiation of a spiral ramp at a TD. The presence of vicinal step flow prevents the spiral from making a full revolution, which suppresses the formation of complete spirals. The frustrated spiral, however, may be the origin of mixed orientation steps as shown in Fig. 2.10 (note that the sample in Fig. 2.10 (a) was grown in 3 sccm of TMGa for 4.7 minutes at 1000 °C and the sample in Fig. 2.10 (b), was grown in 7 sccm of TMGa for 2 minutes at 1050 °C – these conditions differ slightly from other samples reported in this work).

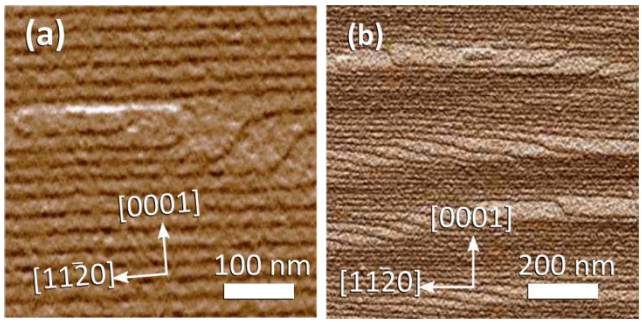

Figure 2.10. Small area (1 - 4 μm^2) amplitude AFM images for thin homoepitaxial template layers grown on -1° **c**-miscut *m*-plane bulk substrates, capturing (a) frustrated spiral formation and (b) regions of kinked steps. Reprinted from[22] with permission.

The AFM scan in Fig. 2.10 (a) captures the formation of a frustrated spiral. While parallel steps in the **a**-direction cover most of the sample, a perturbation caused by the frustrated spiral can disrupt the step direction and cause a kink in the step that can propagate over the substrate surface, as shown in Fig. 2.10 (b). The diagonal striations due to a frustrated spiral might be mitigated with increased miscut angle in the **-c**-direction, which should narrow the terrace spacing between steps along the **c**-axis and prevent the spiral from initiating.[23] Striations caused by other surface perturbations might be mitigated by optimized growth conditions.

2.5.3. Template evolution of 1° a-miscut *m*-plane

Pyramidal hillocks on *m*-plane GaN may also be suppressed by small miscuts toward the **a**-direction, as previous growth studies have found. AFM images of the morphological evolution of GaN template layers grown on nominally 1° **a**-miscut substrates are shown in Fig. 2.11.

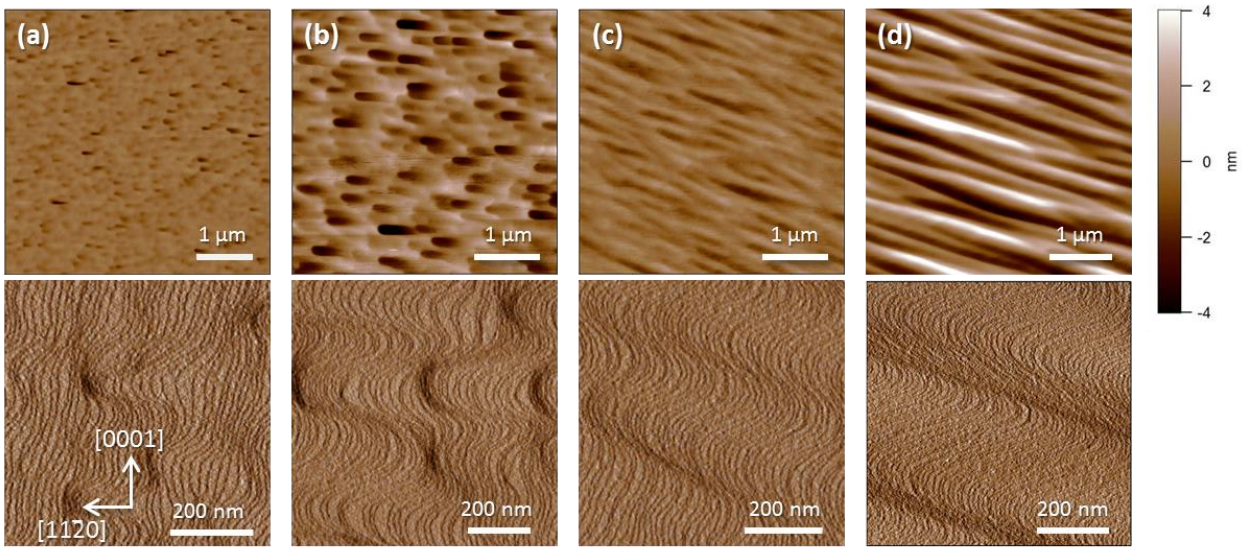

Figure 2.11. AFM images of the morphological evolution of homoepitaxial growth on 1° **a**-miscut substrates for approximate film thicknesses: (a) 25 nm, (b) 100 nm, (c) 500 nm, and (d) 2 µm. The upper panels show 25 μm^2 height images, and the lower panels show 0.64 μm^2 amplitude images, which more clearly reveal the step structure in each sample. Reprinted from[22] with permission.

For the shortest growth time of 30 seconds,, the surface exhibits shallow depressions on the surface (Fig. 2.11 (a)). The lower panel of Fig. 2.11 (a) shows that the vicinal steps have a meandering profile, with some areas of step-bunching. For thicker GaN layers, the depressions become larger (Fig. 2.11 (b)) and give way to diagonal striations, as shown in Fig. 2.11 (c) and (d). The amplitude images reveal that the steps are not parallel to the **c**-direction, but instead appear to favor the *a*+*c* direction or *a*–*c* direction. These S-shaped steps align together to form diagonal striations visible in thicker films (Fig. 2.11 (c-d)). The RMS roughness for a 0.64 μm^2 scan size increases from 0.36 nm to 1.74 nm for the 25 nm thick film and the 2 µm thick film, respectively. As was the case for –**c**-miscuts, **a**-miscut samples with diagonal striations lead to broad spectral emission due to differences in indium incorporation along differently oriented steps.[11]

These data demonstrate that **c**-direction steps are unstable and the meandering steps may result from the decomposition of **c**-direction steps into components of *a*+*c* and *a*–*c* directions, which have longer step length, but apparently lower energy. This observation is consistent with the observations on both on-axis and –**c**-miscut *m*-plane, which appear to favor the formation of steps in *a*±*c* directions over formation of pure **c**-direction steps. Pure **c**-direction steps have not yet been observed for any miscut or growth condition in our studies.

Unlike **–c**-miscut *m*-plane, for which the diagonal striations might be mitigated with increased miscut or improved growth conditions, these results indicate that pure **a-**miscut *m*-plane will always lead to homoepitaxial surfaces with mixed step orientations and high surface roughness.

2.5.4. Discussion

Broad spectral emission of blue-emitting QW structures on *m*-plane GaN was tied to progression of vicinal steps of the underlying template layers.[11,22] Miscut direction and magnitude as well as template growth conditions determine the overall vicinal step orientation and progression. Step orientation (i.e. miscut direction) is proposed to play a larger role in emission wavelength than step spacing (i.e. miscut magnitude) because miscut samples with very different terrace widths yet similar step orientations maintain approximately the same peak emission wavelengths as the on-axis samples.[11]

Steps oriented in the *a*+*c* direction appear naturally in lieu of **c**-direction steps on all three substrate miscuts: (1) on the *a*-faces of on-axis pyramidal hillock features, (2) propagating in striations generated from surface perturbations in –**c**-miscuts, and (3) in

meandering step flow for **a**-miscuts, which decompose **c**-direction steps into a combination of *a*±*c* and *a*–*c* direction steps. These regions with *a*±*c* orientation are also associated with longer wavelength emission,[11] indicating higher indium incorporation. This suggests that we may take advantage of the natural *a*±*c* step direction by intentionally miscutting substrates in this orientation.

2.6. Morphology and Electroluminescence of LEDs on "Double Miscut" *m*-Plane Substrates

In the last sections, it was shown that double-peaked PL on -1° **c**-miscut *m*-plane could be attributed to the striated template morphology. The striated regions exhibited longer wavelength emission than the rest of the field, and were composed of diagonal step flow with an "*a*±*c*" step direction.[22] It was proposed that the *a*±*c* direction steps are more stable and have higher indium uptake.[11,22]

Here, MOCVD epitaxy is examined on *m*-plane substrates that are intentionally miscut along both the **a**- and the **c**-direction ("double miscuts"). The purpose of this investigation is to replicate the stable step flow growth and longer emission wavelength exhibited on a+c oriented steps that were observed on morphological features on other *m*-plane surfaces. With an intentional double miscut, we aim to control the direction and density of the step flow to achieve smooth, featureless films with long emission wavelength and narrow emission linewidth.

MOCVD growth on "double miscut" bulk *m*-plane substrates is compared to -1° **c**-miscut bulk *m*-plane substrates. We discuss the relationship between surface morphology, indium uptake, linewidth, and peak output power, which are all improved with double miscut substrates. The previous study is extended to examine the EL characteristics,

and we discuss the repeatability of these characteristics and their implications for LED and LD devices.

All growths in this study were performed by atmospheric pressure MOCVD. The gallium precursor for high temperature (950 - 1150 °C) n-GaN (~5.4 Å/s) and p-GaN (950 - 980 °C) (~2.5 Å/s) was trimethylgallium (TMGa). Triethylgallium was used for low temperature (790 - 885 °C) GaN (~0.3 Å/s), InGaN (~0.4 - 0.7 Å/s) and AlGaN layers (850 - 950 °C) (~0.6 Å/s). Trimethylindium and trimethylaluminum were used for the indium and aluminum precursors, respectively. Growths were performed on the following miscuts: -1° **c**-miscut, double miscut with 1.49° toward [0001] and 2.01° toward [$11\bar{2}0$] (hereafter denoted, (1.49° **c**, 2.01° **a**)), and double miscut with 0.21° toward [0001] and 0.51° toward [$11\bar{2}0$] (hereafter denoted (0.21° **c**, 0.51° **a**)).

The homoepitaxy morphology was compared for a -1° **c**-miscut substrate and the small angle double miscut (0.21° **c**, 0.51° **a**) substrate, which were co-loaded in the MOCVD reactor. The samples were grown at 1100 °C in TMGa and N_2 carrier gas to thicknesses of ~100 nm. An Asylum MFP-3D atomic force microscope (AFM) was used in tapping mode to study surface morphology. The small angle double miscut was used for the AFM comparison due to the limits of the AFM, which cannot resolve the shorter terrace widths associated with larger miscut angles. Apart from the AFM analysis, all double miscut substrates reported in this study were of angle (1.49° **c**, 2.01° **a**). In initial comparisons with several miscut angles (not shown), the (1.49° **c**, 2.01° **a**) double miscut yielded the highest output power and narrowest linewidth and was therefore selected for further study.

Samples for comparison of EL characteristics included LED and LD epitaxial structures employing one to three QWs with widths of 4 – 12 nm and QBs with widths of 8 –

16 nm. LD epitaxial structures included n- and p-side $In_{0.07}Ga_{0.93}N$ waveguiding layers. Approximately 70% of the samples included a p-$Al_{0.2}Ga_{0.8}N$ electron blocking layer adjacent to the active region. Typical EL output powers in blue for this configuration were 1.5 – 2.5 mW, and samples emitting less than 1.25 mW were omitted from the analysis (omissions constituted ~15% of the raw data set).

EL measurements were performed on-wafer at 20 A/cm^2 by probing 0.1 mm^2 indium p-contacts. Side n-contacts were formed by soldering indium to the wafer edge. Spectral information was collected using a USB Ocean Optics Spectrometer (2 nm resolution), and relative power was collected from the backside of the wafers with a Si photodiode.

2.6.1. Morphology of Double Miscut Homoepitaxy

Figure 2.12 shows a comparison of the homoepitaxial morphology on co-loaded -1° **c**-miscut and (0.21° **c**, 0.51° **a**) double miscut *m*-plane substrates. As previously described,[22] homoepitaxial growth on the -1° **c**-miscut surface exhibited diagonal striations composed of *a+c* oriented steps, while the rest of the field exhibited steps with line direction along the **a**-axis. Fig. 2.12 (a) shows one such striation. Steps remained monolayer height in the striated region with terrace widths averaging 40 nm, compared to terrace widths <15 nm for the **a**-direction steps on the remainder of the film.

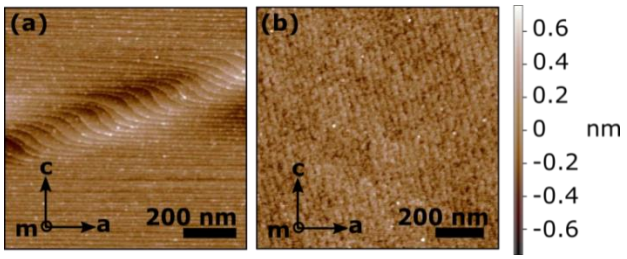

Figure 2.12. AFM images of co-loaded ~100 nm homoepitaxy for (a) -1° **c**-miscut showing a striation composed of steps with a+c direction, and (b) double miscut (0.21° **c**, 0.51° **a**), showing a+c direction step flow growth. Reprinted from [32] with permission.

The co-loaded homoepitaxy on the (0.21° **c**, 0.51° **a**) double miscut substrate in Fig. 2.12 (b) exhibited stable step flow growth in an *a*+*c* direction with straight step edges and constant terrace widths of ~27 nm. The uniformity of the step structure indicates that it is possible to achieve stable growth along this orientation. No pyramidal hillocks were observed for the -1° **c**-miscut or any double miscut samples in this study.

All double miscut samples that were investigated in the course of this study showed some macroscopic eyelet pit defects (20 μm diameter, density ~10^6 cm^{-2}), which occurred during GaN growth and are tentatively attributed to extrinsic origin, such as contamination from substrate chemical mechanical polishing (Fig. 2.13). AFM images were taken in regions away from these pit defects.

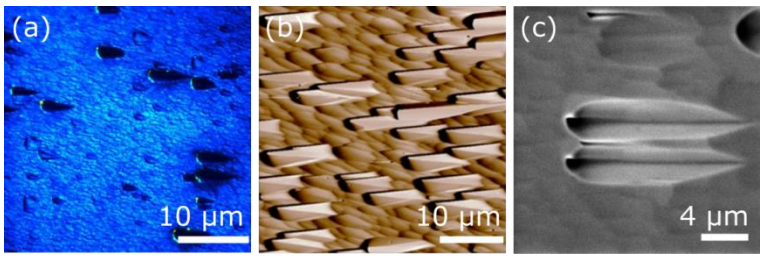

Figure 2.13. Images of eyelet defects on (1.49° **c**, 2.01° **a**) double miscut *m*-plane using (a) fluorimetry, (b) AFM, and (c) SEM.

Appendix A presents a more in-depth discussion of the dependence of eyelet size, shape, and density on the miscut angle, the growth conditions and the pre-growth surface preparation. Ultimately, eyelet densities were reduced by changing growth conditions, but were not completely eliminated for luminescing samples.

2.6.2. EL Wavelength of Double Miscut LEDs

Several co-loaded LED growths on -1° **c**-miscut and (1.49° **c**, 2.01° **a**) double miscut substrates were analyzed to determine the magnitude and reproducibility of the EL wavelength difference between the two samples. All samples for this comparison were triple QW LED structures with 5 nm QWs and 10 nm QBs.

In these co-loaded growths, the (1.49° **c**, 2.01° **a**) double miscut LEDs consistently showed longer wavelength emission in fluorescence, PL and EL measurements, despite run-to-run variations. Fig. 2.14 shows as much as a 38 nm EL wavelength shift between the -1° **c**-miscut and (1.49° **c**, 2.01° **a**) double miscut LEDs. The higher indium uptake on (1.49° **c**, 2.01° **a**) double miscut surfaces enables blue QW growth temperatures 10-20 °C hotter than for -1° **c**-miscut samples.

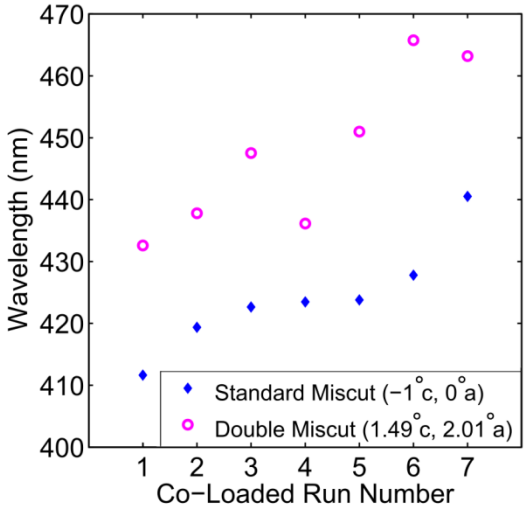

Figure 2.14. The EL wavelength shift is shown for seven separate co-loaded MQW LED growths of (1.49° **c**, 2.01° **a**) double miscut compared to -1° **c**-miscut substrates. Reprinted from [32] with permission.

2.6.3. EL Linewidth of Double Miscut LEDs

In addition to higher indium uptake, (1.49° **c**, 2.01° **a**) double miscut substrates also demonstrated narrower spontaneous EL emission in the blue spectrum. Fig. 2.15 shows a comparison of representative spontaneous EL spectra for double QW LD structures (12 nm QW, 15 nm QB) on -1° **c**-miscut and (1.49° **c**, 2.01° **a**) double miscut substrates. The two samples were grown separately to obtain the same peak wavelength, which was achieved by increasing the active region growth temperature for the (1.49° **c**, 2.01° **a**) double miscut (842 °C) compared to the -1° **c**-miscut (831 °C) substrate.

The peak wavelengths were 447 nm and 446 nm for the (1.49° **c**, 2.01° **a**) double miscut and -1° **c**-miscut, respectively. The -1° **c**-miscut had a FWHM of 44.9 nm, while the (1.49° **c**, 2.01° **a**) double miscut was much narrower at FWHM = 30.5 nm. Additionally, Fig. 2.15 shows that the double miscut spectrum was more symmetrical, lacking major secondary peaks or shoulders whereas the -1° **c**-miscut sample exhibited a high energy shoulder.

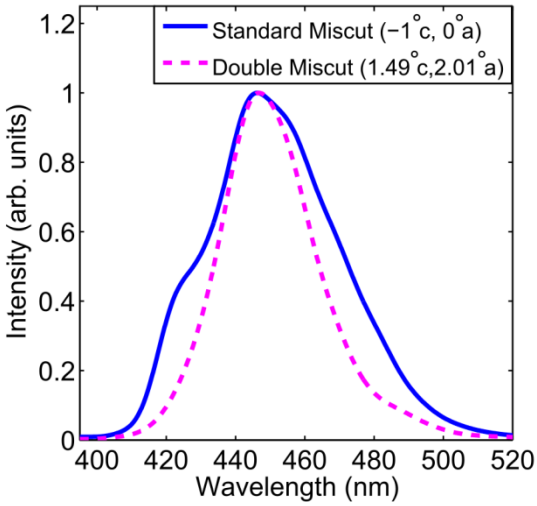

Figure 2.15. Comparison of separately grown blue LD structures shows narrow and symmetric EL lineshape for the (1.49° **c**, 2.01° **a**) double miscut (λ_{peak}=447 nm, FWHM=30.5 nm) compared to the -1° **c**-miscut (λ_{peak}=446 nm, FWHM=44.9 nm). Reprinted from [32] with permission.

Asymmetric lineshapes were observed for both SQW[11] and MQW[27] structures on -1° **c**-miscut *m*-plane. In both cases, local step features such as striations or step-bunching regions contributed to broadening or double-peaked emission by causing different surface regions to emit at different wavelengths. The improved lineshape for double miscut samples is attributed to their more uniform atomic step structure and absence of local step features that were shown on -1° **c**-miscut to lead to regions with different wavelength emission.

Additional sources of broadening that may affect both -1° **c**-miscut and double miscut samples include the effects of VB splitting, QW width fluctuations, and small-scale indium alloy fluctuations. VB splitting on *m*-plane results in two distinct energy transitions, where the measured separation is ~50 meV (10 nm) for 495 nm emitting *m*-plane QWs.[33] Width fluctuation effects on the energy levels were simulated using a commercial software package[34] and showed that monolayer fluctuations from a 5 nm, $In_{0.185}G_{0.815}N$ QW led to

<10 meV (1 nm) broadening. These contributions are relatively small compared to the *m*-plane linewidth, which is usually >200 meV (30 nm).

Ongoing studies are focused on understanding the origin of the remaining luminescence broadening. Previous near-field scanning optical microscopy studies on blue *m*-plane InGaN QWs grown on -1° **c**-miscut substrates show that the origin of the broad linewidth corresponds to features finer than the 100 nm lateral resolution of the technique.[16] Atom probe tomography studies on semipolar InGaN QWs[35] show that the indium composition follows a binomial distribution as expected for a random alloy. Preliminary work on *m*-plane InGaN QWs also shows no evidence of indium clustering beyond what is expected for a random alloy.[36]

Narrow linewidth EL for structures on (1.49° **c**, 2.01° **a**) double miscut substrates was consistent in many growths. Fig. 2.16 shows a plot of the FWHM of over 300 -1° **c**-miscut and (1.49° **c**, 2.01° **a**) double miscut samples as a function of wavelength. The -1° **c**-miscut samples exhibit narrow linewidth (10-20 nm) in violet (<420 nm), broadening to greater than 40 nm in blue (440 – 460 nm) and narrowing again in the cyan spectrum (>470 nm). At wavelengths beyond 490 nm, the onset of a high density of basal plane stacking faults (BPSFs) leads to a precipitous drop in output power for *m*-plane LEDs,[37,38] so only the range of 400 – 500 nm was explored. Preliminary evidence suggests that BPSFs are also a limitation for long wavelength double miscut *m*-plane. The cause of the narrowing of the FWHM at cyan wavelengths >470 nm and the impact of morphology throughout the wavelength range are topics of ongoing materials studies.

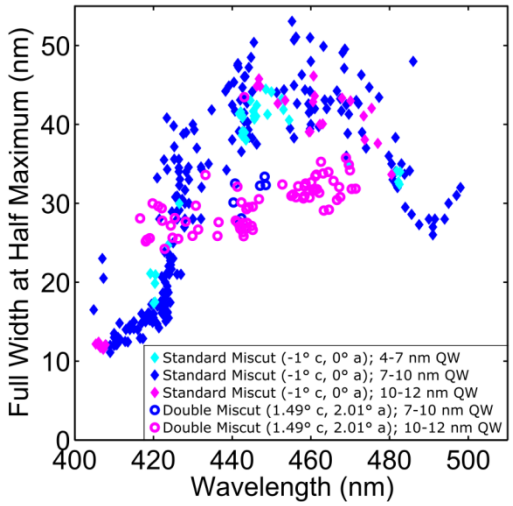

Figure 2.16. Spontaneous EL linewidth at 20 A/cm^2 for *m*-plane QW structures grown on -1° **c**-miscut and (1.49° **c**, 2.01° **a**) double miscut substrates. Reprinted from [32] with permission.

Figure 2.16 shows that the EL linewidths for the (1.49° **c**, 2.01° **a**) double miscut samples were often narrower by 10 – 15 nm, especially in the blue region (440 – 460 nm) where the -1° **c**-miscut samples are anomalously broad. In general, the EL linewidth comparisons are most accurate for wide QWs because the effect of monolayer thickness fluctuations is minimized as the QW width increases. Here, there was not a strong dependence of QW thickness on EL FWHM in the range of 4 – 12 nm QWs. There was also no strong dependence of the EL linewidth on QW number (plot not shown), likely due to the relatively thick QBs (8 – 16 nm) used throughout this study.[39] At wavelengths <420 nm, the -1° **c**-miscut showed narrower FWHM than the (1.49° **c**, 2.01° **a**) double miscut, which could be a result of the selection and optimization of the (1.49° **c**, 2.01° **a**) double miscut for the blue region, however, further characterization is needed.

Broad spontaneous emission spectra tend to lead to broad laser gain spectra. For instance, reported experimental gain spectra for *m*-plane LDs[7] follow the same linewidth

trend as shown in Fig. 2.16 for the spontaneous emission. Namely, for *m*-plane violet emission (λ ~ 405 nm), both the spontaneous emission and gain spectra are narrow, whereas for *m*-plane blue emission (λ ~ 450 nm), both the spontaneous emission and gain spectra are broad. We therefore expect that the narrower spontaneous emission linewidth achieved for (1.49° **c**, 2.01° **a**) double miscut samples in the blue spectrum should lead to a narrower gain spectrum.

2.6.4. EL Spectral Power Density of Double Miscut LEDs

Finally, Fig. 2.17 shows a comparison of the peak of the spectral power density for -1° **c**-miscut and (1.49° **c**, 2.01° **a**) double miscut samples in the blue spectrum as a function of the center wavelength. The integrated output power (collected by the Si photodiode) was multiplied by the normalized intensity spectrum (collected by the spectrometer) to give the spectral power density. Each data point represents the peak of the spectral power density curve for that sample.

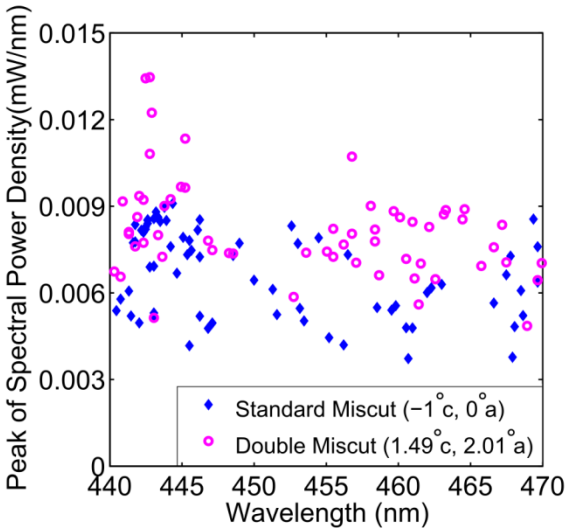

Figure 2.17. Higher peak powers are observed in the blue spectrum for (1.49° **c**, 2.01° **a**)double miscut than for -1° **c**-miscut samples. Reprinted from [32] with permission.

Figure 2.17 shows higher peak powers for (1.49° **c**, 2.01° **a**) double miscut than for -1° **c**-miscut samples in the blue spectrum. This is attributed to the improved step stability and narrower emission linewidth on double miscut substrates. In the simplified case of a normalized unimodal distribution, a narrower linewidth necessarily corresponds to a higher peak, which is demonstrated by Fig. 2.16 and Fig. 2.17. Higher peak power in the spontaneous emission should result in higher peak gain. This, along with a narrower gain spectrum, should lead to more efficient allocation of carriers to the primary lasing mode. We therefore anticipate lower threshold carrier densities for blue LDs grown on *m*-plane (1.49° **c**, 2.01° **a**) double miscut compared to -1° **c**-miscut substrates.

It was confirmed by AFM that MOCVD homoepitaxy on (0.21° **c**, 0.51° **a**) double miscut bulk *m*-plane GaN substrates leads to stable step flow growth. The *a*+*c* step direction that results from the double miscut leads to longer wavelength QW emission, indicating higher indium uptake. This step direction also leads to narrower EL emission in blue wavelengths compared to the -1° **c**-miscut. This is attributed to the stability of this naturally occurring step direction and the absence of step features that lead to non-uniform emission wavelength.[22] Finally, the (1.49° **c**, 2.01° **a**) double miscut samples show higher spontaneous emission power at the peak wavelength compared to the -1° **c**-miscut. This may lead to higher peak gain and lower threshold carrier densities for *m*-plane blue LDs on (1.49° **c**, 2.01° **a**) double miscut substrates.

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Chapter 3. Ray Tracing Simulations of Light Extraction Efficiency in Nitride LEDs

3.1. LED Light Extraction Efficiency

The direct conversion of electricity into light in semiconductor light emitting diodes (LEDs) could, in principle, occur with 100% (or greater) efficiency. The wall-plug efficiency (WPE) of electricity to light conversion is given by the product of three terms:

$$WPE = IQE \times LEE \times \frac{V_p}{V} \tag{3.1}$$

where IQE is the internal quantum efficiency, describing the number of electrons injected into the LED which generate photons in the active region, LEE is the light extraction efficiency of photons generated in the active region that are emitted to free space, V is the operating voltage, and Vp is the photon voltage (the band gap voltage). The voltage term accounts for all ohmic losses in the LED including contacts, voltage drop resulting from transport over epitaxial heterobarriers, and series resistance. The voltage term also accounts for the promotion of carriers above the nominal band gap energy due to thermal energy. Thus, this term can be greater than unity. This topic will be discussed in greater detail in Ch. 4.

This chapter focuses on LEE, which is adversely impacted by the high refractive index of nitride semiconductors ($n \approx 2.5$). The index mismatch between semiconductor and air leads to total internal reflection (TIR), which occurs when light rays impinge on the semiconductor-air interface at an incident angle larger than the critical angle for refraction. The problem of total internal reflection is often addressed using chip shaping or textured

interfaces. If textures have large dimensions compared to the wavelength of light in the device, their physics can be accurately represented by ray optics.

Ray optical simulations are presented to identify the main loss mechanisms in typical nitride LED structures and to provide a pathway to reaching 95% LEE for devices designed for low current density operation.

3.2. Ray Optical Simulations

Maxwell's equations fully describe the behavior of light, but solving these equations for large, complex geometries such as in full LED structures requires tremendous computational power. Ray optics provide a good approximation in the limit of dimensions larger than the wavelength of the light in the material (450 nm in air and 182 nm in GaN for blue LEDs).

Ray optical simulations model the reflection, refraction, and absorption processes in geometrical structures. These light behaviors can be described by the Law of Reflection (Eq. 3.1), the Snell-Descartes Law (Eq. 3.2), and the Beer-Lambert-Bouguer Law (Eq. 3.3), respectively:

$$\theta_i = \theta_r \tag{3.2}$$

$$n_1 \sin(\theta_1) = n_2 \sin(\theta_2) \tag{3.3}$$

$$I = I_o e^{-\alpha L} \tag{3.4}$$

where $\theta_i$and θ_r are the incident and specularly reflected angles, n_1 and n_2 are the real refractive indices of the dielectric materials, and θ_1 and θ_2 are the angles of incidence and refraction (see Fig. 3.1). I is the attenuated light intensity after passing through a length L of absorbing material with absorption coefficient α, and I_o is the unattenuated incident light

intensity. The absorption coefficient α can be related to the imaginary part of the complex refractive index $\underline{n} = n + ik$ where n is the real refractive index, and k is the extinction coefficient. The relationship between α and k is $\alpha = \frac{4\pi k}{\lambda_0}$, where λ_0 is the free space wavelength of the light.

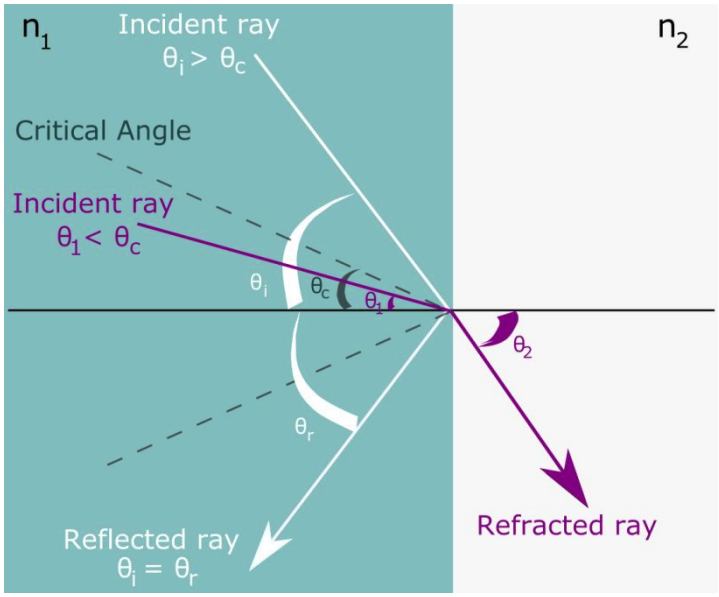

Figure 3.1. Schematic of the interaction of a light rays at a dielectric interface. Rays impinging at angles larger than the critical angle, θ_c will reflect. Rays impinging at angles smaller than the critical angle will refract at angles according to Snell's Law.

Additionally, the Fresnel equations are required to describe the intensity of light in the reflected and refracted portions:

$$R_s = \left|\frac{n_1 \cos(\theta_1) - n_2 \cos(\theta_2)}{n_1 \cos(\theta_1) + n_2 \cos(\theta_2)}\right|^2 \tag{3.5}$$

$$R_p = \left|\frac{n_1 \cos(\theta_2) - n_2 \cos(\theta_1)}{n_1 \cos(\theta_2) + n_2 \cos(\theta_1)}\right|^2 \tag{3.6}$$

where R_s is the reflection for s-polarized incident light and R_p is the reflection for p-polarized incident light. The total reflection, R, and total transmission, T, are then:

$$R = \frac{(R_s + R_p)}{2} \tag{3.7}$$

$$T = 1 - R_t \tag{3.8}$$

During a ray tracing simulation, light rays are emitted in random directions (or following a prescribed probability distribution) from defined light emitting sources. The rays propagate according to the rules of ray optics until they are either absorbed or exit the system. Surfaces can be defined in the model as reflectors, absorbers, scatterers or smooth optical surfaces.

A ray tracing result can produce an overall extraction efficiency as well as detailed information about the fate of rays in the system. This includes information about what percentage of rays are absorbed on specific surfaces or while propagating in specific layers. Ray tracing is unable to describe or calculate wave optical phenomena such as interference or diffraction, but these effects are of minor importance for LEDs with large-scale features.

3.3. Ray Propagation and Absorption in Nitride LED Structures

The high refractive index of GaN (n = 2.47) results in a small critical angle for light extraction into air (θ_c = 23.9°), corresponding to an escape cone of 6.52% for each interface. The most common substrate for commercial nitride blue LEDs is sapphire (Al_2O_3), which has a refractive index of n = 1.7. The difference in refractive index between the epitaxial material and the substrate result in guided optical modes in the layer structure (Fig. 3.2).

Assuming a semi-infinite, two-layer, lossless structure of GaN (n = 2.47) on sapphire (n = 1.7) with rays originating in the GaN, a ray tracing simulation calculates that 8.6% of light is directly extracted into the air (n = 1) cones, 23.4% enters the sapphire mode and 68.0% remains guided in the GaN mode.

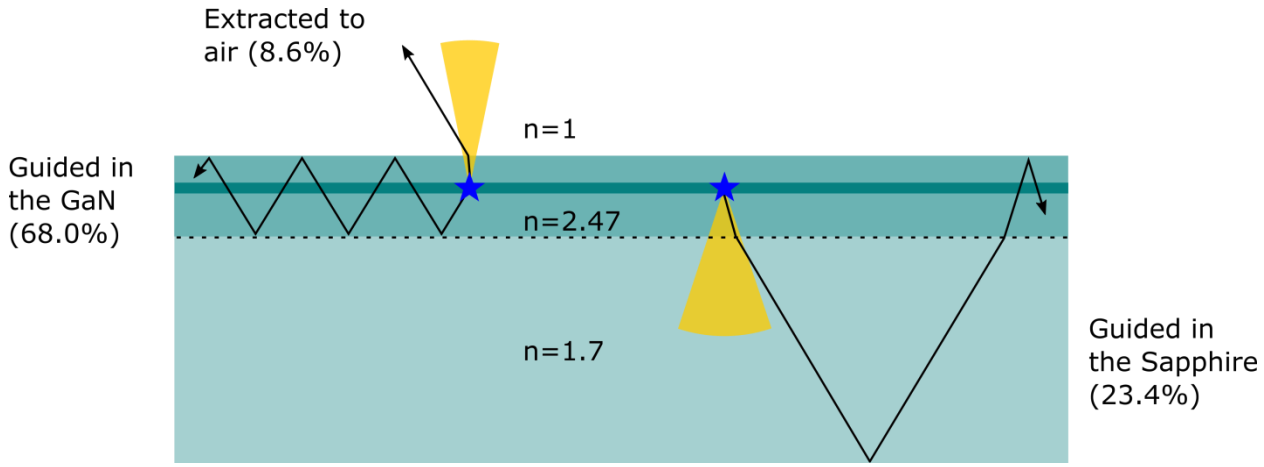

Figure 3.2. Schematic of guided modes in nitride LEDs on planar sapphire substrates.

As rays propagate in guided modes, absorption in any of the lossy materials or interfaces will reduce LEE, including the doped layers, substrate, contacts, current spreading layer, and/or the backside mirror. The design of the chip (e.g. substrate removed flip chip, GaN substrate chip, etc.) determines which lossy elements will dominate and what extraction methods will best optimize the packaged device efficiency.

3.3.1. Model of a Vertical Nitride LED Design on a Planar Sapphire Substrate

A reference structure is now introduced of a nitride LED chip on a planar sapphire substrate to illustrate the loss mechanisms and design concepts with a ray tracing model. The model uses the geometrical and materials parameters from Table 3.1, which assume an emission wavelength of 450 nm via the selected refractive index and absorption coefficient parameters.

Material	Layer Dimensions $l \times w \times h$ (μm)	Refractive index	Absorption Coefficient (cm^{-1})	Average Metal Reflectivity (%)	Surface Area (μm^2)
ITO[1]	460 × 260 × 0.2	2.00	1000	--	--
p-GaN	470 × 270 × 0.2	2.47	100	--	--
Ray Source	470 × 270 × 0.1	--	--	--	--
n-GaN	700 × 500 × 2	2.47	7	--	--
UID GaN Buffer	700 × 500 × 3	2.47	1	--	--
Sapphire Substrate	700 × 500 × 430	1.70	0.1	--	--
Epoxy Glue	700 × 500 × 10	1.50	0	--	--
Palladium (p-metal)	--	1.31	8.91×10^5	66.3	9000
Titanium (n-metal)	--	1.69	6.32×10^5	92.2	7670
Rear metal (Silver)	--	0.135	6.65×10^5	92.2	--

Table 3.1. Nominal dimensions and optical materials parameters for the reference LED on planar sapphire substrate ray tracing model.

The layer structure is presented schematically in Fig. 3.3, and includes the sapphire substrate, GaN buffer layer, n-GaN, p-GaN and ITO layers. The ray source in the model is a volume emitter with an isotropic emission distribution. While this layer marks the origin of the rays, it is not ray traceable itself, and thus no optical constants are defined for it. The model also includes the top metal contacts, and some packaging elements such as the backside silver reflector (a.k.a. the silver header) and epoxy glue for mounting, but is otherwise unencapsulated. It is assumed that in fabrication, the mesa will be etched to access the n-GaN for n-contact, and thus the surface area of the ray source, p-GaN, and ITO layers also have an etched-out region, which reduces their nominal surface areas to 0.1 mm^2.

[1] The ITO layer thickness is close to the limit of accurate ray tracing dimensions. The table lists the values that would be used in an actual device. In the simulation, the ITO thickness was doubled to 0.4 μm and the absorption coefficient was halved to 500 cm^{-1} accordingly to enable more accurate modelling of the proposed structure. Note that although the p-GaN layer is also thin, it is index-matched to the adjacent thick n-GaN and UID GaN layers so the effective feature size is the aggregate of those index-matched layers.

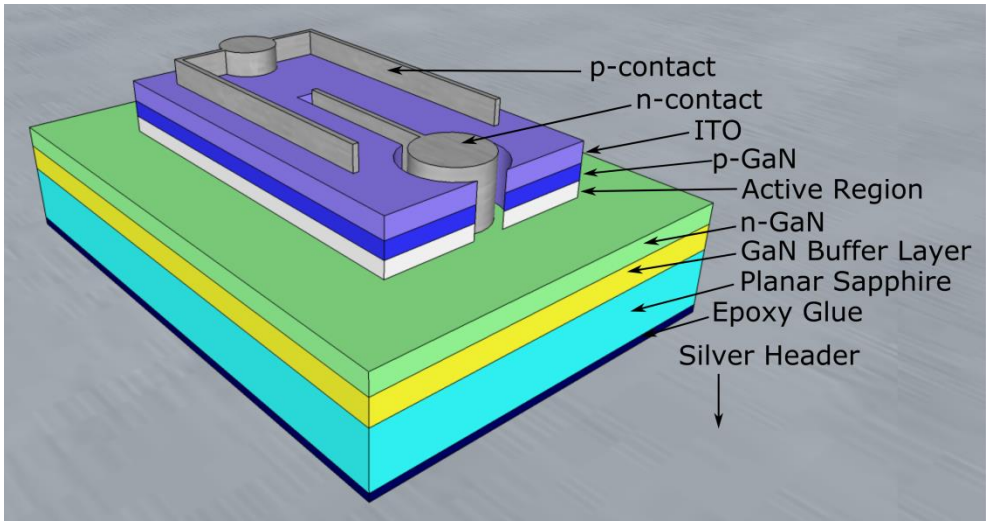

Figure 3.3. Schematic of the layer structure and geometry of a standard thin film planar sapphire LED chip design (not-to-scale).

The total LEE of this design and the breakdown of losses in the various materials are given in Table 3.2. Less than one third of the light generated in the active region can escape the chip in the absence of any extraction techniques. The majority of the rays are caught in TIR in the GaN layers, leading to large losses in the active region elements, including the epitaxial layers, the ITO, and the topside contacts. The rays that are guided in the sapphire mode are mostly absorbed at the silver header or topside materials rather than in the sapphire itself because of the its small absorption coefficient.

Material	Losses (%)
ITO	14.0
p-GaN	6.15
n-GaN	13.2
UID GaN Buffer	2.64
Sapphire Substrate	3.08
Palladium (p-metal)	6.65
Titanium (n-metal)	13.6
Silver Header	10.1
TOTAL Extraction Efficiency	**30.5%**

Table 3.2. Breakdown of losses in a standard GaN on planar sapphire LED chip that is mounted on a silver header with epoxy glue, and otherwise unencapsulated.

The optical losses in LEDs can be divided into two main phenomena: interface absorption and propagation absorption. Interface absorption refers to loss on metallic surfaces including the contacts and the silver reflector. Metal reflectivity and absorption are accurately described in a ray tracing model for all angles of incidence using Fresnel's equations (Eq. 3.5 and 3.6) using the complex refractive index of a material (in a model, these inputs are given as the real refractive index and the optical density). The typical absorption length of metals is ~ 20 nm, which is much thinner than the metal contacts (typically > 300 nm), so these materials are considered opaque and all the incoming light is either reflected or absorbed. Strategies to diminish the impact of contact absorption include reducing the surface area of the top contacts, using current blocking layers below the contacts,[1] or using current apertures away from the contacts.[2]

Propagation losses occur in semi-transparent materials including all epitaxial layers, current spreading layers, and some packaging materials. The Beer-Lambert Equation (Eq. 3.4) governs the propagation losses, which are proportional to the absorption coefficient and the pathlength of the light ray in the material. Strategies to diminish the impact of these

layers include keeping the materials as thin as possible while maintaining satisfactory electrical properties, especially for very lossy materials such as the current spreading layer or p-doped GaN layer.

3.3.2. Model of a Vertical Nitride LED Design on a Planar Bulk GaN Substrate

Sapphire is the most common substrate material for commercially available devices, but bulk GaN substrates, which have been available since 2007 by the hydride vapor phase epitaxial growth, offer enticing properties for homoepitaxially grown nitride LEDs. These properties include lower dislocation densities,[3] and higher substrate thermal conductivity[4,5] than LEDs grown heteroepitaxially on sapphire substrates. Additionally, if the substrates are cut and polished to nonpolar or semipolar orientations, a myriad of additional properties become available including reduced effects of polarization-related electric fields,[6] high indium uptake,[7] or polarized light emission.[8] Growth on native substrates in these alternative orientations has been an active research area at UCSB in the last decade. Thus, this section will present a ray tracing model of a nominal LED on GaN substrate design and consider the sources of loss and extraction strategies that may be employed for such chips.

The simulation mechanics and materials properties are the same as those described in the previous section, except the sapphire substrate is replaced with a 330 μm bulk GaN substrate (n = 2.47, α = 1 cm^{-1}), as shown in Fig. 3.4. In this nominal model, the chip is smooth-sided and mounted on a silver header with epoxy, and otherwise unencapsulated.

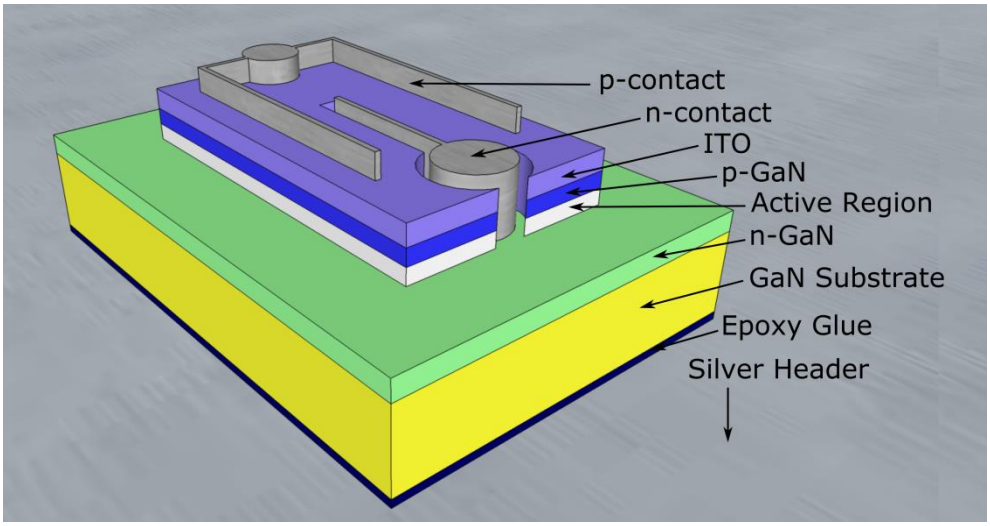

Figure 3.4. Schematic of the layer structure and geometry of a standard LED on bulk GaN substrate chip design (not-to-scale).

The total LEE of this design and the breakdown of losses in the various materials are given in Table 3.3. In this case, less than a quarter of the rays emitted in the active region escape to free space. The greatest fraction of the loss occurs in the GaN substrate where more than 35% of emitted rays terminate. The substrate is index-matched to the active region, and although its absorption coefficient is fairly small, its thickness and high refractive index lead to TIR and long ray pathlengths. Compared with the sapphire chip, the GaN chip has reduced interaction of the rays with the metal contacts, metal mirror, and ITO layer. The distributed losses in the substrate dominate over the localized losses in the metals.

Material	Losses
ITO	12.9
p-GaN	1.82
n-GaN	4.00
GaN substrate	35.2
Palladium (p-metal)	5.13
Titanium (n-metal)	9.06
Rear Metal (Silver)	8.67
TOTAL Extraction Efficiency	**23.2%**

Table 3.3. Breakdown of losses in a standard design GaN substrate chip that is mounted on a silver header with epoxy glue, and otherwise unencapsulated.

In both of these designs, no extraction strategies were employed, leading to losses resulting from rays trapped in TIR. In the next section, options are examined to improve the LEE compared to these nominal designs.

3.4. Extraction strategies

In this section, extraction methods are discussed to improve the LEE compared to the nominal designs presented in sections 3.3.1 and 3.3.2. These methods include surface roughening or texturing, which serve to break the guided modes that otherwise lead to TIR. Methods are also discussed to increase sidewall extraction, which include chip shaping and "volumetric" (low aspect-ratio) designs. We discuss encapsulation, which increases the size of the extraction cone for a given interface by reducing the refractive index contrast compared to air. Finally, we discuss optimizations to the designs including layer thicknesses, absorption coefficients, etc. to identify other effective leverage areas for improving the LEE.

3.4.1. Surface roughening and texturing

A common method to break the guided modes in LED structures is to introduce surface roughness on one or more interface to randomize the propagation direction of light rays as they strike the surface.[9–12]

Sapphire substrates, for example, can be prepared with a surface pattern (usually micro-scale bump or cone pattern) that is designed to randomize rays at the GaN/sapphire interface. This reduces the average number of bounces that the rays must undergo before they are extracted and results in very efficient light extraction. The high efficiency coupled with the low cost of patterned sapphire substrates (PSS) makes this the most common commercial design.[13]

On GaN surfaces, roughness may be generated by photoelectrochemical (PEC) wet etching in KOH solution to produce hexagonal pyramids on the nitrogen face of *c*-plane GaN.[14] In metalorganic chemical vapor deposition (MOCVD) in the Ga-polar orientation, the n-GaN is grown first so that the p-GaN is left exposed to the surface for later activation in an annealing oven. This limits PEC etching to bulk *c*-plane GaN substrates or exposed *c*-plane n-GaN layers.

Extraction textures may also be produced on any desired crystal plane by lithography and subsequent dry etching to produce cone roughening. Recent work also demonstrated a "moth eye" roughening method that uses close-packed silica spheres as a micro mask for a smaller-scale cone texture.[15] Patterning techniques involving dry etching such as these, generate donor level nitrogen vacancies, which are compensating in p-GaN, thus also limiting these techniques to exposed n-type GaN layers.[16] These roughening or patterning

techniques are therefore mainly useful for LEDs on bulk GaN substrates or for flip chip (p-side down, substrate removed) structures, both of which have exposed n-GaN.

Ray tracing simulations were produced to demonstrate the improvement in LEE for chips on PSS and roughened GaN substrates compared with the nominal planar designs presented in sections 3.3.1 and 3.3.2. The PSS chip model is identical to the planar sapphire chip model except that a periodic hemispherical bump pattern is added to the sapphire at the sapphire/GaN interface. The pattern has hexagonal spacing and dimensions shown in Fig. 3.5 (a)(inset). Likewise, a backside roughened GaN substrate chip was modeled to compare with the planar GaN substrate chip. The roughening was modeled as close-packed hexagonal pyramids with 3 μm height and an angle of 58° measured from the horizontal (Fig. 3.5 (b))(inset). Schematics of the two chips are shown in Fig. 3.5 (a)-(b), and Table 3.4 compiles the extraction efficiency and breakdown of losses for the enhanced designs.

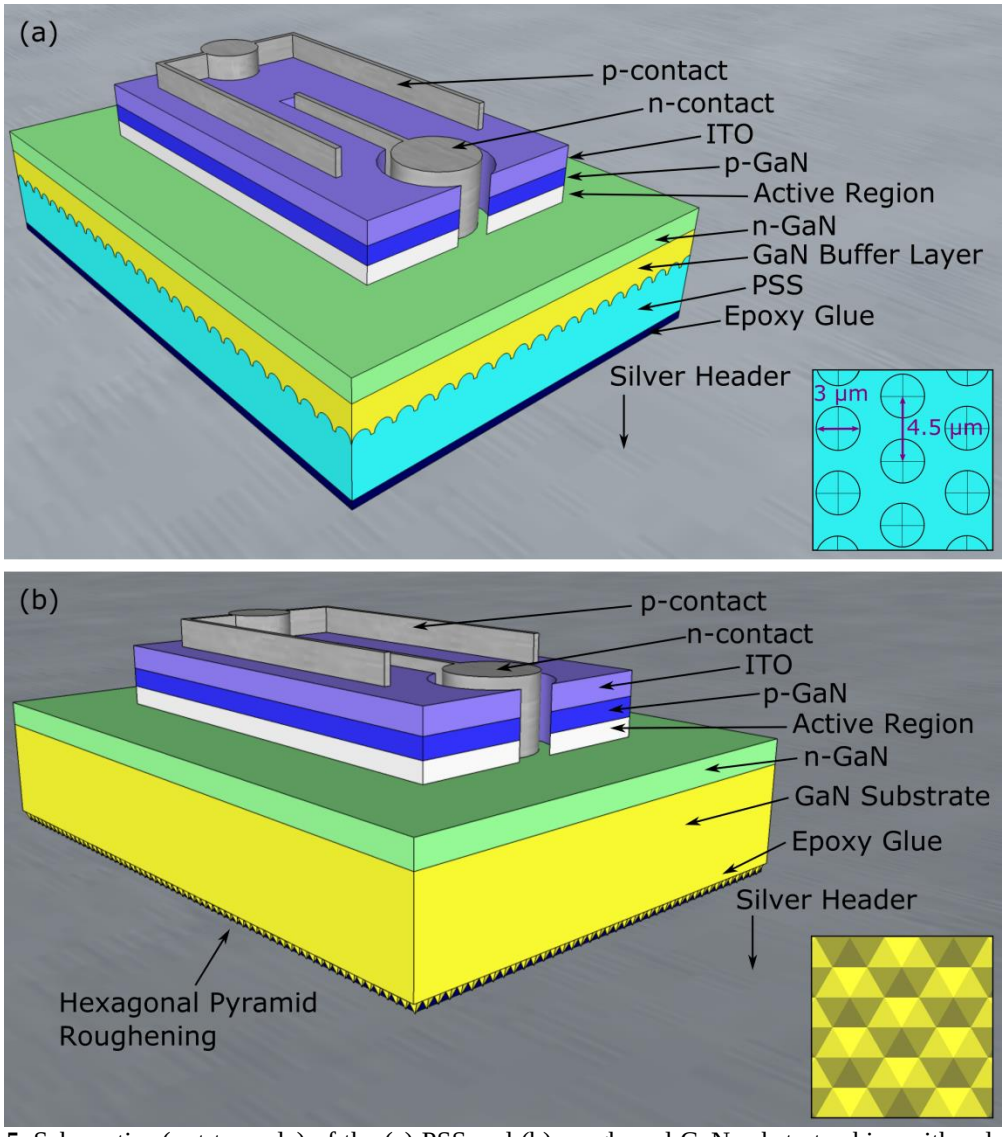

Figure 3.5. Schematics (not-to-scale) of the (a) PSS and (b) roughened GaN substrate chips with enlarged top-views of the sapphire texture and the roughening pattern shown in the inset of each, respectively.

Material	Planar Sapphire Chip Losses (%)	Planar GaN Chip Losses (%)	PSS Chip Losses (%)	Roughened GaN Chip Losses (%)
ITO	14.0	12.9	11.0 ($\Delta \approx$ -21%)	6.91 ($\Delta \approx$ -46%)
p-GaN	6.15	1.82	1.82 ($\Delta \approx$ -70%)	0.93 ($\Delta \approx$ -49%)
n-GaN	13.2	4.00	2.66 ($\Delta \approx$ -80%)	1.80 ($\Delta \approx$ -55%)
UID GaN Buffer	2.64	--	0.47 ($\Delta \approx$ -82%)	--
Sapphire Substrate	3.08	--	2.04 ($\Delta \approx$ -34%)	--
GaN Substrate	--	35.2	--	16.1 ($\Delta \approx$ -54%)
Palladium (p-metal)	6.65	5.13	4.50 ($\Delta \approx$ -32%)	3.49 ($\Delta \approx$ -32%)
Titanium (n-metal)	13.6	9.06	3.42 ($\Delta \approx$ -75%)	3.86 ($\Delta \approx$ -57%)
Rear Metal (Silver)	10.1	8.67	9.57 ($\Delta \approx$ -5%)	8.98 ($\Delta \approx$ +4%)
TOTAL Extraction Efficiency	**30.5%**	**23.2%**	**64.5%**	**58.0%**

Table 3.4. Breakdown of losses in the chip designs that are enhanced from the nominal structure to include patterning and roughening. The models assume that the chips are mounted on a silver header with epoxy glue, and are otherwise unencapsulated.

The interface patterning in the PSS chip more than doubles the total LEE from 30.5% to 64.5%. There were reduced losses in all of the materials. The greatest reduction in losses occurred in the GaN layers and the n-metal. This can be attributed to the randomization effect of the PSS, which breaks the highly guided GaN mode and enables rays to be extracted into air or into the surrounding materials in fewer bounces. In the case of the GaN materials, this reduces the optical pathlength of the rays in the material. In the case of the n-metal, no light emission occurs directly beneath this surface due to the etched mesa design. Thus, rays must bounce at least once before hitting this surface. The reduced number of bounces before extraction greatly reduces the n-metal absorption.

Similar to the PSS effect, the backside roughening on the GaN chip also more than doubles the total LEE from 23.2% for the smooth chip to 58.0% for the roughened chip. The more even distribution of rays throughout the index-matched GaN chip resulted in a more even improvement for the various materials ($\Delta \approx 50\%$ in most cases).

In the backside-roughened GaN chip, the absorption on the silver header actually *increased* slightly compared to the smooth chip. This result can be attributed to an interesting secondary effect of surface roughening or patterning. The main effect, as already discussed, is the randomization of reflected light rays, but another important effect is the increase in single pass escape probability.[17,18] The single pass escape probability is defined as the probability for a random ray of light propagating from the high index material to be transmitted to the lower index material. This value is modified by surface roughness because light, at the second escape attempt, does not intersect the interface with the same angle, giving the ray a greater chance to be in the extraction cone. Fig. 3.6 shows a ray bouncing twice inside of a cone, increasing its probability of being extracted by roughly a factor of two.

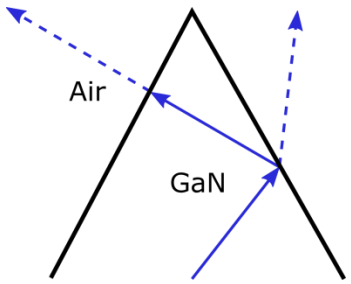

Figure 3.6. A double reflection inside a pyramid leads to approximately double the escape probability because the successive angles of incidence are different. Reprinted from [17] with permission.

The single pass escape probability for a flat GaN/air interface vs. a hexagonal pyramid roughened GaN/air interface were calculated. Fig. 3.7 shows that roughened surfaces transmit less than flat surfaces for angles below the critical angle, but transmit more in the range of 40° - 70°, which is outside of the flat surface extraction cone. Averaging over all solid angles, the single pass escape probability from roughened GaN into air is 13.4%, which is roughly double that of a flat interface (6.7%). Detailed simulations have shown that

the randomization of reflected rays leads to transmission probabilities of ~13% for 2nd and subsequent attempt, compared to flat surfaces, which will undergo TIR and subsequent attempts have zero extraction probability.[17]

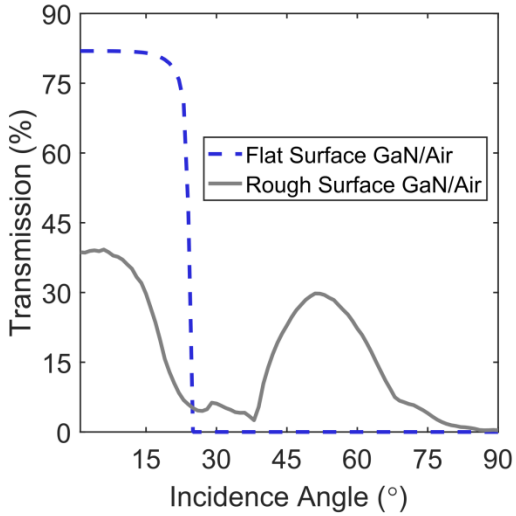

Figure 3.7. GaN roughened surface transmission in air (n = 1) and in epoxy encapsulant (n = 1.5).[2]

The increase in single pass escape probability is not well utilized in these PSS and backside roughened GaN chip designs because in both cases, the pattern or roughness is not at the final extraction interface. In the PSS chip, the patterned surface increases first pass escape into the sapphire substrate, but not directly into free space. In the roughened GaN chip, the rays escaped at first pass simply hit the backside mirror, which actually results in a higher net absorption at that particular interface. The substrate-removed flip chip is an example of a design which can take advantage of both the randomization and the single pass escape enhancement effects of surface roughening or patterning. A flip chip is a p-side down

[2] Notably, ray tracing gives very similar results for roughening patterns with periodic close-packed placement vs. random placement.[17] Because the periodic structures are more computationally efficient, these were used for all simulations in which the realistic roughening should be random (such as with wet chemical etching).

device, and thus surface extraction can occur through a roughened or patterned top exposed n-GaN. An example of a high efficiency flip chip design will be presented in Section 3.5.

3.4.2. Encapsulation

Packaging schemes that utilize high index, transparent encapsulant materials may also be used to increase light extraction.[19] In this scenario, instead of attempting to break the guided modes in the material, the rays are simply given a larger extraction cone. Extraction into a shaped silicone or epoxy encapsulant (n = 1.5) increases the escape cone from GaN (n = 2.47) to ~17.6% by increasing the critical angle to θ_c = 37.4°.

Rays incident on infinite-area flat surface between the semiconductor and the encapsulant will only have a complete extraction cone when the encapsulant index equals the semiconductor index. In a real cuboid-shaped chip with finite surface area, however, full extraction can be achieved when the encapsulant index is somewhat lower than that of the semiconductor. This is because the extraction cones from different faces of the chip will overlap. In a GaN cuboid, overlap of the cones occurs at $n \approx 2$. Section 3.4.5 will also show that in chips with roughening or chip shaping, extraction saturates with encapsulant index as low as n = 1.8.

The encapsulant is usually shaped into a dome to ensure that most rays impinge at near-normal angles, and thus within the critical angle (Fig. 3.8). Another option is an inverted cone shape, which extracts nearly all of the light by the second pass, although the final beam shape is less directional. In both cases, ray tracing calculates that over 99% of the light can escape the encapsulant material into air (assuming a lossless encapsulant).

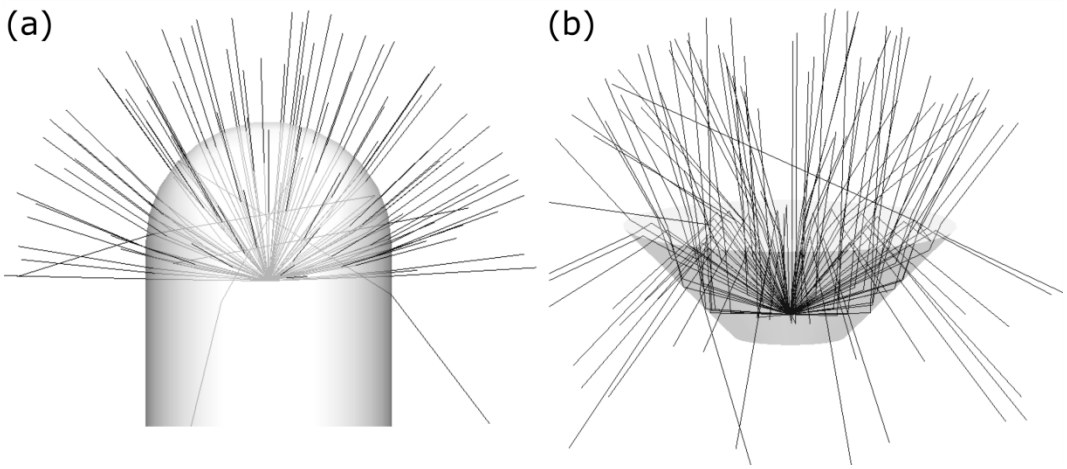

Figure 3.8. Ray tracing simulations of point source emission inside of shaped lossless encapsulants (n = 1.5) with an air ambient. Both shapes can extract > 99% of rays from the encapsulant to the air, however, the dome may be preferable for devices because of its beam shape.

The models are again updated to show the additional enhancements afforded by encapsulation in transparent epoxy (n = 1.5) ambient (where it is assumed for simplicity that 100% of the rays escape the domed epoxy/air interface). The results for the encapsulated PSS and roughened GaN chips are given in Table 3.5.

Material	PSS Chip Losses (%)	Roughened GaN Chip Losses (%)	Encapsulated PSS Chip Losses (%)	Encapsulated Roughened GaN Chip Losses (%)
ITO	11.0	6.91	7.06	4.12
p-GaN	1.82	0.93	1.20	0.50
n-GaN	2.66	1.80	1.29	0.81
UID GaN Buffer	0.47	--	0.23	--
Sapphire Substrate	2.04	--	0.27	--
GaN Substrate	--	16.1	--	6.97
Palladium (p-metal)	4.50	3.49	3.15	2.46
Titanium (n-metal)	3.42	3.86	1.13	1.71
Rear Metal (Silver)	9.57	8.98	3.78	5.22
TOTAL Extraction Efficiency	**64.5%**	**58.0%**	**81.9%**	**78.2%**

Table 3.5. Breakdown of losses for encapsulated PSS and roughened GaN substrate chips. The models assume that the chips are mounted on a silver header and are fully encapsulated in transparent epoxy (n = 1.5).

The improvement in LEE is more pronounced for the roughened GaN chip because the extraction cones on both the surface and the four sidewalls are all significantly increased for the GaN/epoxy interface compared to the former GaN/air interface. The PSS chip sees a somewhat smaller improvement from encapsulation. This is partly because the sidewall extraction is a less important extraction path for a PSS chip than an index-matched GaN chip, and also because the reduction in index contrast is greater for the GaN/epoxy interface than for the sapphire/epoxy interface. Thus, five interfaces on the roughened GaN substrate chip will be greatly improved by encapsulation, whereas one interface on the PSS chip will be greatly improved by encapsulation, while the other four interfaces will only be moderately improved.

3.4.3. Sidewall Extraction and Chip Shaping

Sidewall extraction is an important consideration, especially for LEDs grown on bulk GaN substrates which are thick (~ 300 μm) and approximately index-matched to the active region. This leads to significant light escape via the extraction cones on the sidewalls of the chip. However, the long pathlengths of light in the thick substrate lead to significant substrate absorption, despite its relatively low absorption coefficient (α = 0.5 cm^{-1} - 2 cm^{-1}).

Chip shaping may be used with bulk GaN substrates to redirect light rays at sidewall bounces, increasing their extraction probability on subsequent attempts. This can be achieved using either in-plane or out-of-plane chip shaping. In-plane shaping maintains vertical sidewalls, but the top view of the LED is a non-rectangular shape, such as a triangle or

parallelogram.[20] Out-of-plane shaping angles the sidewalls of the chip, for example in a truncated inverted pyramid (TIP) shape.[21]

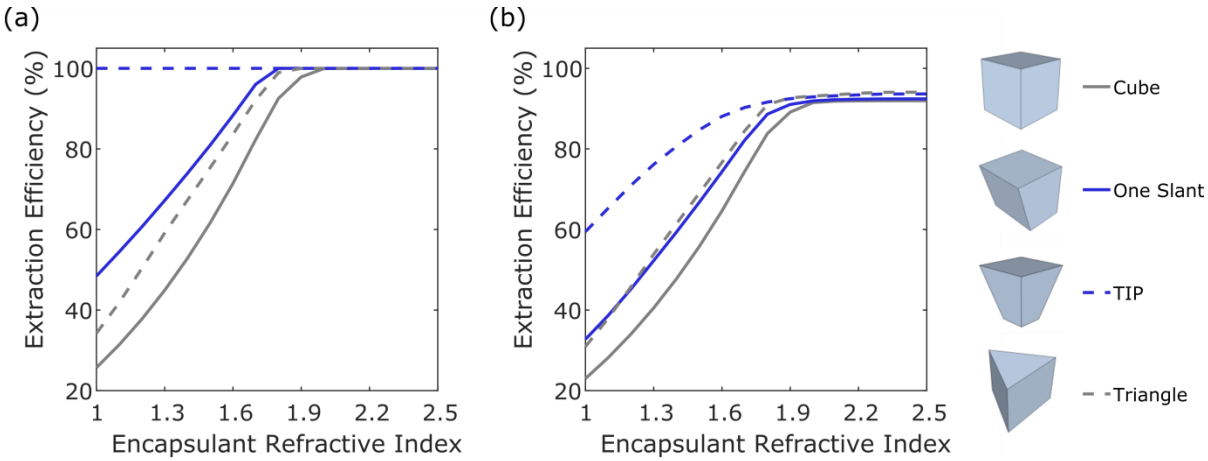

Figure 3.9. Extraction from a point source at the center of four different volumetric shapes (n = 2.5) as a function of ambient refractive index. Trends are shown for (a) non-absorbing materials (where LEE goes to 100%) and for (b) absorbing materials where the LEE reaches a maximum ~90% LEE at high ambient refractive indices. The absorption value for the latter was set to yield a typical amount of loss that is representative of a full LED structure (including contacts, etc).

Simplified ray tracing simulations were performed to illustrate the impact of chip shape on ray re-direction and extraction. Four volumetric shapes were simulated with a central isotropic point source and a refractive index n = 2.5. The ambient refractive index was varied from n = 1 to n = 2.5.

The out-of-plane chip shaping techniques are most effective at breaking the guided modes (Fig. 3.9). Introducing just a single angled sidewall to a non-roughened GaN-based device increases extraction dramatically by breaking the symmetry of the chip. The TIP, which has four slanted sidewalls, breaks all guided modes, eliminating TIR and producing 100% light extraction when material losses are neglected. In fact, even just two slanted sidewalls are sufficient to produce this same result of 100% light extraction, provided that those sidewalls are adjacent and not opposite (data not shown). Furthermore, the angle can be

as small as 4° to achieve this. The in-plane shaping (triangle) provides a benefit over the perfect cuboid, but is not as effective at breaking all guided modes as the out-of-plane techniques.

The TIP shape is applied in ray tracing simulations to both the sapphire and GaN substrate chip encapsulated designs of this chapter. Fig. 3.10 shows the effect of increasing the TIP sidewall angle on the LEE for the planar GaN, roughened GaN, planar sapphire, and PSS chips. Large improvements from TIP shaping were first demonstrated in the GaAlInP materials system for red-orange LEDs where the initial GaAs absorbing substrate was removed and replaced with a TIP transparent GaP substrate, leading to extraction efficiencies up to 60%.[21,22]

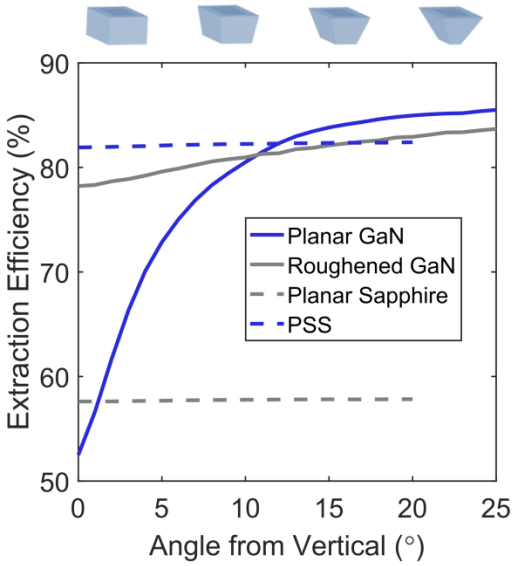

Figure 3.10. A TIP out-of-plane chip shaping design was applied to the planar GaN, roughened GaN, planar sapphire and PSS chips. The LEE is viewed as a function of sidewall angle. Simulations were performed using an epoxy ambient environment (n = 2.5).

It is apparent from Fig. 3.9 that planar GaN substrates experience a greater increase in extraction by angled sidewalls than roughened GaN substrates. The roughening pattern already serves to break the guided modes, and the additional chip shaping provides a smaller benefit than it does for the smooth GaN chip.

The PSS designs, by contrast, are mostly unaffected by the change in sidewall angle. There are relatively few rays propagating into the substrate, and most of those rays are able to quickly exit the substrate sidewalls due to the small refractive index contrast between the sapphire (n = 1.7) and the encapsulant (n = 1.5). Thus, chip shaping provides no significant additional benefit for PSS chips and needs only to be considered for GaN substrate chips.

In this simulation, all four sidewalls of the chip were angled to increase extraction, but it should be noted that for the smooth GaN chip, ~50% of the improvement in extraction is obtained by angling just the first sidewall (at 15° angle from vertical). Furthermore, ~96% of the extraction improvement is achieved by angling just two of the four sidewalls, provided that they are adjacent sidewalls, which will break all guided modes in the chip.

3.4.4. Optimizing Layer thicknesses

Current spreading materials are a necessity for vertical (p-side up) LEDs because p-GaN is such a poor conductor. Without a current spreading layer, current crowding is observed by a localization of the emission under the p-contact. Current crowding results in non-uniform injection, and thus non-uniform carrier density throughout the active region. As a result, the IQE, which is a function of carrier density, will be lower than if uniform injection were achieved. Current crowding also reduces the LEE because light emission is confined to the region under or within a few hundred nanometers of the absorbing metal p-contact.

Current spreading materials for vertical devices must be transparent since they are deposited on the top-side of the chip where light must escape. Typical materials are transparent conducting oxides such as ITO or ZnO. Although called “transparent,” the ITO

layer dominates the optical loss in an encapsulated PSS design, as tabulated in Table 3.5, and is among the most lossy elements in the encapsulated rough GaN substrate chip design as well.

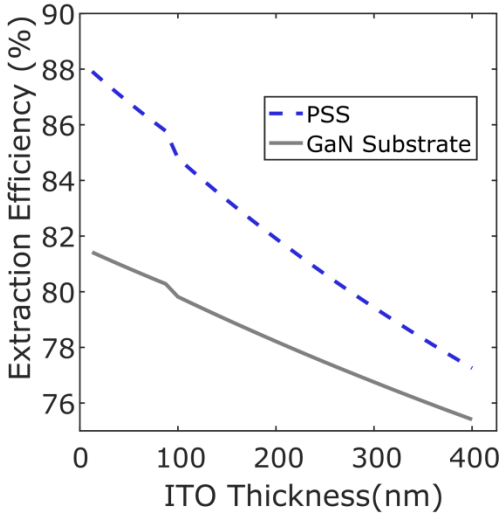

Figure 3.11. Effect of ITO thickness on LEE for roughened GaN substrate and PSS chips, assuming an ITO absorption coefficient of 1000 cm^{-1}.

The impact of the ITO absorption on LEE is shown in Fig. 3.11 as a function of ITO layer thickness for the encapsulated rough GaN substrate and PSS chips. The slope of the curve is steeper for the PSS chip because the rays guided in the thin GaN epi layers interact more heavily with the ITO than in the GaN substrate chip where sidewall extraction is stronger.

In flip-chip (p-side down) devices, the current spreading can be achieved in the p-GaN by a complete Ag or Al metal layer, which also serves as a backside reflector. In this chip design, no transparent conducting oxide is required, but the loss on the backside reflector is usually greater. Section 3.5 includes a simulation of a high LEE flip chip design.

Recent developments in tunnel junction devices using a hybrid MOCVD/MBE growth enable both contacts to be applied to n-GaN layers.[23] The current spreading of

n-GaN is sufficient without the need for an additional ITO layer. This has the potential to significantly enhance the LEE in vertical chips.

Modern bulk GaN substrates grown by hydride vapor phase epitaxy by industry suppliers typically have absorption coefficients $\alpha \approx 1\text{-}2\ \text{cm}^{-1}$. Despite this relatively low value, there is still significant absorption in the substrate due to its high index and the long propagation lengths of rays in the layer. This suggests that reducing the substrate thickness should increase LEE. However, a competing benefit of the thick substrate (also called a volumetric chip design) is an enhanced sidewall extraction efficiency. The influence of substrate thickness in both the PSS and roughened GaN case are shown Fig. 3.12.

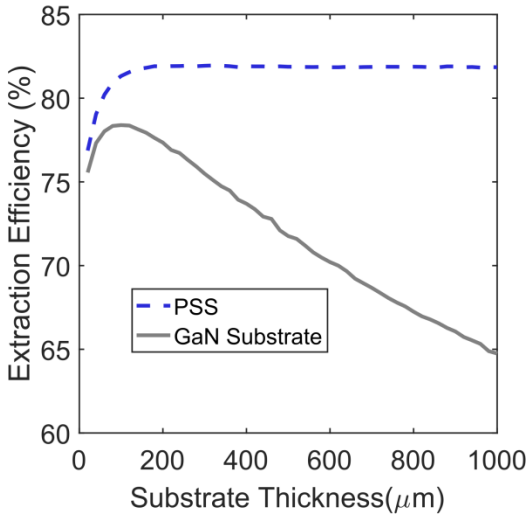

Figure 3.12. Influence of substrate thickness on LEE for encapsulated (n = 1.5) PSS and roughened GaN substrate LED chips.

The roughened GaN substrate model shows an optimum substrate thickness of approximately 120 μm. Below this value, the sidewall extraction is inhibited. Above this value, the sidewall extraction benefit saturates and the distributed losses dominate, leading to a monotonic drop in LEE with further increasing substrate thickness. In the case of the PSS chip, very thin substrate samples will also suffer reduced sidewall extraction. Greater

substrate thicknesses, however, do not appreciably detract from the LEE due to the low absorption coefficient of the sapphire and its low refractive index, which limits propagation of rays into the layer.

3.4.5. Comparing and Combining Extraction Methods

A comparison was done to demonstrate the hierarchy of techniques of roughening, out-of-plane angled sidewalls (TIP pyramid structure), and high refractive index encapsulation for nitride LEDs on bulk GaN substrates (Fig. 3.13). A sidewall angle of 15° was used for the chip shaping. The most effective extraction techniques have high extraction values at low index that saturate earlier with increasing index. The combination of roughening and the sidewall angling gives the highest extraction for low index encapsulants and the benefit of increasing encapsulant index saturates at ~n = 1.8.

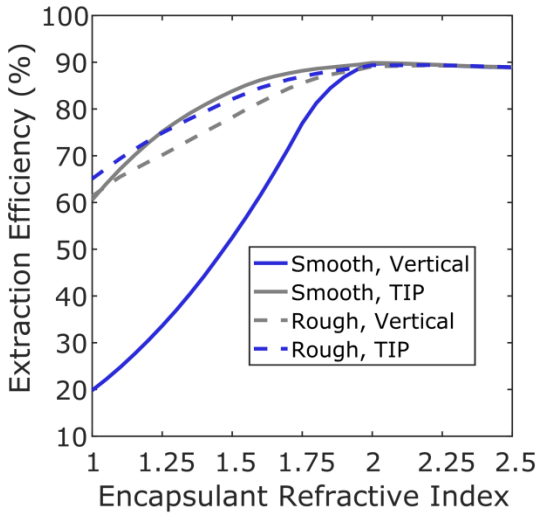

Figure 3.13. Comparison of roughening and chip shaping techniques for light extraction.

The advantage of combining both roughening and sidewall angling over sidewall angling alone, however, is small, differing at most by less than 2%. Roughening without sidewall angling follows after that, indicating that at least for the chip dimensions modeled

here, sidewall angling into a truncated pyramid structure is a more effective extraction method. It should be noted, however, that for larger chip sizes, backside roughening may gain an advantage over chip shaping. This is because the improvement from angled sidewalls diminishes with increasing chip area as the rays must travel further through the device to reach a wall where they may be extracted or redirected.

It is also of interest to compare the effect of the encapsulant index on all of the LED case studies discussed in this chapter. Fig. 3.14 shows that LEDs on bulk GaN substrates, which experience greater internal reflection due to their high refractive index (n = 2.47), exhibit a much greater enhancement in their light extraction as the refractive index of the transparent encapsulant is increased.

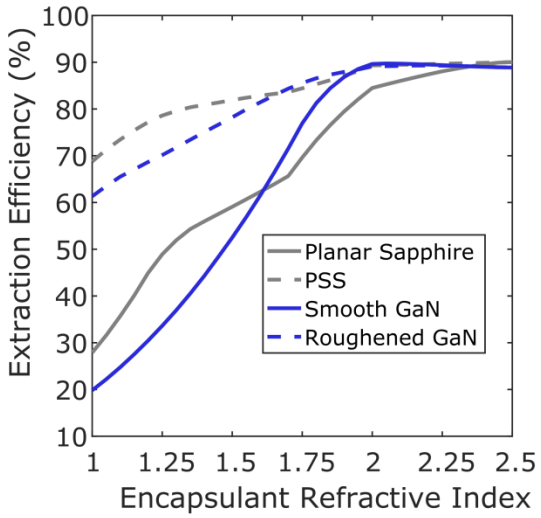

Figure 3.14. Extraction efficiencies with increasing ambient refractive index for four chip simulations.

High index, transparent encapsulation may make GaN substrate chips more competitive with PSS chips for wall-plug efficiency. Use of native GaN substrates for nitride LEDs is well known to improve other aspects of LED optical performance due to the low dislocation densities and high thermal conductivity relative to sapphire substrates.

Additionally, at high refractive indices, the distinction between roughened and non-roughened GaN vanishes, so there would be no need to roughen the device if sufficiently high index, transparent encapsulants are used.

The extraction efficiencies in these various chips all exceed 80% at a relatively low index of $n = 1.8 - 1.9$. Refractive indices of this magnitude are available in commercial glasses and some epoxies and polymers. In practice, however, most of these materials have nontrivial absorption coefficients in the visible range, which currently limits their implementation. Advances in this related field of materials will be advantageous for LED packaging.

3.5. Simulation of 95% LEE Chip Designs for Low Power Operation

As introduced in Ch. 1 and discussed in depth in Ch. 4, a WPE approaching or even exceeding 100% is possible in a real device. Eq. 3.1 shows that a critical component of the WPE is the LEE, which must be increased to its practical limit to achieve ultra-high efficiencies. In this chapter, three different nitride LED chip designs will be discussed that can achieve LEEs in the range of 95%. These include advanced PSS and volumetric GaN chip designs. A high efficiency GaN flip chip design will also be introduced.

3.5.1. LEE Designs for Low Current Density Operation

High power LEDs are operated with current densities on the order $J \approx 10 - 100$ A/cm^2. At these high current densities, Auger recombination dominates over radiative recombination, reducing the IQE and WPE. The IQE of typical nitride LEDs peaks at a current density of $J \approx 1 - 5$ A/cm^2.

One goal for the lighting industry is to maximize the light output per dollar (W/$), and historically, this has been achieved by driving each (expensive) LED chip at high output powers (and high input current density). This optimized the competition between epitaxial costs and the balance of system costs, but did not necessarily result in the highest efficiency devices.

However, the situation is changing rapidly as recent dramatic reductions in epitaxial costs have been realized. Today, the greatest component cost in a packaged LED is the heatsink. The size of the heatsink depends on the WPE of the semiconductor device, making it more advantageous to operate at the highest possible efficiencies. This results in a modern LED lamp which is characterized by many (cheap) LED chips, each of them operating at low output power (and low input current density), but high efficiency.

Operation at low current densities allows the IQE to be maximized and the heatsink costs to be reduced (or eliminated). It also allows for relaxed design constraints in the light extraction schemes. For example, low injection current reduces current crowding effects and enables the use of widely-spaced thin contact stripes, which reduce the areal coverage of the n- and p-contact metals and the associated light absorption. The reduced current crowding also allows the ITO current spreading layer to be thinned or eliminated.

With low power operation, there is also less concern for self-heating and associated thermal droop. This enables the replacement of the highly absorbing bottom silver reflector (header) with a ~99% diffuse reflective scattering material to redirect light out of the package. Omnidirectional dielectric materials can also be used for very high reflectivity, low loss materials.[24] Alternatively, a fully transparent package can be used to extract light out all sides of the chip.

The metal contacts, current spreading layer, and backside metal reflected are the major sources of optical absorption for PSS chip designs, as previously discussed. Therefore, significant improvements in overall LEE are possible considering designs for low current density operation.

In this section, three viable nitride LED chips were designed to reach LEE ≈ 95% considering low current density operation ($J \sim 1$ A/cm^2). Ray tracing simulations were carried out for the envisioned LED structures (Fig. 3.15) to determine the total LEE and to rank the sources of loss in each chip. The structures include a p-side-up rectangular chip on a patterned sapphire substrate (hereafter "PSS chip") (Fig. 3.15 (a)), a p-side-up triangular chip on a bulk GaN substrate (hereafter "triangular chip") (Fig. 3.15 (b)), and an n-side-up triangular flip chip ("TFC") on a bulk GaN substrate (Fig. 3.15 (c)).

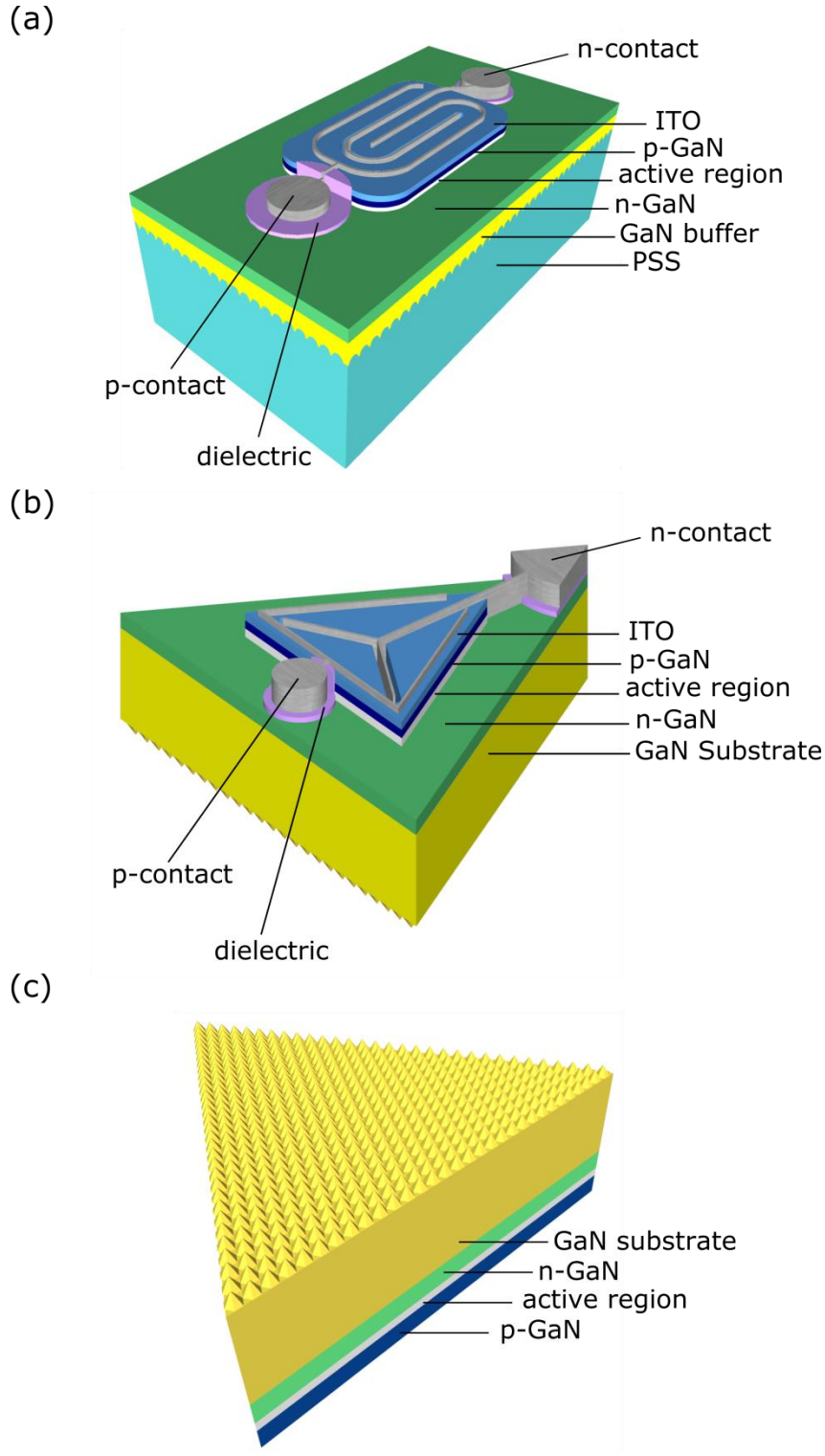

Figure 3.15. Schematic of LED chip designs of (a) a thin film PSS chip with thin ITO and small contact area, (b) a triangular chip on bulk GaN with backside roughening, thin ITO and small contact area, and (c) a flip chip on bulk GaN with topside roughening, and where both the n- and p-contacts reside on the backside of the chip, and double as the bottom reflector (92.2% reflectivity), allowing for the elimination of the ITO spreading layer.

Table 3.6 lists the optical materials parameters used in the simulations of the advanced LEE designs including refractive index, absorption coefficient and reflectivity values. Some lower-loss materials were employed compared to the simulations in Sections 3.1 - 3.4, such as higher reflectivity metal options (Al instead of Ti and Pd), however we will rely mainly on design changes rather than assumption of improved material properties.

Table 3.7 provides the dimensions of the layers and features for each of the three simulations: the PSS chip, the triangular chip, and the TFC. The following sections will discuss the details of each chip, comparing and contrasting with designs for high power chips.

Material	Refractive index	Absorption Coefficient (cm^{-1})	Reflectivity (%)
ITO	2.00	1000	--
p-GaN	2.47	100	--
Ray Source	--	--	--
n+-GaN	2.47	7	--
n-GaN	2.47	3.5	--
UID GaN Buffer	2.47	1	--
Sapphire Substrate	1.70	0.1	--
GaN Substrate	2.47	1	--
SiO_2	1.4	0	--
Aluminum (p-metal)	0.617	1.48×10^{6}	92.0
Aluminum (n-metal)	0.617	1.48×10^{6}	92.0
Rear Scatterer	--	--	99.0
Rear Silver	0.135	6.65×10^{5}	92.2
Epoxy Dome	1.50	0	--

Table 3.6. Nominal optical materials parameters for the high LEE LED designs.

Material	**PSS** Nominal Layer Dimensions $l \times w \times h$	**Triangular Chip** Nominal Layer Dimensions (s, h)	**TFC** Nominal Layer Dimensions
ITO	450 × 270 × 0.04 μm	500 μm, 0.04 μm	--
p-GaN	450 × 270 × 0.10 μm	500 μm, 0.10 μm	400 μm, 0.10 μm
Ray Source	470 × 270 × 0.04 μm	500 μm, 0.04 μm	395 μm, 0.04 μm
n+-GaN	900 × 570 × 0.30 μm	850 μm, 0.30 μm	400 μm, 0.30 μm
n-GaN	900 × 570 × 1.00 μm	850 μm, 1.00 μm	400 μm, 1.00 μm
UID GaN Buffer	900 × 570 × 3.50 μm	--	--
Sapphire Substrate	900 × 570 × 430 μm	--	--
GaN Substrate	--	850 μm, 150 μm	400 μm, 150 μm
Aluminum (p-metal)	fsa = 6.11%	fsa = 5.91%	--
Aluminum (n-metal)	fsa = 3.60%	fsa = 3.44%	--
Rear metal header or scatterer	r = 9 mm	r = 9 mm	r = 9 mm
Epoxy Dome	r = 10 mm h = 10 mm	r = 10 mm h = 10 mm	r = 10 mm h = 10 mm

Table 3.7. Nominal dimensions for the high LEE LED designs. For the rectangular-shaped PSS chip, the layer dimensions are given by the length *l*, width *w*, and height *h*, unless otherwise notated as values of the radius *r*, or fractional surface area coverage *fsa*. The fsa refers to the surface area coverage of the metal contacts divided by the mesa area of the chip, which is nominally 0.1 mm^2 for the PSS and triangular chip and 0.07 mm^2 for the TFC. The triangular chip and TFC dimensions are given as the side length *s* of the equilateral triangle and the height, unless otherwise notated.

3.5.2. Description of the Advanced PSS Design

The advanced PSS chip design has similar elements to the design presented in Section 3.4. The simulation assumed a 430 μm thick sapphire substrate with an extraction pattern of hemispherical bumps at the sapphire/GaN interface. The bumps had radii r = 1.3 μm and heights h = 1.3 μm with a hexagonal center-to-center spacing of 3.63 μm. The epitaxial structure assumed a 3.5 μm undoped GaN buffer layer, a 1 μm n-GaN layer, and a 100 nm p-GaN layer. The ray source was modeled as a non-ray-traceable volume that emits isotropically from the interface of the n- and p-GaN layers. Layers that are too thin for accurate modelling with ray tracing, such as the quantum wells and the electron blocking layer, were neglected, as was any refractive index difference between the n-GaN and p-GaN (all GaN layers were modelled with n = 2.47).

The ITO layer was given a thickness of 40 nm (much thinner than the 200 - 250 nm that is typically used for high power LEDs), and the contact metal coverage was ~ 6% of the surface area (compared to > 9% for the standard designs described in the Sections 3.3 - 3.4). Higher reflectivity Al contact metal (R = 92%) was simulated for the advanced chips compared to the previous designs which used Ti and Pd.

The PSS chip has an etched-mesa design with a nominal area of 0.1 mm^2, as before, and thus no light emission occurs beneath the n-contact. An enhancement of the LEE was sought by moving the large wire bonding pads of both the n- and the p-contact off the mesa and away from the light emission area. A 300 nm SiO_2 underlayer was placed beneath each of these metal pads to enhance reflection beneath the pads. In the practical implementation of the design, the SiO_2 also serves to prevent device shorting and assists with metal adhesion (see Ch. 4 for additional details).

The enhanced package employs a diffuse scattering surface rather than a metallic one. Diffuse reflector materials such as $BaSO_4$ are nearly perfect reflectors in the visible light range and, as such, have been used for applications such as integrating spheres. These simulations assume a similar type of coating and a reflectivity estimate of 99%. The best silver headers produced and stored in controlled industry environments, on the other hand, do not exceed R = 97%. The encapsulant was dome-shaped (as in Fig. 3.8 (a)) and perfectly transparent epoxy (n = 1.5) with a total height of 1 cm and a radius of 0.5 cm.

3.5.3. Description of Triangular Chip Design

The triangular chip is a bulk GaN substrate chip that has both surface roughening and in-plane chip shaping (which is more industrially feasible than out-of-plane chip shaping).

Like the PSS chip, it is a vertical chip with an etched mesa design. The GaN substrate was given a thickness of 150 μm and hexagonal pyramid roughening[14] on the N-face of the chip. The hexagonal pyramids were close-packed with a height of 4.3 μm and an angle of 58° measured from the horizontal.

The epitaxial structure was similar to the PSS design except for the absence of an additional 3.5 μm buffer layer. The chip mesa area was also nominally 0.1 mm^2 with an equilateral triangular design and similar fractional surface coverage of p- and n-contact metals (Fig. 3.15). The wire bonding pads were also placed off the mesa for the triangular chip with SiO_2 layers placed beneath each to enhance the backside reflectivity and reduce the metal absorption. The same package was used as in the PSS design.

3.5.4. Description of Triangular Flip Chip Design

A flip chip design is introduced. Many flip chip designs utilize a backside mirror which covers the whole p-side of the chip, doubling as the p-contact, tripling as a perfect current spreading layer, and quadrupling as a high thermally conductive layer. The present design assumes a bulk GaN substrate which is flipped and then thinned and PEC roughened with the same hexagonal roughening pattern described for the triangular chip. This simple TFC has neither topside contacts nor an ITO layer. Instead, it is bonded directly to backside silver n- and p-contacts in a flipped mesa design similar to the one presented and demonstrated in ref [25]. The contact material is assumed to be silver with a conservative R = 92.2%.

3.5.5. Simulation Results

The results of these ray tracing simulations are shown in the first three columns of Table 3.8, yielding $\eta_{extract} > 90\%$. The major losses in the PSS chip come from the metal contacts and the ITO layer whereas the major losses in the GaN chips come from the substrate absorption and the metal components (topside contacts for the triangular chip and backside metal mirror for the TFC). An industry design similar to the TFC has been shown to have $\eta_{extract} \approx 95\%$.[25]

Material	PSS (%)	Triangular Chip (%)	TFC (%)	PSS, Transparent Package (%)	Triangular Chip, Transparent Package (%)
ITO	1.31	0.561	--	1.28	0.407
p-GaN	0.626	0.626	0.063	0.615	0.583
n-GaN	0.495	0.453	0.357	0.461	0.370
UID GaN Buffer	0.272	--	--	0.253	--
Sapphire Substrate	0.410	--	--	0.277	--
GaN Substrate	--	6.43	3.55	--	4.22
Aluminum (p-metal)	0.577	0.455	--	0.519	0.267
Aluminum (n-metal)	0.375	0.251	--	0.338	0.103
Rear Scatterer	0.682	0.877	--	0.288	0.259
Rear Metal (Silver)	--	--	2.88	--	--
TOTAL Extraction Efficiency	**95.2**	**90.3**	**93.1**	**96.0**	**93.8**

Table 3.8. Summary of the sources of optical losses in high LEE LED designs.

The main advantage of the triangular chip design is the higher IQE values that could be accessible on a bulk substrate due to the reduction in threading dislocation densities compared to heteroepitaxy. A similar design could also be employed for LEDs grown on nonpolar or semipolar bulk GaN substrates, except that they would require a different

roughening method. This design is the most sensitive to GaN absorption coefficient, and could become much more competitive with small improvements in that material component.

The TFC takes advantage of both benefits of surface roughening: the randomization effect and the enhancement of first-pass extraction enhancement. This is because the texture is at the surface rather than on the backside (e.g. triangular chip) or at an interface (e.g. PSS chip) where it otherwise only benefit from the randomization effect. Again the GaN substrate absorption dominates, followed by the absorption on the imperfect silver mirror.

3.5.6. Transparent Package LED

The light extraction can be further enhanced with a fully transparent package design, which can be implemented for vertical chips. High efficiency structures (>90%) can already be achieved for vertical chips by replacing bottom metal reflectors with diffuse scattering reflectors. A more aggressive approach uses a fully transparent package, which, rather than redirecting downward emitted light back up with a diffuse reflector, instead allows light extraction out of both the top and the bottom of the chip. This can be practically implemented by mounting the chip on the side of the transparent stand (e.g. made of sapphire, glass, or epoxy), wire bonding to a distant metal electrode and encapsulating the full structure in epoxy[26] as illustrated in Fig. 3.16.

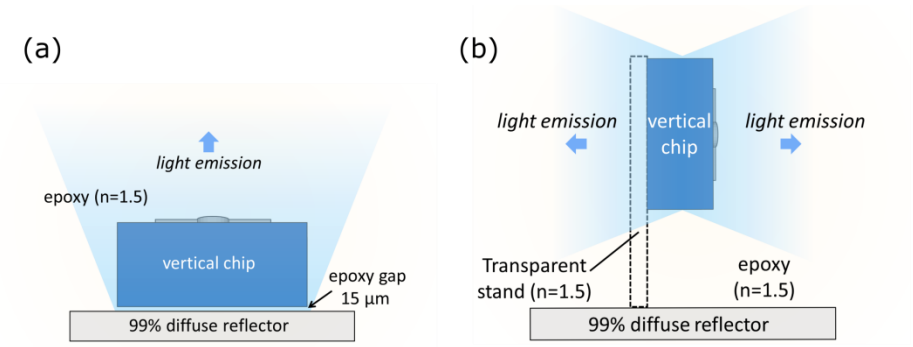

Figure 3.16. Schematic of LED package designs for vertical chips (left) attached with epoxy on a diffuse scattering reflector; (right) in a transparent package that allows light emission out of all sides of the chip.

This approach would normally be limited by the heat sinking ability of the transparent stand material. However, in the case of operation at low current density, this design constraint is relaxed and this design becomes a realistic possibility. In some cases, it may even be advantageous to have an adiabatic system, such as when operating at a theoretical 100% WPE. The physics of this scenario will be discussed in detail in Ch. 4.

The last two columns of Table 3.8 give the simulation results of implementing the vertical chip designs into a transparent package architecture where the chip is mounted on a transparent stand that is index-matched to the immersing epoxy encapsulant. These packages can reach $\eta_{extract} \approx 95\%$.

3.6. Conclusion

This chapter has given a thorough examination of the extraction efficiency design elements relevant to modern nitride LEDs including designs on PSS and bulk GaN substrates. Through ray tracing simulations, extraction enhancements were demonstrated by surface roughening/patterning, encapsulation, sidewall angling, surface electrode, chip architecture and LED packaging. In the final section, advanced LEE designs were proposed

for LEDs operating at low current density (at or near their peak efficiency). Simulations indicate that it is possible to achieve on the order of ~ 95% LEE with these designs, and that it may be easiest to achieve these very high efficiencies with PSS chips, which are mature in the LED lighting industry today. LEE values > 95% greatly enhance the possibility of realizing devices which can operate at 100% or greater WPE.

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Chapter 4. The Prospects for 100% Wall-Plug Efficient Blue LEDs

4.1. LED Efficiency Definitions

The wall plug efficiency (WPE) of an LED, also known as the power conversion efficiency, is defined as the fraction of the input power (IV) that is converted to optical output power. The WPE per electron/hole pair can be expressed as the product of three terms:

$$\mathrm{WPE} = \mathrm{IQE} \times \mathrm{LEE} \times \frac{V_p}{V} \tag{4.1}$$

where IQE is the internal quantum efficiency, describing the fraction of electrons injected into the LED that generate photons in the active region. LEE is the light extraction efficiency, describing the fraction of photons generated in the active region that are emitted to free space (discussed in depth in Ch. 3). V is the operating voltage, and $V_p = h\nu/q$ is the photon voltage, where $h\nu$ is the photon energy.

The product of IQE and LEE is the external quantum efficiency (EQE), which describes the fraction of electrons injected into the LED which generate photons that are emitted to free space.[1] WPE and EQE are easily measured values that are determined from the applied current and integrated electroluminescence measurements of the output power and spectrum. EQE can be expressed as:

$$\mathrm{EQE} = \mathrm{IQE} \times \mathrm{LEE} = \frac{P/h\nu}{I/q} \tag{4.2}$$

where P is the optical output power, and I is the applied current. The EQE has a maximum value of 1.

The IQE and LEE are not easily measured. Simulations and models are used to approximate their values. LEE simulations of full LED structures using ray tracing methods were described in detail in Ch. 3. IQE is often described by the 'ABC' model:

$$\mathrm{IQE} = \frac{\mathrm{B}n^2}{\mathrm{A}n + \mathrm{B}n^2 + \mathrm{C}n^3} \tag{4.3}$$

where A, B, and C are the Shockley-Read-Hall (SRH), radiative, and Auger recombination rates, respectively, and n is the injected carrier density in the emitting quantum wells (not to be confused with the refractive index as in Ch. 3). At current densities beyond the peak efficiency ($J \approx 1$ - 5 A cm^{-2}), the LED efficiency decreases via efficiency droop, which is dominated by a mechanism of non-radiative Auger recombination.[2–4]

The voltage ratio V_p/V in Eq. 4.1 describes the energy efficiency per photon. The voltage, V, accounts for ohmic losses in the contacts, epitaxial heterobarriers, and series resistance, which all increase V compared to V_p. However, V also accounts for the promotion of carriers above the nominal band gap energy due to thermal energy, which decreases V compared to V_p. Thus, it is possible for V_p/V to be greater than unity at finite lattice temperatures, which is the topic of the present chapter.

A 100% WPE (i.e. WPE = 1) is achieved according to Eq. 4.1 and Eq. 4.2 if the following condition is met: EQE = $V/V_p = qV/h\nu$. This means that the gains in V_p/V fully recoup the losses to the EQE. This chapter will discuss the historical evidence for WPE $\geq$ 100%, the requirements for achieving a demonstration for nitride LEDs at technologically relevant current densities, and the progress to date on that task.

4.2. The Physics and History of Heat Recycling and Electroluminescent Cooling

Light emission was first observed at photon energies higher than the injected energy, qV more than 50 years ago.[5–7] The potential for WPE $\geq$ 100% was recognized and subsequent thermodynamic analyses[8,9] supported its validity. Thermal energy from the lattice provides the boost to promote carriers to the quantum well (QW) ground states where they undergo recombination and light emission at energies higher than the injected energy.

The process involves intake of heat energy and its associated entropy from the environment. This is consistent with the laws of thermodynamics. Energy is conserved because the inputs of work from the power source and lattice thermal energy absorbed by the carriers equal the output in radiative and thermal energy to the environment. The net entropy of the closed system increases because the entropy of the emitted spontaneous radiation, which has a broad optical spectrum and omnidirectional emission (leading to emission in many quantum states), exceeds the entropy of the e-h pair and the absorbed heat from the lattice.[10]

Although the thermodynamic framework has been long established, the phenomenon of WPE $\geq$ 100% operation was only experimentally realized in 2012.[11] In this demonstration, Santhanam et al. operated an $In_{0.15}Ga_{0.85}As_{0.13}Sb_{0.87}$ mid-IR LED (λ = 2.42 μm) in a low bias regime, $V \ll k_BT$ with an external heat source up to 135 °C.

Such operating conditions resulted in extremely low voltage V = 70 μV, enabling 100% and greater WPE. This is because the voltage term V_p/V more than recoups the losses in EQE. Low V, however, requires exponentially low current I according to the ideal diode equation (Eq. 4.4), and thus the demonstration was at correspondingly minuscule output power (pW).

$$I = I_o(T)(e^{qV/kT} - 1) \tag{4.4}$$

The diode equation includes the temperature-dependent saturation current $I_o(T)$ among the other terms already defined.

Figure 4.1 shows the relationship between WPE, EQE, and V_p/V as a function of optical output power. The plot is based on data from [11]. The EQE has a single peak corresponding to the point at which the radiative recombination dominates in the IQE equation. The IQE and EQE drop at lower bias due to growing competition from Shockley-Read-Hall non-radiative recombination compared to radiative bimolecular recombination. Under heated operation, carrier leakage increases and additional SRH recombination states are also activated, further reducing the IQE and EQE.

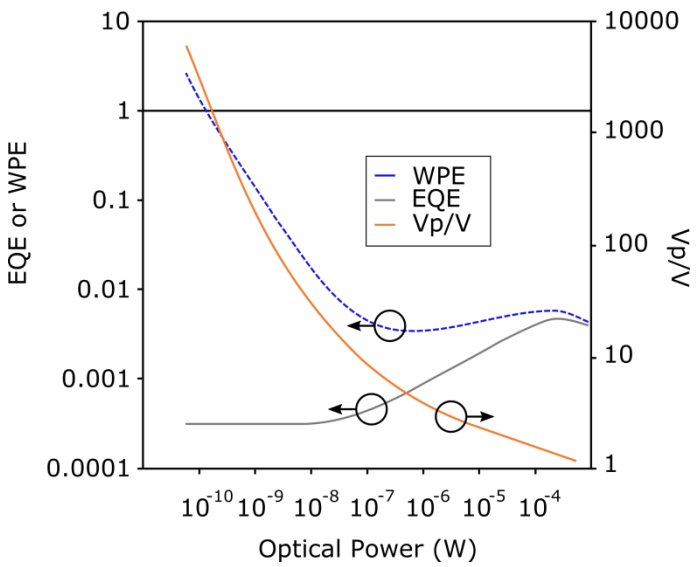


Figure 4.1. The WPE curve has two peaks, the conventional peak occurring near the EQE peak, and the other occurring at low bias where the EQE saturates as V_p/V continues to rise. At low bias, the WPE exceeds 100% at an EQE of just 0.03% and V_p/V of ~700,000%. The plot is based on 135 °C measurement data for a mid-IR LED in [11].

At extremely low bias such that $V < k_B T/q$, the IQE (and the EQE under the assumption that LEE is independent of applied bias) saturates, while voltage continues to

drop, allowing the WPE to rise along with the photon energy efficiency, V_p/V. Thus, at very low bias and optical output power, it is observed that the LED can exceed 100% WPE despite an EQE of just 0.03%.[11] For an arbitrarily low power, an arbitrarily high WPE can be achieved because the EQE remains finite even as V→0.[12]

$$\lim_{V\to 0}\ EQE \neq 0 \tag{4.5}$$

$$\lim_{V\to 0}\ \frac{h\nu}{qV} \times EQE = \infty \tag{4.6}$$

Operating in this low-bias regime, a peak WPE of ~ 230% was demonstrated at 135 °C, delivering just 69 pW of output power. A subsequent publication demonstrated the electroluminescent cooling phenomenon at room temperature in the low bias regime for smaller bandgap InGaAsSb LEDs, emitting at 3.4 μm and 4.7 μm.[13] The highest room temperature output power achieved for 100% WPE LEDs was approximately 100 pW at 3.4 μm,[13] and the highest reported WPE was 5700±1600% at 2.5 μm, emitting just 1 pW at 150 °C.[14]

Such low powers require special detection methods and do not produce technologically relevant light intensities, but nonetheless have confirmed the longstanding possibility of electroluminescent cooling in LEDs, and may contribute to more specialized applications.

While these first demonstrations of 100% WPE LEDs required very low bias operation and utilized mid-IR LEDs, recent experiments also demonstrated the possibility of thermoelectric pumping at technologically relevant operation points ($J \approx 3$ A/cm^2) for a singulated, unpackaged semipolar InGaN/GaN single QW LED emitting at 450 nm.[15] Upon heating up to 615 K, the device exhibited negligible drop in peak WPE, while the peak moved to higher current densities, thus resulting in a nearly fourfold greater output power.

The point at which the peak WPE began to exceed the peak EQE was at 535 K, indicating the crossover where gains in V_p/V can recoup losses in EQE.

The enhanced high temperature performance was attributed to thermoelectric pumping as the maximum WPE was observed at a bias such that $V < hv/q$. The combination of electrical work and Peltier heat transferred from the lattice phonons enabled injection below the photon energy. A thermal-droop-free WPE was also demonstrated at Soraa, Inc. in 2015 for a fully packaged violet LED over a temperature range of 25 - 85 °C. This device achieved a very high WPE of 84%.[16] These results demonstrate that thermal pumping occurs in GaN devices and can be used to mitigate the effects of thermal droop for a heated package. However, WPE of 100% or higher for nitride LEDs has not yet been achieved.

4.3. Requirements for ≥ 100% WPE Operation for Nitride LEDs

Nitride LEDs in the blue spectrum now have WPE > 70% at current densities (J = 1 – 5 A cm-2) with records exceeding 80%.[16,17] At higher current densities, which are desirable operating points for high power lamps, a decline in the efficiency is observed, which is referred to as "efficiency droop."[18,19] Efficiency droop is attributed to the onset of significant non-radiative Auger recombination at medium to high current densities. As a result, commercial blue LEDs today operate below their peak efficiency in order to minimize the total lamp cost.

According to the 2016 Department of Energy (DOE) solid-state lighting (SSL) research development plan, typical state-of-the-art blue LEDs that would be employed in a phosphor-converted white LED lamp operate at WPE ≈ 66%. The losses come from LEE (87%), IQE (88%), efficiency droop (10% loss considering 35 A/cm2 operation), and the

energy efficiency per photon (referred to in that document as the electrical efficiency) (96%).[20] The full phosphor-converted white lamp has a WPE $\approx$ 33% considering the additional Stokes, phosphor IQE, and LEE losses of the converted light.

In the case of blue LED operation targeted at $\geq$ 100% WPE, it is proposed to operate at low current density at the peak LED efficiency, where all aspects of the LED design are different than today's paradigm. At low current density operation, efficiency droop can be neglected. For $\geq$ 100% WPE, the photon energy efficiency losses, V_p/V, must not only be eliminated, but in fact, this aspect of LED efficiency must have significant gains by thermal energy recycling to recoup EQE losses. As we will show in this chapter, $V_p/V > 100\%$ is readily achievable for commercial and lab devices operating at low current densities (~ 1 - 5 A/cm^2), which also typically correspond to the position of the peak EQE.

Thus, the main challenges are to maximize the IQE, the LEE, and V_p/V, while maintaining operation at a reasonable current density that would yield competitive power densities for commercial applications (~ 1 - 5 A/cm^2). The condition for operating at WPE $\geq$ 100% is EQE $\geq V/V_p$. If the LEDs are to be operated at elevated temperature, then a region in the EQE and voltage relationship must be located where the drop in EQE is slower than the drop in voltage, such that the condition EQE $\geq V/V_p$ can be met. The comparative features of today's LED designs with the target designs for WPE $\geq$ 100% are given in Table 4.1 below.

Parameter	State of the art	Requirements for ≥ 100% WPE
Operating V	2.95 V	2.50 V
Operating J	35 A/cm^2	1 – 5 A/cm^2
Operating T	20 – 85 °C	80 - 300 °C
IQE	88%	95%
LEE	87%	95%
Efficiency Droop	-10%	100%
Photon Energy Efficiency V_p/V	96%	111%
WPE	66%	100%

Table 4.1. Comparison of state-of-the-art and target technology for blue LEDs emitting at 450 nm (corresponding to V_p = 2.75 V). The state-of-the-art data is based on the 2016 DOE SSL RDP.[20] The voltage boost in the energy efficiency per photon, V_p/V, that is required to make up for the LED EQE losses for WPE = 100% is approximately 250 mV.

A key challenge of the project is to obtain emitter material with very high IQE > 90% that is optimized for low voltage and high temperature operation. A high peak IQE signals a low SRH recombination rate, which is generally the result of reduced defect sites within the material. This becomes important upon heating, which is one of the possible pathways to reach > 100% WPE. A higher quality epitaxy should, in principle, be more thermally stable because of the reduced density of SRH recombination sites which could become thermally activated. Another benefit of low SRH recombination rate is that the peak IQE will tend to not only shift higher in magnitude, but should also shift to lower current densities (e.g. ~1 A/cm^2 rather than ~3 A/cm^2). This is beneficial because at lower current densities, a larger V_p/V boost can be captured. Thus it is important that the highest quality epitaxial material is developed or obtained for this project.

Another key challenge is to obtain the highest practical LEE. The operation of blue LEDs at relatively low voltage and high temperature opens a new light extraction design space compared to today's designs, which are aimed at high current density, room temperature operation. Simulations presented in Ch. 3 of our optimized mask design and

package demonstrate the feasibility of 95% LEE for a device designed for low current density and heat-sink-free operation. Operation at low current densities and high temperatures alleviates the requirements on high p-doping and thick current spreading layers, which give rise to electrical and light extraction losses. The increased operating temperature decreases the p-GaN resistivity due to higher hole concentration.[21] Lower surface area coverage of metal contacts and thinner ITO are sufficient for uniform current spreading and will result in reduced optical losses. Furthermore, packaging constraints are also alleviated. Most notably, the expensive, bulky heat sink can be eliminated and a high LEE package is demonstrated, which also serves as an adiabatic package to allow the LED to intentionally self-heat.[22]

The following sections will discuss the implementation of these principles and designs to processing and packaging of high efficiency blue nitride LEDs. The main focus will be on components contributing to the LEE, with some discussion of epitaxy selection, voltage, and temperature dependent operation. Results demonstrating thermal pumping in blue nitride LEDs will be presented, along with a demonstration of a device with peak room temperature WPE of 78%. Temperature-dependent trends of the efficiency and electrical characteristics will be presented and compared with the state-of-the-art reports from industry.

4.4. Epitaxial LED Material

The epitaxial material for a low current density, high peak WPE device must have high LEE potential, low voltage, and high peak IQE. Ch. 3 discussed several potential options for high LEE devices, considering both sapphire and GaN substrate architectures. The easiest path to LEE > 95% at low current density operation was to use a PSS

architecture, which is also the most common architecture employed in today's commercial SSL lamps. Apart from high LEE, the substrates are large area and low cost. Growth on these substrates is highly developed, with record-high EQEs[17] despite higher known dislocation densities compared with homoepitaxial growth on bulk GaN substrates. Thus, the efforts herein on 100% WPE focus exclusively on this growth and chip design platform.

Today's LED epitaxy is designed to operate near room temperature at high current densities, while minimizing droop. One of the few practical ways to address efficiency droop is to reduce the carrier densities in the QWs, which is generally done by increasing the number of QWs. Industry LEDs use 8 - 15 QWs to decrease the carrier density and the associated Auger recombination that dominates at high carrier densities. This MQW design, however comes at the cost of increased operating voltage. This application, which calls for low voltage, low current density operation, and thus low carrier density, already eliminates losses from efficiency droop. Theoretically, only a single QW is needed to minimize voltage and maximize carrier density.

In practice, however, reducing the QW number for *c*-plane devices on PSS grown at UCSB resulted in significant reductions in output power (data not shown). Industry studies have also shown reductions in efficiency as QW number was reduced,[23] although at least one very high IQE (90%) single QW structure has been reported.[24] It is possible that dedicated in-house optimizations of single QW LED epitaxy could produce QWs of a quality that can rival modern commercial MQW epitaxy. However, in light of the time-constraints of this project, we decided to use commercially-supplied MQW LEDs for the best chance at obtaining > 90% IQE material and 100% WPE.

4.5. Processing for High Light Extraction Efficiency and Low Voltage

Increasing the LEE to its practical limit is critical to achieving 100% WPE as shown by Eq. 4.1. Modeling of LEE for conventional LED designs using ray tracing methods was described in detail in Ch. 3. The main light absorbing features in PSS LEDs were the metal contacts, ITO spreading layer, and silver header. Advanced designs were envisioned for optimizing the LEE at low current density operation. The following sections will focus on the advanced design for LEDs on PSS, which employed interface patterning, encapsulation, high reflectivity and low surface coverage metals, and a thin ITO layer. Ray tracing simulations estimate that the combined effect of fully optimized light extraction features enables LEE ≈ 95%.

4.5.1. Mask Design

The LED mask was designed to maximize light extraction efficiency by minimizing the metal contact surface coverage, moving the wire bonding pads off the LED mesa, and including a reflective dielectric layer beneath the bond pads to minimize absorption, while still maintaining adequate current spreading. The interdigitated metal design provides consistent current spreading distances compared to the previous design which required a thick ITO layer. Table 4.2 presents the differences between the present design, "Advanced Chip A" and prior "High *J* Design" as well as a more aggressive design "Advanced Chip B."

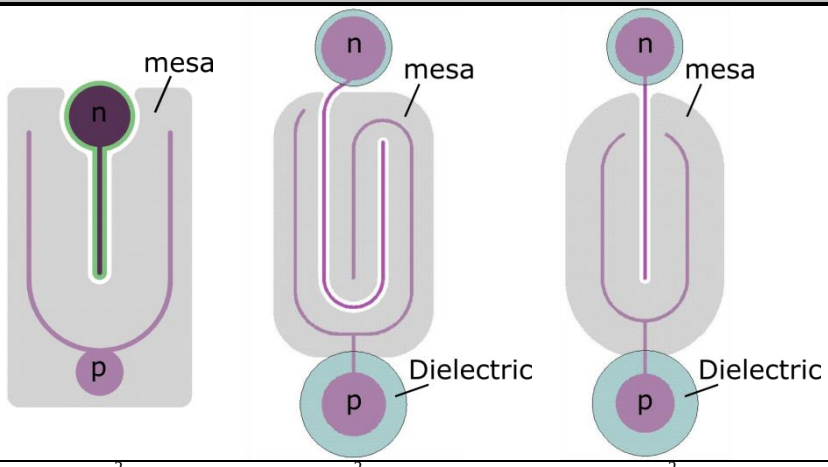
Parameter	High *J* Design	Advanced Chip "A"	Advanced Chip "B"
Mask Design			
SA of emitting material	0.098 mm^2	0.100 mm^2	0.100 mm^2
SA of n-contact	7670 μm^2	3660 μm^2 (not on SiO_2)	1650 μm^2 (not on SiO_2)
SA of p-contact directly above light emission	9010 μm^2	6220 μm^2	4040 μm^2
Ratio p-contact: emitting SA	9.17%	6.11%	4.03%
LEE Simulation Results	82%	95% (including all other package optimizations)	>95% (including all other package optimizations)

Table 4.2. Details of the advanced chip design compared to the previous high current density chip design.

All three chip designs have an etched mesa architecture with an emitting surface area of 0.1 mm^2. There is no light emission directly below the n-contact, which is recessed from the mesa. In the advanced designs, the wire bonding pads were moved off and away from the mesa to minimize direct absorption under the p-pad and indirect absorption under the n-pad. This design change also helps to reduce shadowing from the wires themselves after packaging. A dielectric insulating layer is required beneath the p-pad to prevent an electrical short (blue layer in Table 4.2). This layer also serves as a dielectric reflector and further reduces absorption on the metal pads, which is why it is also employed beneath the n-pad even though it is not electrically required.

The advanced designs have smaller and more uniform distances between the p-contact and the mesa edge compared to the High *J* Design, which helps to improve current spreading without adding undue optical absorption. The reduced current density operation allows for thinner contact stripes. The advanced designs use 5 μm wide contacts compared to 7 μm (p-contact) and 21 μm (n-contact) wide contacts in the former design. The surface area coverage of the p-contact above direct QW emission is reduced from the High *J* Design (~9%) to the Advanced Chip A (~6%) compared to the 0.1 mm^2 emitting area. The Advanced Chip B pushes the design even further to just ~4% surface area coverage. The n-contact area does not have as large an overall effect on the extraction efficiency (see Ch. 3), however, the advanced designs also reduced the exposed surface area of the n-contact approximately to 50% and 20% of the original surface area for the chip designs A and B, respectively.

Ray tracing simulations were performed to compare the High *J* and Advanced designs. The details of the simulation results for the High *J* design were tabulated in Ch. 3 in Table 3.5 ("Encapsulated PSS Chip Losses") and for Advanced Design A in Ch. 3 in Table 3.8 ("PSS(%)"). A ray tracing simulation was not performed for Advanced Design B, but is expected to have a modest improvement compared to Advanced Design A, particularly in the n- and p-metal absorption. The results include all other optimizations to the processing and package (e.g. thin ITO, 99% diffuse reflective header, highly reflective contact metals) which will be discussed in the following sections.

4.5.2. ITO Thickness

As discussed in Ch. 3, the ITO thickness and its absorption coefficient have a significant effect on the total LEE of blue PSS LEDs. The ITO thickness that is required for adequate current spreading depends on several factors including the ITO conductivity, the p-GaN conductivity, the intended operating current density and temperature, and the mask design (maximum distance the current must travel from the p-metal contact).

An ITO thickness series was performed to experimentally determine the minimum ITO thickness for operation at low current density $J \sim 1 - 5$ A/cm^2 considering room temperature or heated operation and Mask Design A with a maximum p-current spreading distance of 40 μm (70 μm for Design B) This series was performed on wafers quartered from a two inch UCSB-grown *c*-plane on PSS LED wafer (sample ID: C160217AD). The sample was grown by MOCVD with 1 μm UID GaN, 3 μm n-GaN, followed by a 30-period n-doped 1.9 nm $In_{0.02}Ga_{0.98}N$/ 1.5 nm GaN superlattice underlying a six-period MQW with 2.7 nm QWs and 15 nm quantum barriers. The active region was followed by a p-doped 9 nm EBL and 230 nm of p-GaN capped with a p++ contact layer. The UID buffer and n-GaN layers were grown in TMGa gallium precursor and the remaining layers were grown in TEGa gallium precursor with indium and aluminum precursors, TMIn and TMAl, respectively. The group V precursor was NH_3.

The sample had quick test powers and voltages of 0.4 - 0.42 mW and 3.6 - 3.9 V at 1 A/cm^2 (6.8 - 7.3 mW and 5 - 5.5 V at 20 A/cm^2). The sample was quartered and processed with four ITO thicknesses. The ITO was deposited by heated substrate e-beam deposition.[25] The final thicknesses were obtained by ellipsometry with a Woollam M2000DI Ellipsometer on co-loaded silicon monitors and were 0 nm, 33 nm, 70 nm, and

83 nm. The samples were co-processed for a self-aligned ITO methane-hydrogen-argon (MHA) reactive ion etch (RIE) followed by a Cl_2 inductively coupled plasma (ICP) GaN mesa etch.

The effect of ITO transparency is shown qualitatively in Fig. 4.2 in optical microscope images with a constant camera integration time of 28 ms. The thicker ITO samples were qualitatively more opaque than the thinner ITO or ITO-free samples, as expected.

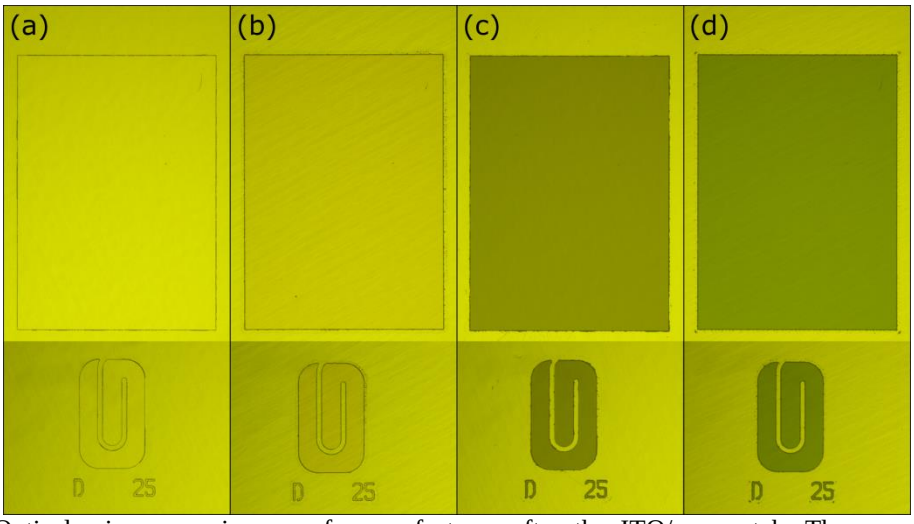


Figure 4.2. Optical microscope images of mesa features after the ITO/mesa etch. The samples had ITO thicknesses of (a) 0 nm, (b) 33 nm, (c) 70 nm, and (d) 83 nm. Images were taken with a 28 ms camera integration time.

After dielectric insulator deposition (SiO_2) and metal deposition (Ti/Al/Ni/Au annealed n-contact and Cr/Ni/Au p-contact), the completed devices were measured by electroluminescence (EL) on-wafer at an input current density of 1 A/cm^2. Luminescence images were taken to inspect the current spreading effectiveness of the respective ITO thickness. The images are shown in Fig. 4.3.

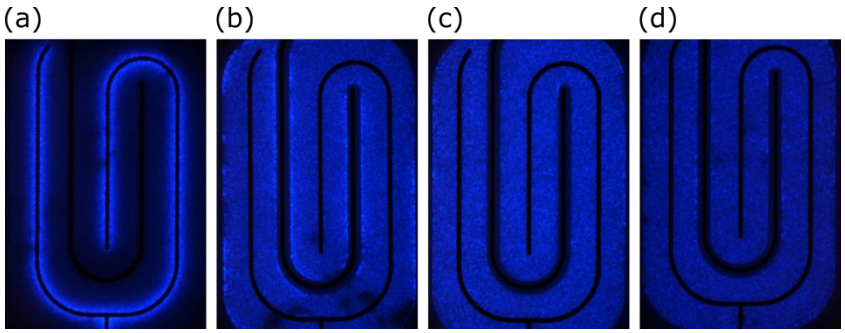


Figure 4.3. EL images of on-wafer LEDs with ITO thicknesses (a) 0 nm (b) 33 nm (c) 70 nm (d) 83 nm under 1 A/cm^2 injection. Images were all taken at room temperature with 1 ms integration time.

Figure 4.3. (a) shows inadequate current spreading in the absence of an ITO current spreading layer. The p-GaN conductivity is insufficient to provide current spreading across the 40 μm spreading distance. This results in luminescence clustered close to the p-contact, and not extending to the mesa edges. Fig. 4.3. (b)-(d), however, all show adequate current spreading with the luminescence extending to the mesa edges without apparent reduction in intensity. The bright areas at some locations at the mesa edges are attributed to roughness and higher local light extraction efficiency. The areas of non-uniform emission are attributed either to epitaxial nonuniformities or to poor ITO wetting with the heated substrate deposition method (the process was later changed to a room temperature deposition followed by an anneal).

Electrical and optical measurements including the IV characteristic and the backside light emission were also taken for 10 - 14 die on each of the four samples. The light was collected from the backside emission with a silicon photodetector. Results of the voltage and backside output power are shown as a function of ITO layer thickness in Fig. 4.4.

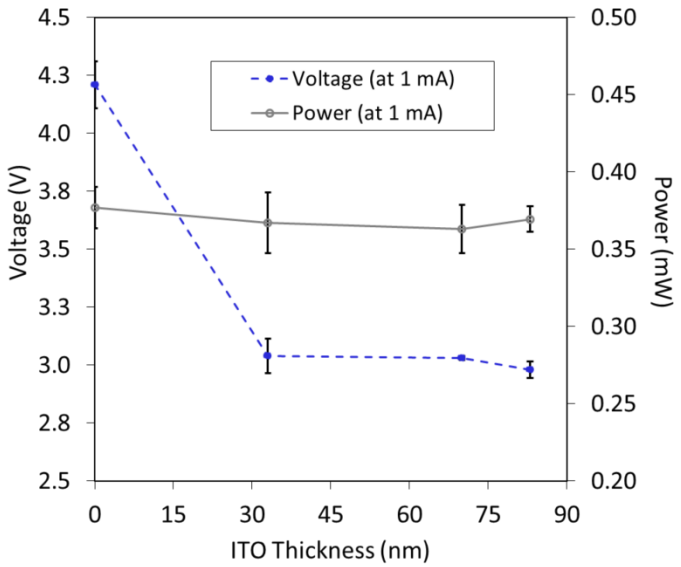


Figure 4.4. Voltage and backside emission output power for the ITO thickness series LEDs. The data points are average values and the error bars represent +/- the standard deviation. The data set represents measurements of 10, 10, 14, and 11 LED die for the 0, 30, 70, and 83 nm ITO samples, respectively.

For the range 33 - 83 nm, there was not a significant dependence of V on ITO thickness. However, 0 nm of ITO led to a spike in the voltage. This accompanied the poor current spreading observed in Fig. 4.3.(a) There was not a significant increase in output power observed for the thinner ITO samples. It may be that the experiment was not sensitive enough to the change in transparency of the ITO layer because the emission was measured from the backside of the on-wafer devices. Overall voltages measured here were high compared to commercial devices, but not unexpected considering the similarly high quick test voltage for the unprocessed UCSB epitaxy (~3.7 V at 1 A/cm^2) compared to that of typical commercial unprocessed epitaxy (~3.0 V at 1 A/cm^2).

We conclude that even for low current density operation, some ITO is required for current spreading, but as little as 33 nm was sufficient. An ITO thickness of 33 nm performed equally well to a thickness of 83 nm at 1 A/cm^2. Additional refinements of this experiment (not shown) allowed us to hone the minimum value further. A 15 nm ITO layer was observed

to have significant current crowding, while 24 nm had similar results to 33 nm. Thus 24 nm was decided as the lower limit of the ITO thickness for this mask design.

4.5.3. Metal Reflectivity

Previous mask designs and processing schemes required lower reflectivity contact metals including Ti and Cr for their adhesion properties. If the wire-bonding p-pad is deposited directly on the mesa, as in the "High *J* Design" shown in Table 4.2. , then adhesion to ITO can be problematic. A Cr process was adopted because of the relatively strong adhesion compared to more reflective metals such as Al or Ag.

In the advanced designs, the adhesion problem was solved by using off-mesa dielectrics with either SiO_2 or Al_2O_3 top layers which both have improved adhesion to Al compared to ITO and are sufficient for wire bonding purposes.

The n-contact that was previously in use was a Ti/Al/Ni/Au annealed contact. The Ti anneal produces an ohmic contact to GaN. This effect has been attributed to at least two origins: production of a low work function TiN semimetallic interfacial compound, and the generation of donor-type nitrogen vacancies in the contact layer.[26] An annealed Ti contact was found to reduce contact resistance compared to unannealed contacts for the case of a moderate to low-doped n-GaN contact layer, which was etched with Cl_2 chemistry by ICP or RIE.[27]

Etching in $SiCl_4$ chemistry was previously shown to reduce contact resistances,[28] which was attributed to its contribution of surface Si donor states. The use of this etch chemistry at UCSB (developed and tested by B. Yonkee [27]) enabled a low contact resistance Al n-contact. Thus, Al/Ni/Au was adopted for both n-contact and p-contact,

eliminating a mask layer, a deposition step and an anneal compared to the "High *J* Design," while increasing adhesion, increasing reflectivity, reducing absorption, and enabling easier wire bonding.

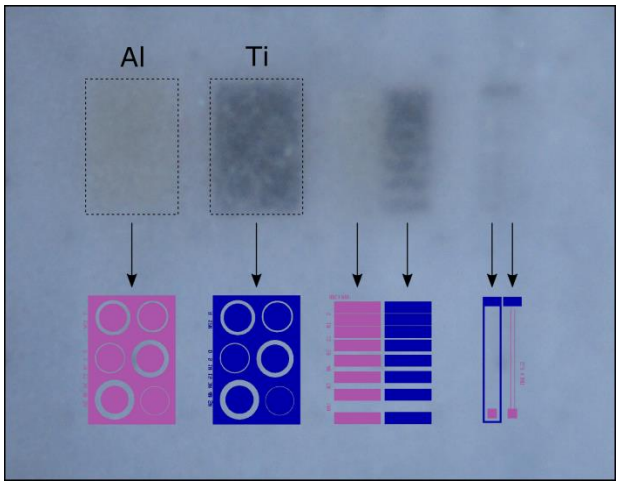


Figure 4.5. Optical microscope image taken through the unpolished sapphire substrate of an LED wafer to show the metal reflectivity from the perspective of the QW emission. Dotted boxes are overlaid on the first two TLM patterns to guide the eye. The mask design is overlaid on the bottom of the image to show which regions are high reflectivity Al/Ni/Au (pink) and which are low reflectivity Ti/Al/Ni/Au (blue).

Measured reflectivity at 450 nm of the annealed Ti/Al/Ni/Au and Al/Ni/Au on *c*-plane GaN were 73% and 85%, respectively.[27] The qualitative difference between the two metal stacks is also apparent in Fig. 4.5 which is an optical microscope image taken through the backside of the unpolished sapphire substrate. The metal corresponding to the pink overlaid mask pattern is Al/Ni/Au whereas the metal corresponding to the blue overlaid mask pattern is the annealed Ti/Al/Ni/Au.

4.5.4. Dielectric Insulator

The dielectric insulator (blue layer in the advanced designs shown in Table 4.2) serves two purposes. The first is to prevent an electrical short which would result from

moving the wire bonding p-pad off the mesa and onto the recessed n-GaN layer. Another important feature of this layer is to provide a lossless dielectric reflector beneath the metal pads. This enhances the reflectivity and reduces absorption on the metal pads.

Two dielectric insulating layers were compared for otherwise co-processed LEDs with Advanced Design A on pieces from the same epitaxial blue LED wafer on PSS from Epistar. The first was a simple sputtered 300 nm SiO_2 layer. The second was a multilayer dielectric stack containing Al_2O_3, Ta_2O_5 and SiO_2 deposited by ion beam deposition (IBD) that was modelled in TF-Calc software, assuming an Al metal contact for omnidirectional reflection > 98% at 450 nm (mirror stack design courtesy of Benjamin Yonkee). Al was used for both the n- and p-contact layers. The details regarding the deposition are given in the process traveler in App. B. Fig. 4.6. shows optical microscope images of the topside of the finished devices where the insulator material is visible.

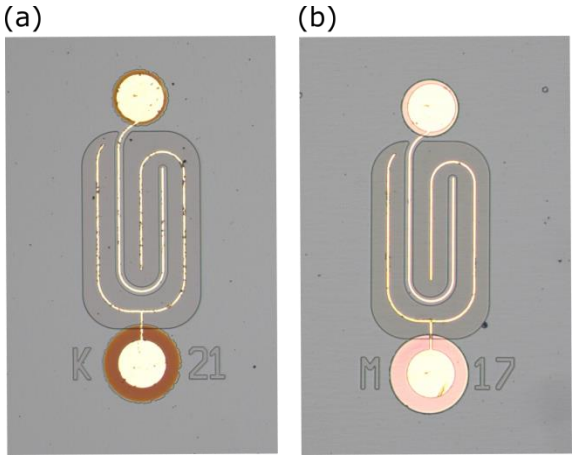


Figure 4.6. Topside optical microscope images of the sample with (a) 300 nm SiO_2 dielectric and with (b) a multilayer dielectric stack.

After processing, the devices were tested on--wafer with backside emission collection by a silicon photodetector at an input current density $J = 3$ A/cm^2. Table 4.3. shows a higher

average backside emission power with the multilayer dielectric stack than with the SiO_2 layer. This indicates a higher reflectivity of the multilayer stack.

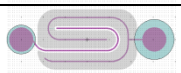
Epitaxy Source	Mask Design	Dielectric Layer	*V* (V)	*P* (mW)	λ (nm)
Epistar		SiO_2	2.67 (±0.003)	1.36 (±0.017)	449
Epistar		Multilayer Stack	2.68 (±0.006)	1.43 (±0.025)	449

Table 4.3. Comparison of backside light emission for samples with SiO_2 vs. a multilayer dielectric stack beneath the wire bonding pads. Average values are given with standard deviations given in parentheses as the measure of variability. Results were based on measurement of 22 die in the case of the SiO_2 sample and 29 die in the case of the multilayer stack.

The wafers were singulated, and the brightest on-wafer devices from each sample were mounted on a white header, wire bonded, and measured in the integrating sphere (unencapsulated). The results of the packaged device comparison, which are given in Table 4.4, were less conclusive.

Die Number	Dielectric Layer	*EQE unencapsulated*	*EQE encapsulated*
K20	SiO_2	68.4%	74.6%
O18	SiO_2	69.7%	75.8%
K18	Multilayer Stack	67.4%	74.8%
M20	Multilayer Stack	68.4%	n/a
M19	Multilayer Stack	75.2%	75.0%

Table 4.4. EQE results for packaging the dielectric comparison.

The encapsulated EQEs were similar. One sample with the multilayer dielectric stack had much higher unencapsulated EQE, but actually lost efficiency upon packaging. The most efficient sample was one with the sputtered SiO_2 dielectric layer. More data are needed to understand if the higher reflectivity of the multilayer dielectric stack translates to higher

efficiency in a packaged LED with integrated emission collection. This is a topic of future work.

4.6. Packaging Research and Development

The LED package is often the site of significant optical losses, including losses from the metallic header or reflector cup which also often serves as a heat sink, as well as wire bonds, which may shadow emission and/or absorb reflected light. It was proposed in Ch. 3 to replace the silver header with a 99% diffuse reflective header for LEDs that are intended for low current density operation. The mask design modelled there and employed in this chapter also helps reduce wire bond absorption by moving the bonding pads off the mesa.

The reflectance and transmittance of white diffuse reflective materials were investigated to determine their suitability as low-loss coatings for LED headers. These materials included an integrating sphere coating liquid, a white acrylic craft paint, and $BaSO_4$ powder in a silicone matrix. The Avian B pre-mix, produced by Avian Technologies, is a $BaSO_4$-based material used for integrating sphere coatings. The Avian B liquid was dip coated by hand onto a glass slide for measurement. The acrylic paint is a typical white craft paint produced by Craft Smart that was poured onto a glass slide. $BaSO_4$ powder is a known high diffuse reflectivity material. A powder purchased from Fisher Scientific was mixed into a silicone matrix (n = 1.4) and spread onto a glass slide with a spatula.

A Shimadzu UV-3600 UV/Vis/NIR spectrometer was used with an integrating sphere to capture reflectivity of diffuse materials. The diffuse reflectance spectrum was determined by comparing the light intensity at the integrating sphere detector for the baseline configuration compared with the sample configuration (Fig. 4.7. (left)). The baseline

configuration for diffuse reflection is a $BaSO_4$ packed powder plate that attaches perfectly flush to the integrating sphere port. Thus, it is very important that the measurement configuration puts the sample material in as perfect a position as possible.

Escaped light events were a common experimental problem caused by imperfect opacity of the sample (light escapes through transmission), imperfect mounting position (light escapes through scattering at the edges of the port), or improper sample size (sample too small to completely cover the port and light escapes at the edges). Thus, the measurements shown in Fig. 4.8. should be considered minimum values compared to the perfect $BaSO_4$ packed powder plate.

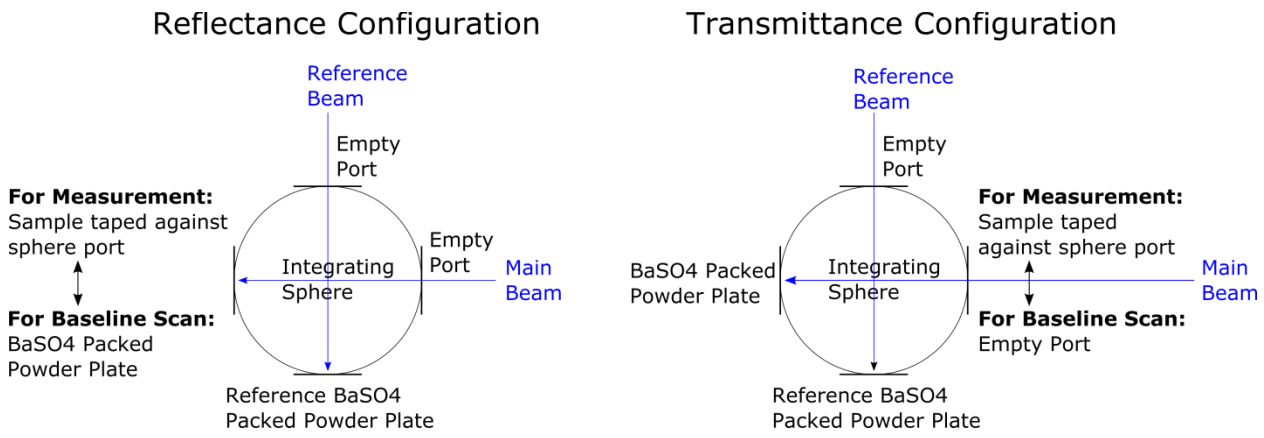


Figure 4.7. Shimadzu UV-3600 UV/Vis/NIR configurations for (left) reflectance and (right) transmittance measurements.

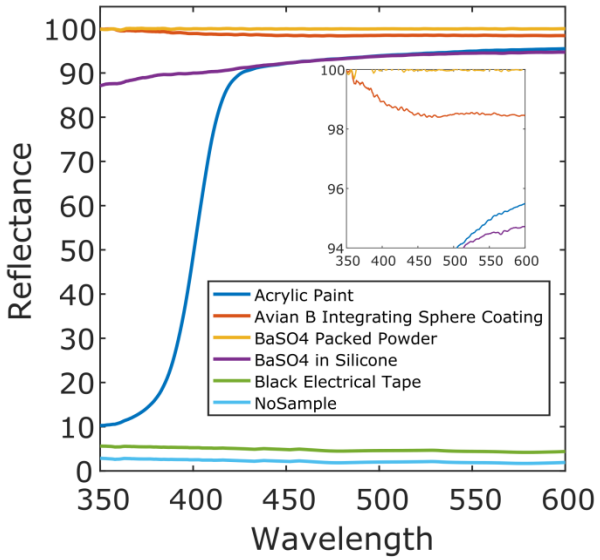


Figure 4.8. Diffuse reflectance spectra for some common materials. The Avian B integrating sphere coating had the most perfect reflection compared to the $BaSO_4$ packed powder baseline material.

The $BaSO_4$ packed powder baseline material was 100% reflective, as required by the measurement procedure. The acrylic paint was 92.2% reflective at 450 nm and showed a strong absorption tail in the violet, which is the absorption signature of the acrylic matrix. The $BaSO_4$ in silicone was only 92.2% reflective. This low value is attributed to the sample configuration. The silicone caused the sample to have a convex shape, which was difficult to push flat against the sphere port. Some escaped light was observed by eye, suggesting an artificially low measured reflectivity. Finally, the Avian B integrating sphere coating was 98.5% reflective at 450 nm. The sample was flat and pushed as well as possible against the sphere port, but should still be considered a minimum possible value due to the difficulty of eliminating light escape paths in the sample mounting procedure.

Separate transmittance measurements were performed on the same samples to ensure sample opacity. The transmittance measurement configuration is shown in Fig. 4.7. (right). Black electrical tape was used as the zero transmittance reference. The measurement was also

double checked with an air measurement (100% transmittance). Fig. 4.9. shows that the $BaSO_4$ in silicone transmitted < 1% of the impinging light. The Avian B sample was even more perfectly opaque, tracking the noise level of the black electrical tape measurement.

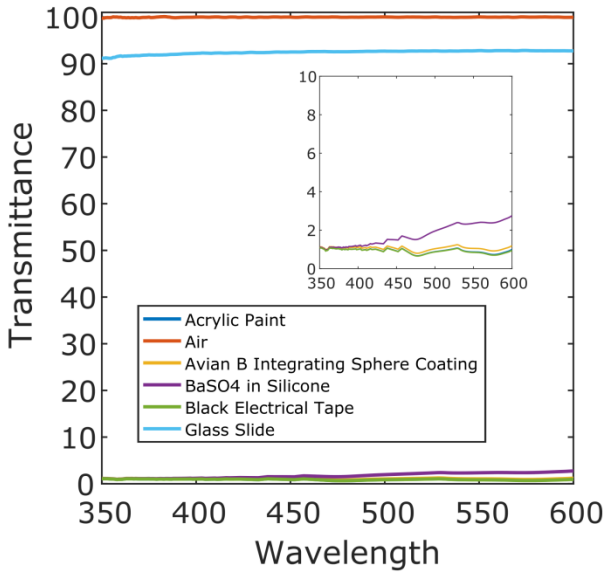


Figure 4.9. Transmittance spectra showing <1% light transmission for the $BaSO_4$ in silicone and Avian B samples. Black electrical tape serves as the 0% transmittance reference.

The Avian B integrating sphere coating was selected for the advanced package because of its very high reflectivity, its ease of application (dip coating), and its production for use as a high reflectivity coating. Fig. 4.10. compares two headers, one dip coated with Avian B, and the other an uncoated silver header. In the case of the coated header, the metallic leads are each protected with a drop of silicone, which was cured prior to dip coating. After coating the Avian B, the protective silicone was removed so as to reveal the metallic wire bonding leads.

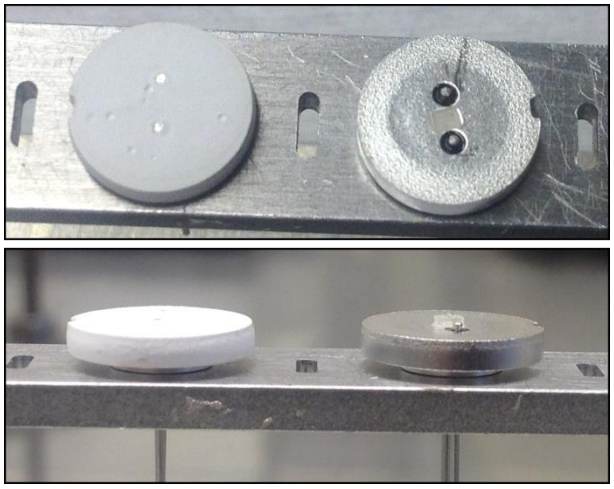


Figure 4.10. Image showing the difference in reflectivity between (left) a header dip coated with Avian B, a diffuse reflective integrating sphere coating, versus (right) an uncoated silver header.

4.7. Evidence for Thermal Pumping in Nitride LEDs

At typical high current density operating conditions, $V > V_p$ and V_p/V is less than unity. However, nitride LEDs are known to turn on at operating voltages below the photon voltage ($V < V_p$) due to population of localized states and the finite ambient temperature which provides additional energy to promote carriers to the QW energy levels. Fig. 4.11. shows images of the room temperature turn on at very low currents corresponding to current densities for the 0.1 mm^2 chip area of (3×10^{-4} - 8×10^{-4} A/cm^2). The LED is electroluminescent at a voltage as low as 2.28 V, which is a remarkable > 0.5 V less than photon energy, $V_p = 2.85$ V. This wafer was processed with the "High *J* Design" with 110 nm of ITO.

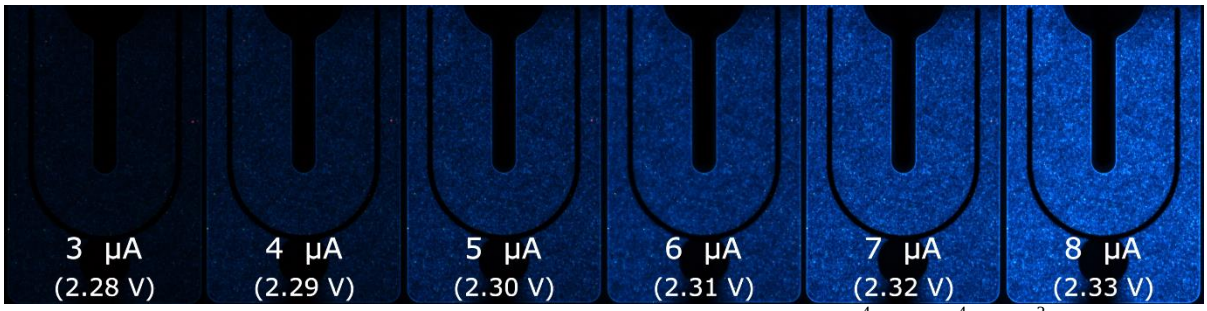


Figure 4.11. Optical microscope images of the electroluminescence at 3×10^{-4} - 8×10^{-4} A/cm^2 . The images were taken at room temperature with a constant integration time of one second.

The measurement was repeated on the same device at elevated temperature using a hot plate set to 100 °C. This produced much darker images (not shown) due to increased non-radiative recombination. However, a significant reduction in the voltage was also observed and is shown in Fig. 4.12., with a diode turn-on in at just 2.0 V. The average reduction in voltage over the 19 different current densities was 0.24 V.

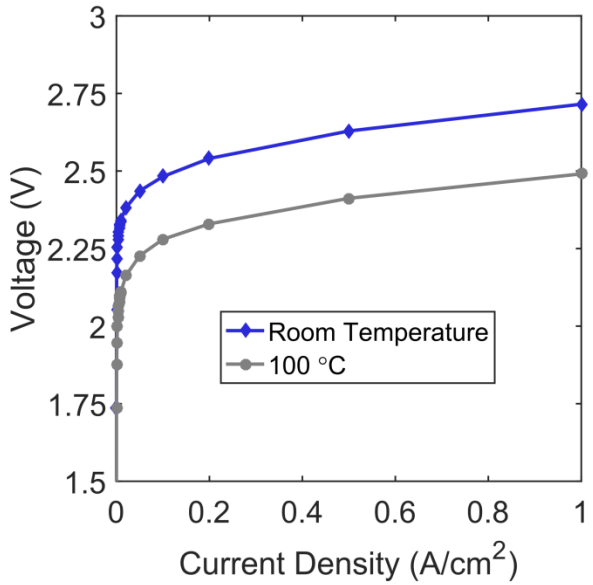


Figure 4.12. JV curves for the room temperature and 100 °C heated die. The voltage decreases as a result of heating by an average of 0.24 V (±0.03 V standard deviation) for these 19 data points.

The voltage often remains below the bandgap value until current densities in the realm of several A/cm^2. Fig. 4.13 shows the room temperature V_p/V vs. J curves for several devices including UCSB, Powerway and Epistar material processed and packaged at UCSB

with Advanced Design A, a commercial fully packaged device from OSRAM measured at UCSB, and a recent literature result from Soraa[29]. These different devices have similar voltage performance at low current densities (~ 1 A/cm^2). The shaded area indicates the region where greater than unity V_p/V occurs and where ≥ 100% WPE could occur if the EQE is sufficiently high. The onset of this region at room temperature is at current densities less than 3 – 12 A/cm^2.

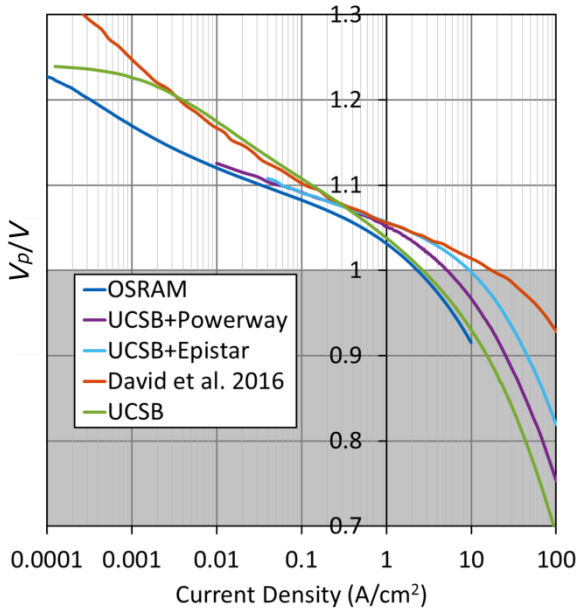


Figure 4.13. The room temperature voltage ratio V_p/V as a function of current density. The V_p/V is greater than 100% where the curve is > 1 on the y-axis. This corresponds to current densities less than 2.5 A/cm^2 - 20 A/cm^2. Most peak EQE values occur between 2 and 5 A/cm^2, which means that in many cases, the peak EQE will occur at a point where the V_p/V > 100%. In those cases, the peak WPE will exceed the peak EQE.

In the case of high quality (low SRH recombination, high IQE) LED material, the peak IQE is 2 – 5 A/cm^2 for commercial devices, which usually falls within the thermal pumping regime. This allows for a peak WPE that exceeds the peak EQE. The crossover point where WPE = EQE is when V/V_p = 1 or in other words, when the photon voltage equals the applied voltage. Fig. 4.14 shows the integrating sphere measurements of WPE, EQE and

V/V_p of a device processed and packaged at UCSB from a commercial blue epitaxial wafer supplied by Epistar. It reaches a peak WPE of 78.1% at 3.45 mA and 2.68 V. The peak EQE is 75.8% and is reached at 5.5 mA and 2.71 V. For a peak emission wavelength of 448.4 nm, this corresponds to a room temperature V_p/V = 103%. At this peak operating point, the LED produces 7.2 mW of output power.

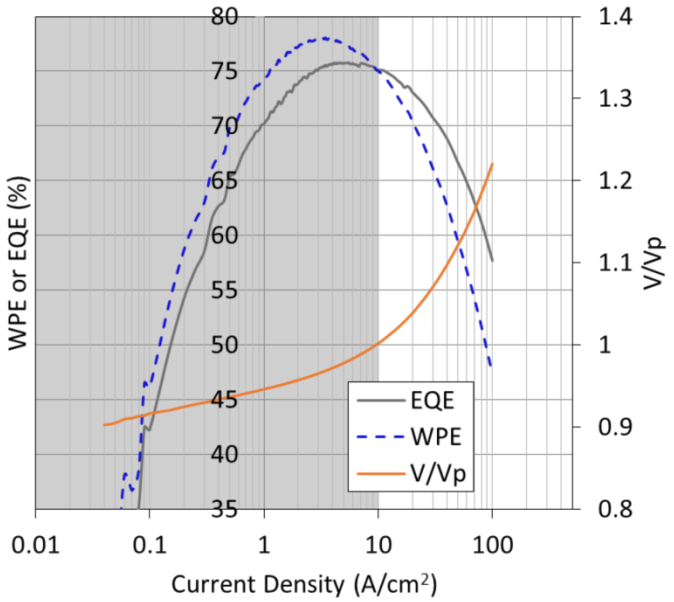


Figure 4.14. Epistar material processed and packaged at UCSB with " Mask Design A" showing the WPE, EQE, and V/V_p as a function of current density (plotted on a logarithmic scale). The peak WPE reaches 78% at room temperature and is accompanied by V_p/V = 103%.

A further reduction of the forward voltage V can be accomplished by heating the sample (or allowing it to self-heat from its own inefficiency by enclosing it in an adiabatic package). Heating also induces a drop in the IQE by thermally activating SRH recombination centers. The key is to find a current density operating regime where the IQE drops slower than the voltage ratio. Fig. 4.15 shows a temperature-dependent measurement of a sample processed with Design A on a blue epitaxial wafer from Powerway.

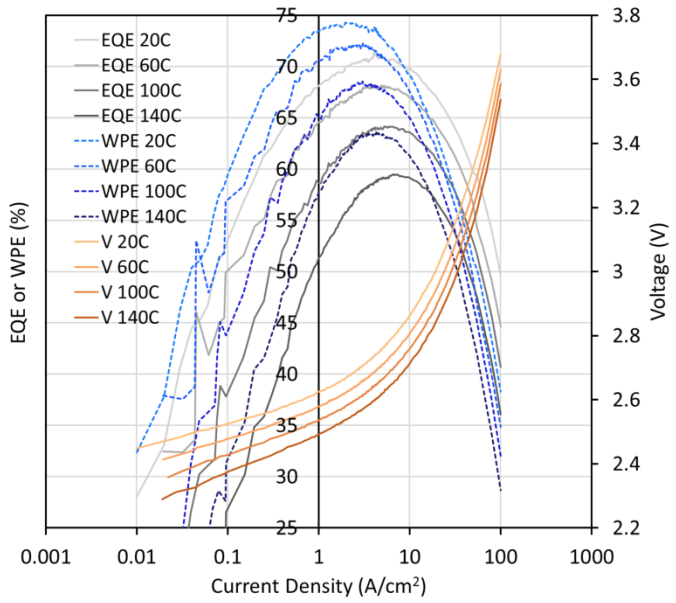


Figure 4.15. Increasing stage temperature results in a decrease in the LED operating voltage as well as a decrease in peak EQE. The peak WPE drops slower than the peak EQE.

The EQE drops faster than the WPE with increasing temperature due to the compensation from the reduced voltage. However, the WPE still drops very quickly. The condition for 100% WPE is that EQE = V/V_p. Thus, we can present the data in a graph of EQE vs. V/V_p, where the diagonal indicates the threshold for 100% WPE operation. The curves can move in any combination of leftward or upward directions to reach the threshold. In the case of prior demonstrations of > 100% WPE, the LEDs were operated in a low bias regime with very small EQE and very small voltage. Thus, the WPE curves crossed the threshold level very near to the origin.

In the nitrides, we aim to achieve 100% operation at current densities much closer to the maximum EQE (~ 1 – 5 A/cm^2). This would make the 100% WPE blue LED relevant for commercial devices. Fig. 4.16 plots several curves from UCSB and from the literature to indicate the status of today's LEDs.

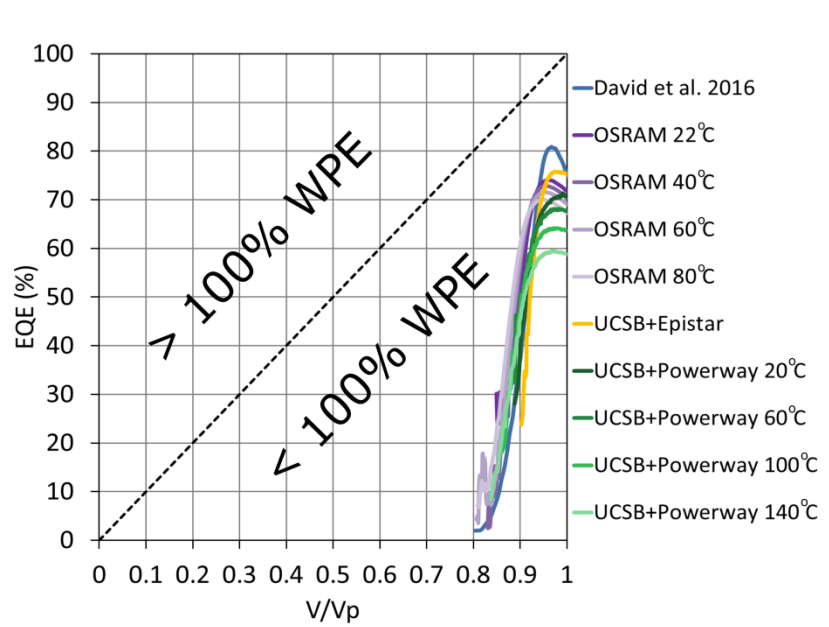


Figure 4.16. EQE vs. V/Vp for several devices. The dashed black line indicates the threshold for >100% WPE operation.

Figure 4.16 includes some temperature-dependent measurements. It appears that the WPE drops with increasing temperature faster than it moves leftward. This indicates that once EQE and voltage opportunities at room temperature are saturated, it might be more feasible to cool slightly to promote the curve over the threshold rather than to heat.

The EQE is the product of the LEE and the IQE. Our best design produced EQEs in the range of 73 - 76% using Powerway and Epistar material. It was not known if LEE was still the limiting factor for the overall efficiency or if IQE had become the dominant source of inefficiency.

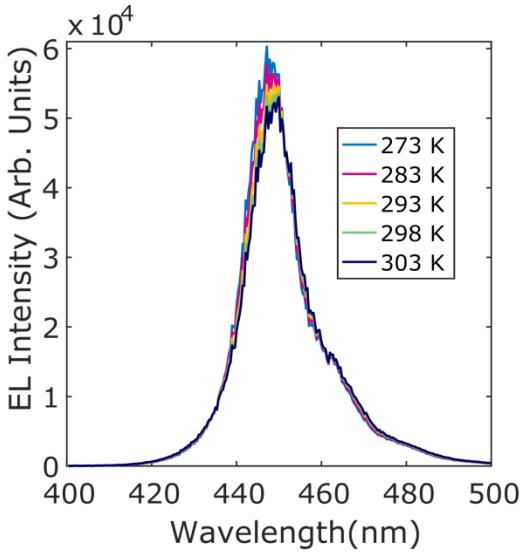


Figure 4.17. EL measurements show a reduction of EL intensity of 9 % from 273 K to room temperature, 298 K for Powerway blue epitaxial material. This indicates an IQE which is far-from-unity. The Powerway blue material produced a best peak room temperature WPE of 76.2%, compared to the best die from Epistar (WPE = 78.1%).

Figure 4.17 shows measurements of the EL intensity for temperatures from 273 K to 303 K for an on-wafer Powerway die. The EL intensity is reduced by about 9% from 273 K to room temperature, 298 K. This indicates that the IQE is far-from-unity for this epitaxial material. The Powerway material was nearly as good as the Epistar material, reaching a best peak WPE of 76.1% encapsulated (n=1.4) die compared to 78.1% for the best encapsulated (n=1.5) Epistar die. This implies that the IQE of the epitaxial material is likely still a limiting factor for the overall efficiency.

4.8. Future Work

Only a few reports of > 80% WPE have been published for industry hero LEDs in the violet to blue wavelength range.[16,17] The world record WPE for a blue-emitting LED currently stands at 81.3%.[17] The best WPE achieved in this work was 78.1% using

commercial blue MQW Epistar material and a process and package designed for low current density, low power operation.

Future work should extract the few remaining options for LEE improvement including accessing higher reflectivity Al metal and investigating new ITO source material for high transparency and high conductivity. Advanced Design B is an aggressive high LEE etched mesa design, which in an initial on-wafer test with 24 nm ITO had slightly higher voltage than devices co-processed using Advanced Design A. With better ITO, Advanced Design B may reduce remaining absorption losses even further while maintaining similarly low voltage.

It is anticipated that with the available epitaxial wafers, mask design, and process, if executed with the most recent optimizations (see App. B and D), can produce die that exceed 80% WPE. This is an anticipated near-term outcome of this project and may put world record WPE values within reach.

The possibility of reaching 100% WPE still requires substantial improvements. Some further LEE improvements will be required as discussed, and major improvements in the material IQE will be necessary. Furthermore, these optimizations must be made for materials designed for low current density, low voltage operation. This most likely means moving to single QW and EBL-free designs. The current epitaxial and contact design achieves $V_p/V = 103\%$ at the peak WPE. However, to recoup realistic losses in EQE, a $V_p/V \geq 110\%$ must be achieved, as outlined in Table 4.1.

Once IQE and LEE enhancements are taken to their practical limits, both heating and slight cooling (the cooling range must maintain V_p/V above unity) options should be investigated to help boost the curve over the 100% WPE threshold (Fig. 4.16).

4.9. Conclusion

This work has investigated a low current density, low power operation regime for blue LEDs that has so far not been seriously considered for commercial applications, but which opens up opportunities for ultra-high WPE. The WPE enhancement occurs in all three of its component efficiencies: the IQE, the LEE, and the photon energy efficiency, V_p/V.

First, we can choose to operate at the peak IQE (~ 1 – 5 A/cm^2), where bimolecular radiative recombination is the dominant recombination mechanism, and the efficiency droop losses are circumvented. Second, the design space for high LEE LEDs is opened for low current density because of the alleviation of thermal and electrical constraints otherwise associated with the flow of large currents in the materials. This includes reduced constraints on metal contact size, current spreading layer thickness and metallic heat sink. These enhanced designs produce ~95% LEE in LED ray tracing simulations. Finally, thermal pumping effects are readily observed in this operation regime where the photon voltage is higher than the injected carrier voltage, $V_p/V > 1$, enabling some of the EQE losses to be recouped.

Further opportunities exist to enhance V_p/V by optimizing the epitaxial material for lower current density operation. These include removing heterostructures designed to reduce efficiency droop (multiple QWs) or prevent carrier overflow (EBL). If these changes can be produced while maintaining exceptional material quality (IQE > 90%), then ultra-high WPE becomes available, including the standing possibility of a $\geq$ 100% WPE blue LED.

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Appendix A. Eyelet Pit Defects in Double Miscut and a-Miscut *m*-Plane GaN Template Growth

A.1 Eyelet Pit Formation in Double Miscut Homoepitaxy

Outstanding emission characteristics including narrow PL and EL linewidth have been demonstrated for LEDs grown on double miscut substrates, particularly for substrates with *a*+*c* miscuts exceeding 0.75°.[1] These results were achieved in spite of eyelet pit defects that emerge during homoepitaxial template growth over a wide range of growth conditions for substrates containing intentional **a**-miscut. This appendix discusses the characterization of these defects and methods for reducing their impact on devices.

The double miscut studies discussed in Chapter 2 were based on observations of natural *a*+*c* step directions in homoepitaxial growth on -1 °**c**-miscut, 1 °**a**-miscut and on-axis *m*-plane substrates. The ratio of the **a**- and **c**-components in the double miscut substrates was selected based on the AFM step direction on the *a*-face of an on-axis *m*-plane pyramid (Fig. A.1.). The step angle is ~52°, as shown in Fig. A.1. (b), and from this a ratio of **a**/**c**=1.28 was calculated.

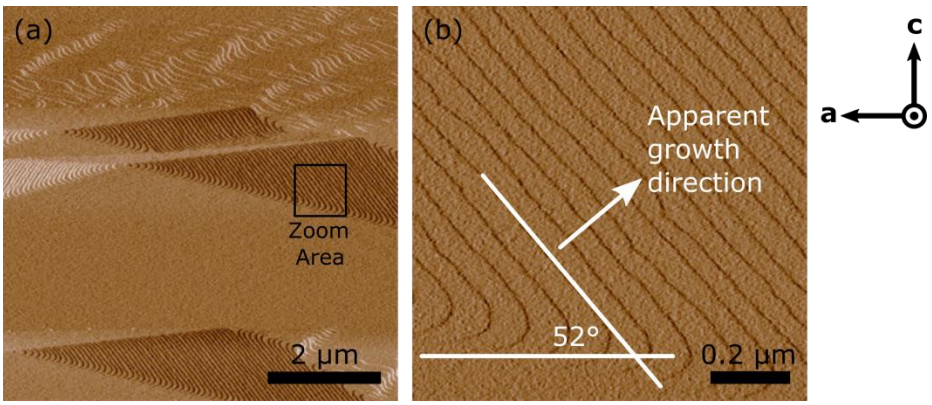

Figure A.1. AFM images of the step direction on on-axis *m*-plane pyramids, which formed the basis for the selection of nominal double miscut orientations. A large area scan in (a) shows a pyramid and the black box denotes the zoom area corresponding to the image in (b). In (b), a step angle of 52° is measured, corresponding to an **a**/**c** ratio of 1.28. Adapted from [2] with permission.

Bulk GaN substrates were acquired from Mitsubishi Chemical Company (MCC) with miscuts in this approximate **a**/**c** ratio, in both the +**c** and –**c** direction with a range of miscut magnitudes up to 2°. Six miscut orientations were originally selected. The nominally requested miscut values and the actual values (which deviate within MCC's specifications) are listed in Table. A.1.

Nominal Miscut	Actual Miscut
0.5 °**a**, 0.375 °+**c**	0.51 °**a**, 0.21 °**c**
1.0 °**a**, 0.75 °+**c**	0.99 °**a**, 0.71 °**c**
2.0 °**a**, 1.5 °+**c**	2.00 °**a**, 1.41 °**c**
0.5 °**a**, 0.375 °-**c**	0.49 °**a**, -0.36 °**c**
1.0 °**a**, 0.75 °-**c**	1.01 °**a**, -0.84 °**c**
2.0 °**a**, 1.5 °-**c**	1.94 °**a**, -1.50 °**c**

Table A.1. Nominal and actual double miscuts from MCC based on AFM images of step structure in the on-axis *m*-plane pyramid.

Homoepitaxial growth studies were performed to assess the surface morphology of the double miscut growth. The six double miscuts were co-loaded in a two-flow atmospheric pressure metalorganic chemical vapor deposition (MOCVD) reactor with standard -1° **c**-miscut, +1° **a**-miscut, and +1° **c**-miscut as controls. Templates were grown at 1100 °C to 2 μm thickness with a TMGa flow rate of 7 sccm (growth rate ≈ 5.3 Å/sec) in N_2 carrier gas.

Optical microscope images of the templates are shown in Fig. A.2. Eyelet pit defects were visible for all samples with an appreciable **a**-miscut. By contrast, neither the pure -1° **c**-miscut nor the pure +1 **c**-miscut exhibited eyelet pits, except at the wafer corners

(Fig. A.2.(g) and (i)), where the miscut is not well controlled due to edge rounding during the chemical mechanical polishing (CMP) process.

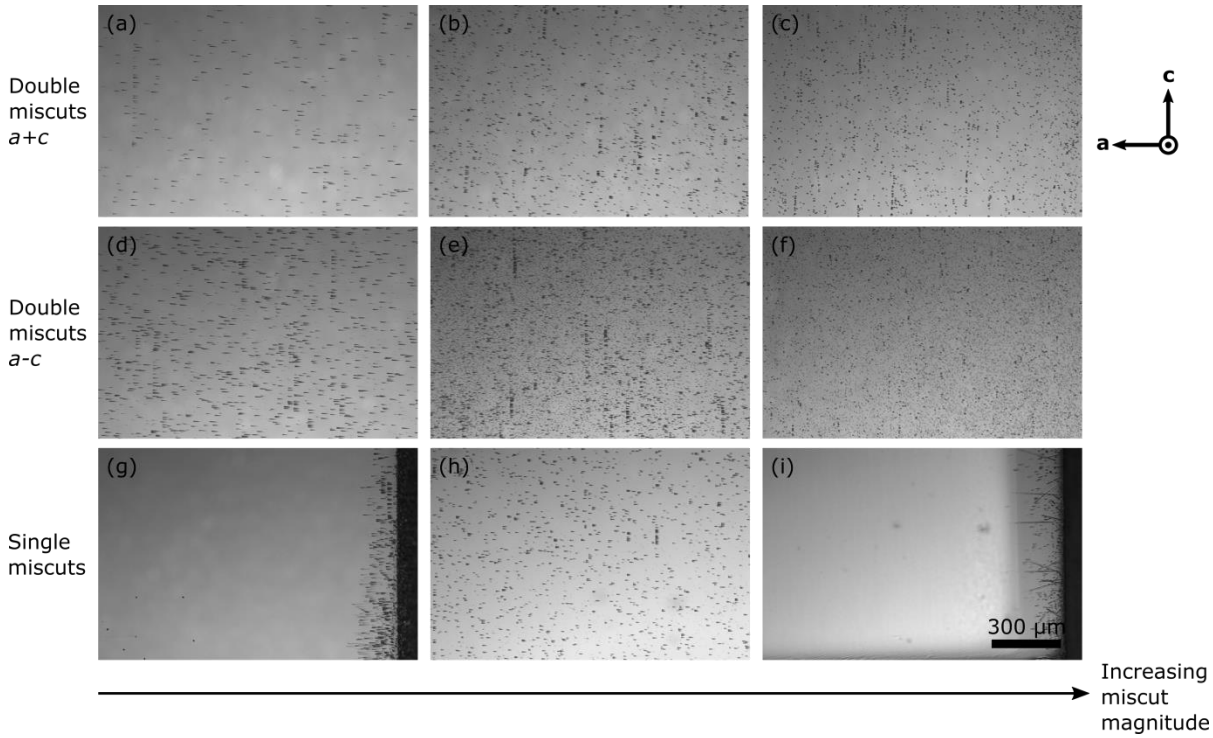

Figure A.2. Optical microscope images of co-loaded homoepitaxial growths at 1100 °C on double miscut and single miscut substrate surfaces. (a) 0.51 °**a**, 0.21 °**c** (b) 0.99 °**a**, 0.71 °**c** (c) 2.00 °**a**, 1.41 °**c** (d) 0.49 °**a**, -0.36 °**c** (e)1.01 °**a**, -0.84 °**c** (f) 1.94 °**a**, -1.50 °**c** (g) – 1 °**c** (h) 1 °**a** (i) 1 °**c**. Eyelet pits were observed on all samples with intentional **a**-miscut components, but not on pure **c**-miscut samples, (g) and (i).

Larger miscut angles produced higher densities of eyelets. Formations of eyelets tended to align along the crystallographic **c**-direction. The eyelet shape also changes with miscut magnitude, which is more clearly visible in AFM amplitude retrace images of the same samples in Fig. A.3.

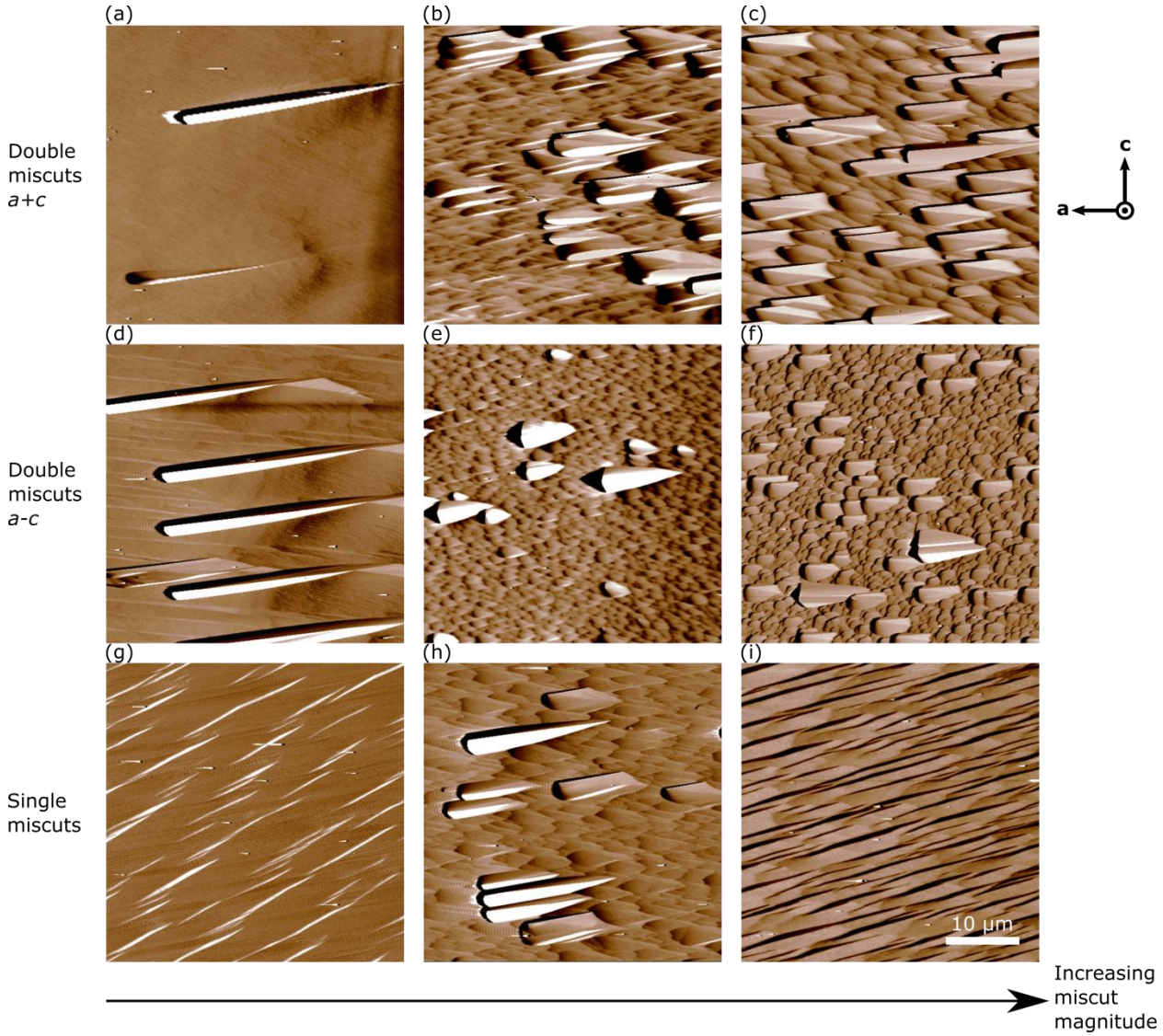

Figure A.3. Large area AFM amplitude retraces of the co-loaded homoepitaxial films (2 µm thickness). Root mean squared roughnesses were calculated from the scans (a) 12.7 nm, (b) 16.9 nm, (c) 23.2 nm, (d) 25.1 nm, (e) 25.5 nm, (f) 30.2 nm, (g) 2.87 nm, (h) 21.3 nm, (i) 2.54 nm.

Smaller angle miscuts produced longer eyelets with lower density and larger angle miscuts yielded shorter, more point-like eyelets with higher density. The eyelet pits orient in the same direction in every growth and exhibit crystallographic faceting. The shapes formed in Fig. A.3. (d) suggest a possible relationship to pyramid spiral growth. The rms roughness values extracted from the images in Fig. A.3. are approximately an order of magnitude larger in the pitted samples than in the reference samples with +1° or -1° pure **c**-miscut

(Fig. A.3. (g) and (i)). The pure **c**-miscut samples exhibited striated surface morphologies, which is consistent with previous analyses of homoepitaxial films grown in the same or similar conditions.[3,2]

Eyelet pits are as large as 20 μm across, and at least several hundred nanometers deep (considered a lower bound due to limitations of the AFM tip size). They are usually visible by the naked eye due to the matte appearance they give to the sample surface. When quantum wells (QWs) are grown on the templates, the pits become visible in fluorescence microscopy, and in cathodoluminescence (Fig. A.4.).

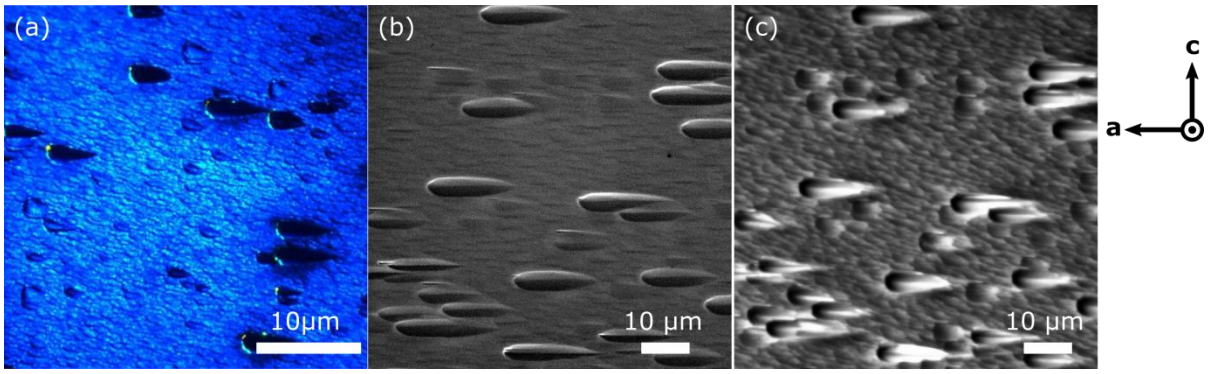

Figure A.4. Luminescence images of single quantum wells grown on double miscut (2.00 °**a**, 1.41 °**c**) substrates under (a) fluorescence (b) SEM (c) panchromatic CL.

Even in the presence of high eyelet densities and surface roughness, narrow linewidth and higher quick test power were achieved for the double miscuts. The high power may be partially attributed to an enhancement of the on-wafer light extraction. Poor laser diode characteristics were observed compared to co-processed standard -1° **c**-miscut samples (data not shown), which could be attributed to the pits which cause waveguide interruptions and loss that would not be present for a smooth film. For example, a deep pit filled with metal after p-contact deposition causes greater metal interaction with the waveguide and can lead to

large internal losses. Thus, several paths were pursued to eliminate or reduce the eyelet defects.

A.2. Surface Treatments Prior to Growth

The origin of the pits is unknown, but may be the result of residual surface contamination after CMP processing of the substrates at the manufacturing facility. Several pre-growth treatments were attempted to remove contaminants prior to MOCVD growth. Table A.2. lists and details the attempted treatments and the target contamination for each treatment. Most treatments produced no change in growth compared to untreated control samples, except for basic piranha treatment, which increased the number of eyelet defects compared to the control.

Cleaning Treatment	Details	Purpose
Buffered HF	1 min with agitation	To remove oxide CMP particles
48% HF	5 min with agitation	To remove oxide CMP particles
Heated Basic Piranha	1) 12 min in boiling NH_4OH and H_2O_2 2) 1 min dip in 1:1 HCl:H_2O	To remove organics
Heated Acidic Piranha	1) 20 min in boiling H_2SO_4 and H_2O_2 2) 1 min dip in 1:3 HCl: H_2O 3) 10 min in 1:1:5 HCl:H_2O_2:H_2O	To remove organics
Aqua Regia	20 min in heated (80 °C) 1:3 HNO_3:HCl	To remove metallics
"Clean H" from MCC	1) Proprietary cleaning procedure done at MCC 2) No additional clean at UCSB	To remove CMP-related surface contaminants
Digital Oxidation and Etching	1) 20 min oxidation in UV/Ozone 2) 1 min in buffered HF	To oxidize and then etch atomic silicon contaminants
ICP Etch Back	1) 20 min oxidation in UV/Ozone 2) 1 min dip in buffered HF 3) 1 min dry etch in ICP (220 nm/min etch rate)	To oxidize and etch back contaminants
Oxidation, Wet Etch and ICP Etch Back	1) 1 min dry etch in ICP (220 nm/min etch rate)	To etch back contaminants

Table A.2. Several surface preparations were tested to attempt to reduce or eliminate eyelet pits.

Surface treatments prior to growth were unsuccessful in reducing the size or the density of eyelet pit defects. Thus, growth studies were next pursued to identify conditions to suppress defect formation.

A.3. Controlling Eyelet Size and Density with Growth Conditions

Homoepitaxial growth was performed under a variety of growth conditions to investigate the mitigation of eyelet pits. First, growth temperature was examined. The samples were grown at a rate of 32.5 A/sec (7 sccm TMGa) for 39 min at a V/III ratio of 5658 (3.2 SLM NH_3) in N_2 carrier gas. The results for a range of temperature from 900-1200 °C are shown in Figs. A.5. and A.6.

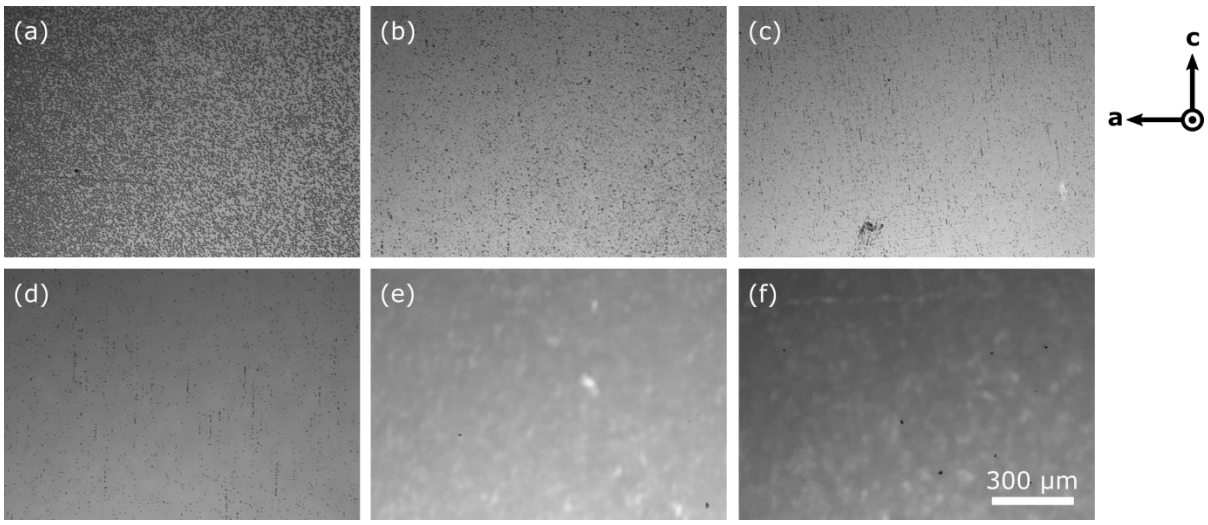

Figure A.5. Optical microscope images of the temperature dependence of pit formation in template growth for the double miscut (1.94 °**a**, -1.50 °**c**). The trend is representative for all double miscuts (data not shown). (a) 1200 °C (b) 1100 °C (c) 1050 °C (d) 1000 °C (e) 950 °C (f) 900 °C. Pits disappear between 950 °C and 1000 °C.

Growth temperature has a strong impact on eyelet density. The eyelet density decreases with decreasing temperature. The lowest growth temperatures of 900 °C and

950 °C exhibited no eyelets, although they began to exhibit some other "crater"-like defects. The trend here is shown for just one of the double miscut orientations, but the trend is the same for all of the orientations. Fig. A.6. shows AFM scans for the same samples to highlight the changing surface morphology and to quantify the rms roughness. This orientation had low temperature films with as little as 2.0 nm rms roughness and other orientations achieved even lower roughnesses in the low temperature, eyelet-free films.

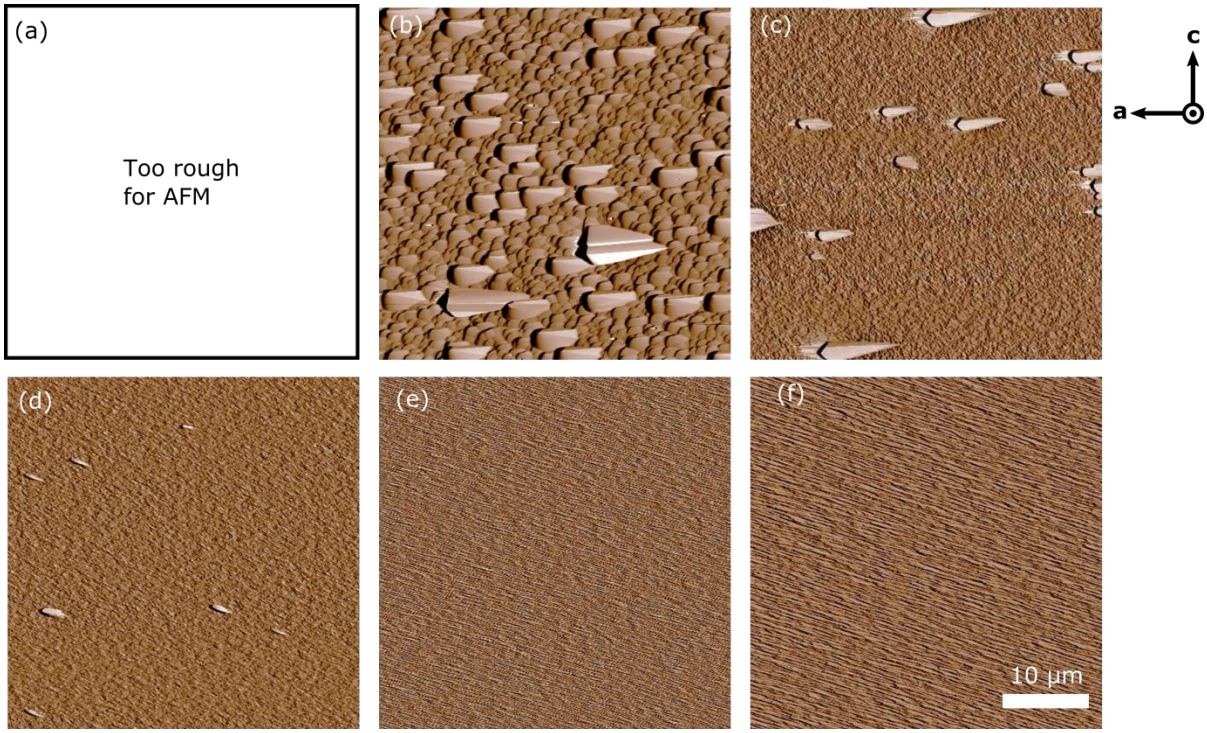

Figure A.6. AFM images of the temperature dependence of pit formation in template growth are shown here for the double miscut (1.94 °**a**, -1.50 °**c**), but the trend is representative for all double miscuts. (a) 1200 °C (b) 1100 °C (c) 1050 °C (d) 1000 °C (e) 950 °C (f) 900 °C. Pits disappear between 950 °C and 1000 °C. The rms roughnesses for these images are (b) 30.2 nm (c) 24.3 nm (d) 2.0 nm (e) 5.4 nm (f) 9.9 nm.

Next, the growth rate dependence was investigated by setting the growth temperature to a moderate 1100°C and varying the TMGa flow rate from 3.5 sccm to 15 sccm, corresponding to approximate growth rates of 2.7 Å/sec to 11.4 Å/sec. Optical microscope images of the film surfaces for this series are shown in Fig. A.7. Increasing growth rate

corresponded to decreasing eyelet density. The range of growth rates this series was not sufficient to see complete elimination of eyelets.

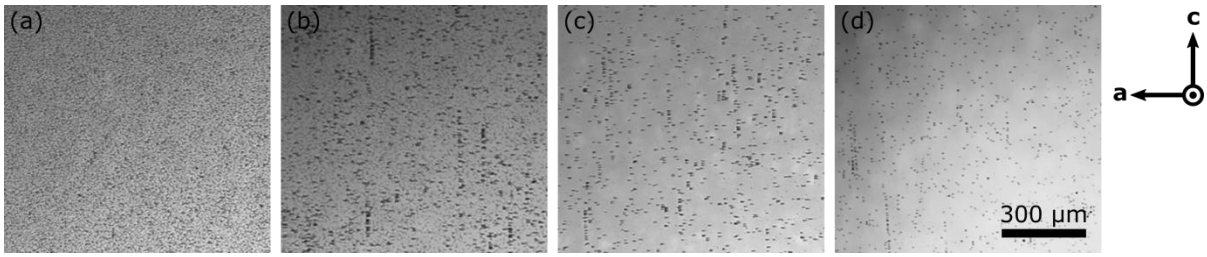

Figure A.7. Growth rate dependence of pit formation in template growth is shown for the double miscut (1.01 °**a**, -0.84 °**c**), but the trend is representative for all double miscuts. The growth rates were (a) TMGa 3.5 (2.7 Å/sec), (b) TMGa 7 (5.3 Å/sec), (c) TMGa 10 (7.6 Å/sec), (d) TMGa 15 (11.4 Å/sec). The growth time was set to 78 min, 39 min, 27.3 min and 18.2 min, respectively, to maintain the same final template thickness.

The temperature and growth rate results suggested that low diffusion conditions can suppress eyelet formation. Thus, a two-point V/III ratio comparison was done to determine if higher V/III ratio could also help to suppress eyelets. High ammonia overpressures reduce the adatom mobility on the sample surface during growth, as do low temperatures and fast growth rates. Fig. A.8. shows that the higher V/III ratio growth condition yields a slight reduction in eyelet density.

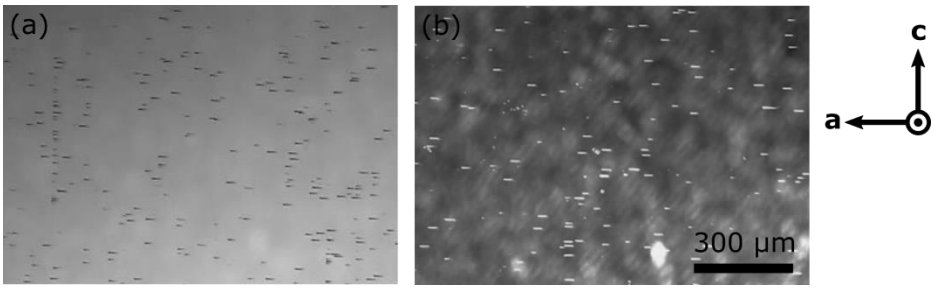

Figure A.8. Template growth for miscut (0.51 °**a**, 0.21 °**c**) grown with two different V/III ratios (a) NH_3 = 3.2 SLM and V/III = 5658, and (b) NH_3 = 4.2 SLM and V/III = 7426.

Low temperature growth was capable of completely eliminating the eyelets. However, in general, low temperature GaN growth is avoided because it is accompanied with

the incorporation of more carbon impurities (especially with TMGa precursor[4]) and poorer crystal quality, which can include deep level defects.[5] Previous work on two-step GaN quantum barriers[6] suggested that the benefits of high temperature growth with high adatom mobility could be recouped if a high temperature GaN layer is grown on top of the required low temperature layer. In the case of the template, this was attempted by growing two consecutive full template layers (~ 2 μm each) and comparing the resulting morphology.

The first low temperature GaN layer was grown at 1000 °C to suppress eyelet formation, and the second layer was grown at 1150 °C to establish a high quality crystal layer suitable for subsequent active region growth. The resulting film surfaces are shown in Fig. A.9., where it is evident that even after a thick low temperature buffer layer growth that is eyelet-free, the eyelets can re-emerge in the subsequent high temperature growth. This suggests that the crystal defects or impurities that cause the eyelets "float" with the film growth.

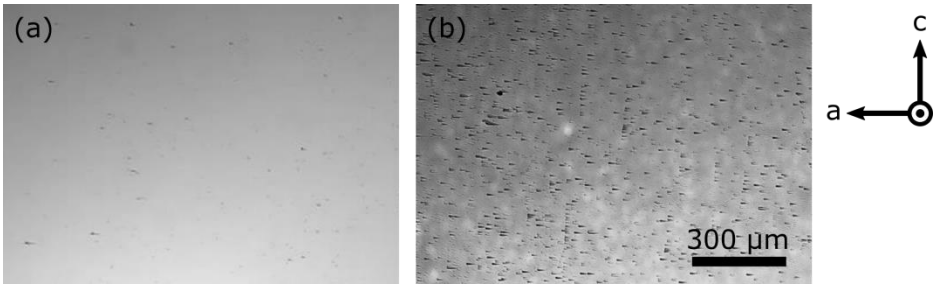

Figure A.9. Optical microscope images of (a) a template grown on 1°**a**-miscut at 1000°C for 39' (b) a two-step template grown on 1°**a**-miscut at 1000°C for 39' followed growth at 1150°C for another 39'. The growth is interrupted during the temperature ramp. Although the defects are not present during the low temperature growth, they re-emerge during the high temperature step.

In general, it appears that low diffusion conditions suppress the formation of eyelet defects in template growth. This includes low temperature, high growth rate, and high V/III ratio during template growth. Changing the temperature had the greatest effect, and was the

only method that has been successful in completely suppressing eyelet formation, however, this required template temperatures between 950 °C and 1000 °C (Fig. A.5. (e)-(f)). A two-step GaN layer designed to first suppress eyelets and then form a high crystal quality layer resulted in a recurrence of the suppressed eyelets.

A.4. LED Growth on Double Miscut Substrates

Reduced growth temperature was the only solution to eliminating the eyelet features, so LED structures were grown on templates with lower temperatures, and the resulting emission characteristics were examined. The LED structures had 2 μm-thick Si-doped template layers ranging from 950 °C to 1100 °C , a triple quantum well active region with 5 nm wells and 10 nm barriers, followed by an AlGaN electron blocking layer (EBL) and 300 nm of *p*-GaN. Quick test EL results were obtained by pressing indium dots onto the sample surface as the *p*-contacts and soldering an indium side-contact to the sample edge for the *n*-contact and applying a current density of 20 A/cm^2. Backside emission was collected with a silicon photodetector. The raw data was filtered to include only samples emitting 445 – 460 nm in the blue spectrum.

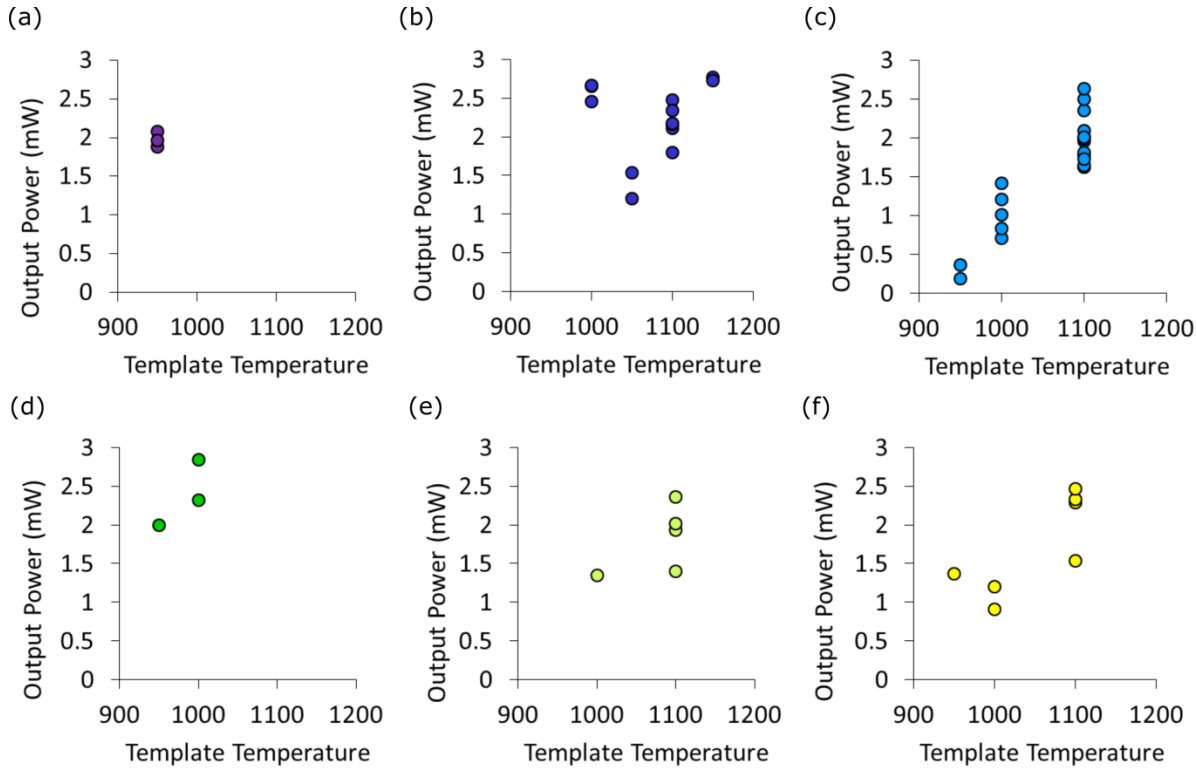

Figure A.10. Quick test power results at 20 A/cm2 for triple quantum well LEDs emitting 445 nm – 460 nm grown on double miscut substrates (a) 0.51 °**a**, 0.21 °**c** (b) 0.99 °**a**, 0.71 °**c** (c) 2.00 °**a**, 1.41 °**c** (d) 0.49 °**a**, -0.36 °**c** (e)1.01 °**a**, -0.84 °**c** (f) 1.94 °**a**, -1.50 °**c**.

Fig. A.10. shows the quick test power results for samples grown with various template temperatures and emitting in the wavelength range of 445 – 460 nm. It is somewhat difficult to identify trends in the data that are valid for all miscuts. The largest data set after filtering and clearest trend occurred for double miscut (2.00 °**a**, 1.41 °**c**). This miscut was also one of the samples that had most consistently produced narrow linewidths in both PL and EL. The trend shows a drop in output power with the reduction in template growth temperature.

The reduced template temperature affects the output power miscuts, sometimes dramatically reducing the power, as in the case of the preferred double miscut (2.00 °**a**, 1.41 °**c**). The only features of the template growth that should affect the active region performance are the morphology and the doping profile. Separately-grown low

temperature template films show that the surface has a low rms roughness (< 2 nm rms roughness in many cases). This led to the hypothesis that the silicon dopant incorporation may be miscut and temperature dependent, which would result in some miscuts with misplaced junctions and resulting poor optoelectronic performance.

Disilane was used as the silicon precursor for its temperature stability, but the large temperature change (200 °C) could possibly be enough to affect the doping profile. If the doping is also miscut dependent, then this could explain the variation between the samples. SIMS analyses were performed to understand doping incorporation on different miscuts and under different temperature growth.

The double miscut (2.00 °**a**, 1.41 °**c**) and the standard -1°**c**-miscut were co-loaded for MOCVD growth of Mg and Si SIMS stacks. The conditions for each layer are listed for both the Si SIMS stack (Table A.3 (top)) and the Mg SIMS stack (Table A.3. (bottom)). The first two layers of the Si SIMS stack are grown at 950 °C and 1150 °C, respectively, so that the temperature effect on doping can be assessed for the two co-loaded miscuts.

Si SIMS			
Layer	Temperature (°C)	TMGa (sccm)	$(SiH_4)_2$ (sccm)
I	950	7	1.9
II	1150	7	1.9
III	1150	14	1.9
IV	1150	7	4
V	1150	7	0.6
VI	1150	7	3.2
VII	1150	7	1.9

Mg SIMS				
Layer	Temperature (°C)	TMGa (sccm)	TEGa (sccm)	Cp_2Mg (sccm)
i	950	3.5	--	10
ii	950	3.5	--	50
iii	950	--	20	20
iv	950	3.5	--	20
v	950	3.5	--	5
vi	950	3.5	--	10

Table A.3. Description of SIMS growth conditions in the various layers in the Mg stack (top) and the Si stack (bottom).

The Si concentration data is shown in Fig. A.11 (a) for the co-loaded miscuts. The standard -1°**c**-miscut miscut sample shows sharper layer definition because of its smoother surface and consequently, more uniform SIMS crater. The doping levels measured on the co-loaded the standard -1°**c**-miscut miscut and double miscut (2.00 °**a**, 1.41 °**c**) samples were similar. Furthermore layers I and II, which were grown at 950 °C and 1150 °C, respectively, were at approximately equal. Thus Si dopant incorporation with disilane does not appear to have a strong temperature or miscut dependence.

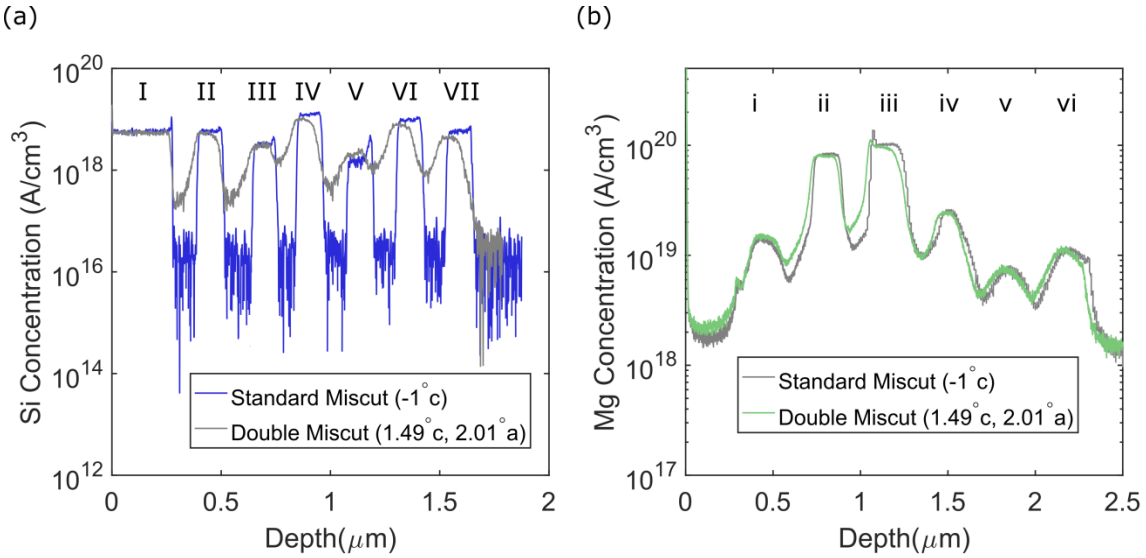

Figure A.11. SIMS analysis showing similar incorporation of (a) Si and (b) Mg in films on -1°**c**-miscut and double miscut (2.00 °**a**, 1.41 °**c**) substrates. The Si data includes seven different growth conditions denoted by capital Roman numerals: (I)-(VII). The Mg data includes six different growth conditions denoted by lowercase Roman numerals: (i)-(vi). The growth conditions are tabulated in Table A.3. SIMS scans courtesy of Seoul Semiconductor.

Similar results are shown for Mg concentrations in Fig. A.11 (b). All these layers were grown at 950 °C. The co-loaded standard -1°**c**-miscut miscut and double miscut (2.00 °**a**, 1.41 °**c**) samples had similar Mg concentrations in all of the layers, indicating that Mg incorporation is also miscut independent.

Neither surface roughness nor intentional dopant incorporation explains the reduced output power for samples. Perhaps impurity incorporation such as carbon or oxygen could be affecting the subsequently grown quantum wells. Further work is required to determine the root cause of the reduced output power with low temperature templates.

Preliminary results suggest that adding a thin (100 nm), high temperature (1150 °C) TEG interlayer between the low temperature template and the active region can recover some of the lost output power for double miscut (2.00 °**a**, 1.41 °**c**) while preventing full

development of eyelet defects. Some eyelets return in the interlayer growth, but are not as large or deep as when a full high temperature template layer is grown (Fig. A.12 (b)).

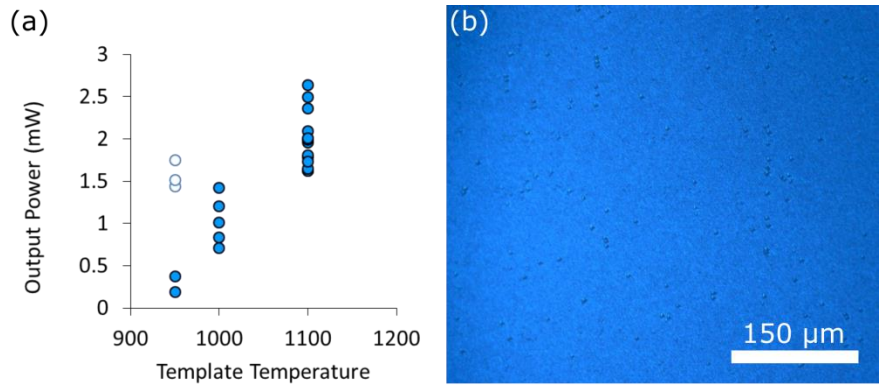

Figure. A.12. Output power recovery for double miscut (2.00 °**a**, 1.41 °**c**) LEDs grown on low temperature templates with the inclusion of a high temperature (1150 °C) 100 nm interlayer before QW growth (a) Open circles indicate LEDs grown with the high temperature interlayer. Solid circles are LEDs grown without the interlayer. (b) Fluorescence image of the double miscut (2.00 °**a**, 1.41 °**c**) LED with 950 °C and 1150 °C interlayer.

The results in Ch. 2 use the high temperature interlayer design as a compromise to reduce eyelet defect densities while maximizing output power for the preferred double miscut orientation, (2.00 °**a**, 1.41 °**c**). This miscut exhibited narrower linewidth, higher indium uptake and higher output power compared with standard miscut, which is attributed to its more uniform atomic step-terrace structure. The results are achieved in spite of some residual eyelet defects.

Appendix A References

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Appendix B. Process Traveler for Ultra-High Light Extraction LED Fabrication

Step	Equipment	Details	Comments
Surface Clean and Reactivation			
Remove Indium Aqua Regia	Acid Bench	1:3 HNO_3:HCl hotplate at 225 °C, 5-10' until soln fades yellow, repeat 2x	Boil HCl, then add HNO_3, then add sample
Tergitol Scrub	Solvent bench	Scrub in tergitol with swabs to get rid of any residual scum	
Clean	Solvent Bench	3' Ace, 3' Iso, 1' DI N2 dry	sonicate on high
Reactivate	MOCVD lab furnace	Reactivate 15' at 600 °C	
ITO Deposition			
HF Dip	HF Bench	1' in BHF silicon monitors and LEDs	
ITO Deposition	E-Beam #2 (RT) (2.5 hrs)	Thickness - 0.24 kÅ, 0.5 Å/s, O2 flow ~30 sccm 6×10^{-5}Torr Room temperature	include Si monitors TF=106
ITO Anneal	RTA (30 min)	600°C, 10min, N_2/O_2, 6/1.5sccm (transparency) 600°C, 3min, N_2, 5sccm (conductivity)	Check RTA Calibration First Check RTA Calibration First
	Ellipsometry	Check annealed SiO2 for ITO thickness	
SiO_2 Sacrificial Layer Blanket Deposition			
SiO_2 Dep	Sputter #3 (1.5 hr)	Load silicon calibration piece Login: Earl Check and run recipe COH_SiO2 Sidewall Dep for 400"	
	Ellipsometry	Measure SiO2 on Si monitor thickness and index	
	Sputter #3	Load sample(s) with a few silicon monitors Calculate dep time for 20 nm SiO2 Update and run recipe: COH_SiO2 Sidewall Dep	
	Ellipsometry	Measure SiO_2 on Si monitor thickness and index	
Mesa Litho			
Mesa Litho	PR Bench	**HMDS** 3,10,30 krpm,krpm/s,s (let HMDS sit 20 s before spinning) **AZnLOF2070** 3.5,10,30 krpm,krpm/s,s EBR, razor blade method Soft Bake @ **110 °C for 90"**	(no clean if directly out of Ebeam2/RTA) Negative Tone, 5.8 um
	Left Contact Aligner	Expose **26"** no filter, "MESA" dark field mask	left aligner, chrome touches sample, check that power is ~ 7.8 mW/cm^2
	PR Bench	Post Bake @ **110 °C for 60"**	
	Develop Bench	Develop in **AZ300 MIF for 40-45"**, DI Rinse and N2 Dry	

	Optical Microscope	Check PR mask	
UV Ozone Descum	PR-100	600"	
HF Dip	HF Bench	Check SiO2 etch rate with monitor (~6")	
		Etch samples 3x etch rate of monitor to create SiO2 PR underlayer	
ITO and Mesa Etch			
ITO dry etch	RIE#2 (2 hrs)	O2 clean, 20 sccm, 125 mT, 500V, 30' M/H/A coat, 4/20/10 sccm, 75 mT, 500V, 20'	No sample in the chamber (blue plasma) M: Methane, H: Hydrogen, A: Argon (pink plasma)
		MHA dry etch, 4/20/10 sccm, 75 mT, 350V, 35% over etch For every 5' MHA etch, O2 descum, 20 sccm, 125 mTorr, 170 V, 50"	Sample in chamber, (~17.2 nm/min) (< 5')
		O2 descum, 20 sccm, 125 mT, 300V, 2.5'	Sample in chamber
GaN mesa dry etch	RIE#5 (2 hrs)	Load bare RIE wafer for chamber prep: yonkee01	O2 clean, BCl3 coat, SiCl4 prep
		Load samples on RIE wafer (no oil) for etch: yonkee02	SiCl4 etch, Etch rate = 30 nm/min (very repeatable)
Inspect	MOCVD Fluorescence Scope	Check that only mesas light up, which means that the active region is etched away outside mesas	
Strip PR	Solvent Bench	**1165** preheated 80°C, 10-15' in heated bath, sonicate on lowest settings 2' Ace, 2' Iso, 2' DI	can do higher sonication if needed for this step sonicate on lowest settings
BHF Dip	HF Bench	1' in BHF silicon monitors and LEDs	to remove GaN redep; both heated substrate and RT+anneal ebeam ITO are very resistant to BHF
Check Etch Depth	Dektak	Drop stylus off of ITO/Mesa	
Quick Test		light up in the MOCVD lab by probing ITO and n-GaN	
Dielectic Mirror Current Blocking Layer Litho			
Clean	Solvent Bench	2' Ace, 2' Iso, 2' DI	sonicate on lowest settings
Dielectric Mirror Litho	PR Bench	**PMGI-SF8** (~400 nm) 5,10,30 krpm,krpm/s,s Soft Bake **170 °C for 2'** **AZnLOF2035** 3,10,30 krpm,krpm/s,s EBR, razor blade method Soft Bake @ **110 °C for 90"**	Left hotplate in left spin bench Negative Tone
	Left Contact Aligner	Expose **11.5"** no filter, "SIO2" bright field mask	left aligner, chrome touches sample, check that power is around 7.8 mW/cm^2
	PR Bench	Post Bake @ **110 °C for 60"**	

		Hard Bake @ **90 °C for 10'**	
	Develop Bench	Develop in **AZ300 MIF for 60-70''**, DI rinse, N2 dry	
	Optical Microscope	Check PR mask	
UV Ozone Descum	PR-100	600"	
Dielectic Mirror Current Blocking Layer Deposition			
Dielectric Mirror Dep	IBD	Login: Nakamura Psw: nitrides	
		Calibrate Ta2O5 recipe 12_BY_Ta2O5_1 for 30 min	~300 nm, Si monitor
		Calibrate Al2O3 recipe 12_BY_Al2O3_1 for 1 hr	~200 nm, Si monitor
		Calibrate SiO2 recipe 12_BY_SiO2_1 for 1 hr	~ 300 nm, Si monitor
	Ellipsometry	Measure samples with Cauchy on Si model and fit for range 360-1200 nm Calculate dep times for 7_Layer Mirror:	
	IBD (12 hrs)	(1) SiO2_1: 195.51 nm	at 45 degree tilt (multiply flat layer calculated time by (1/0.643) to account for slower dep rate w/ tilt)
		(2) Ta2O5_1: 121.37 nm	7_layer mirror >99% reflective at 450 nm
		(3) SiO2_2: 355.70 nm (4) Ta2O5_2: 59.03 nm (5) SiO2_3: 89.83 nm (6) Ta2O5_3: 53.45 nm (7) Al2O3: 59.51 nm	
		Load sample(s) with silicon monitor and DSP sapphire monitor	
	Ellipsometry	Measure SiO2 on Si monitor thickness and index	
Strip PR	Solvent Bench	Soak sample in 1165 pre-heated to 80 °C for 15' Sonicate 1165 in bath at lowest settings swish for 30" Iso, 30" DI, N2 dry	
Inspect	Optical Microscope	check that SiO2 liftoff complete	
Contacts Metal Deposition			
Clean	Solvent Bench	2' Ace, 2' Iso, 2' DI	sonicate on lowest settings
Contacts Litho	PR Bench	**HMDS**, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning) **AZnLOF2035** 3,10,30 krpm,krpm/s,s EBR, razor blade method Soft Bake @ **110 °C for 90"**	Negative Tone
	Contact Aligner	Expose **11.5"** no filter, "CONTACTS" bright field mask	left aligner
	PR Bench	Post Bake @ **110 °C for 60"**	
	Develop Bench	Develop in AZ300 MIF for **50"**, DI rinse, N2 dry	

	Optical Microscope	Check PR mask	
UV Ozone Descum	PR-100	600"	
HCl Dip	Acid Bench	HCl:DI 1:3, 30sec; DI rinse, N2 dry	
n-Electrode Metal Deposition	E-Beam #4 (4 hrs)	Al/Ni/Au, 1250/1250/8000Å	
	Solvent Bench	1165 preheated 80°C, 1hr soak in heated bath, liftoff w/ pipette and razor blade	
Inspect	Optical Microscope	Check final device	sonicate on lowest settings if needed
On-Wafer Testing			
Setup	Quick Test Lab	Change out existing probe tips for personal Au-coated W probe tips Place clean DSP sapphire over detector opening Place sample on sapphire over detector opening	
Testing		Position the probe tips over the center of the detector opening Test all die on the wafer under the same sweep conditions and in the same location w.r.t. the detector	Measure all samples in series in one testing session to avoid changes in the setup, e.g. detector height
		Move from die to die by moving the sample, rather than the probe tips to ensure the same placement of each die over the detector opening	
Die Singulation			
Sample mounting prep	Clean Room Heated Solvent Hood	Set hotplate to 130 °C	
		Apply a few drops of xtal bond soln to sapphire submount (1/4 wafer sapphire for 1 cm2 LED wafer) in an Al tin	Xtal bond solution (20 g xtal bond in 100 mL acetone)
		Apply a few drops of xtal bond soln to sample in an Al tin	
		Place tins on hotplate and evaporate out acetone ~ 5 min	
		Cut a coverslip to size slightly smaller than sample (e.g. 0.9 cm^2 for 1 cm^2 LED wafer)	
		Place coverslip on sample and reheat, ensuring no bubbles form underneath	
Bond sample to dicing submount	Wafer Bonder	Wipe down top and bottom of chamber with ISO	bonder next to the UV/Ozone
		Assemble sample(s) in wafer bonder (samples on top of sapphire submount)	If one sample, put in center of the chamber If multiple samples, put at uniform radius
		SETUP TEMPS: 110 °C bonding temp, endpts 70 °C, 15 °C offset	offset is difference between thermocouple

		SETUP VACUUM: vacuum threshold 2.5E1 mBar, abort if above 3.2E1 mBar SETUP PROCESS: process type heat and outgas, soak 5', bond 10'	and heater total time is about 25' with ramp up and down
Blade Prep	Dicing Saw	Blade: 2.187-8C-54RU Flange: 52 mm Make 15-20 cuts on a 4" silicon wafer (0.77 µm) prior to dress the blade (cut depth 0.6 mm)	30RU is also fine sharpens the blade
Dice Sample		Conditions: 0.515 mm cut depth, 18krpm spindle speed (important!*)	*too fast spindle speed melts the blade resin and gets black gunk on your LEDs cuts just a little into sapphire submount so you can see the cut
		If sapphire substrate is >700 µm, do a 2-pass cut to prevent blade breakage	for 2-pass cut, start cutting on Angle#3 (software bug)
Die Cleaning and Packaging Lab			
Clean Die	Packaging lab dissecting scope	Place diced sample in acetone for several minutes to dissolve xtal bond Clean each die ACE/ISO/DI in the packaging lab Dry thoroughly in a glass petri dish on a hot plate at 105 °C Store LEDs in gel packs with #4 tack	 get from physics store
	Clean room solvent bench	If necessary, individual LEDs can be sonicated on lowest settings in clean room baths	avoid doing this if possible, tedious and precarious, although effective if you do have a dirt problem gasonics also OK on singulated die (low temp settings)
Packaging			
Make white headers	Packaging Lab	Protect header leads by adding silicone drop to each and curing, 10' at 150 °C Shake Avian B bottle Pour a small amount of Avian B integrating sphere coating premix into a separate container Dip headers (single dip) into the coating and place upright to dry overnight	
Package LEDs		Mount LEDs to white headers with silicone, cure 10' at 140 °C	too long or too hot in oven yellows the coating
		Peel away silicone from leads and wire bond Test unencapsulated	
		Use inverted cone mold and OE6550 silicone (n=1.54) to package, 15' at 140 °C	pump out bubbles from silicone
		Remove carefully from mold	

Appendix C. Process Traveler for CAIBE Facet Laser Diode Fabrication

Step	Equipment	#	Process Step	Notes
Surface Clean and Reactivation				
Remove Indium	Acid Bench	1	1:3 HNO_3:HCl (aqua regia) hotplate at 225 °C, 5-10' until soln fades yellow, repeat 2x	Boil HCl, then add HNO_3, then add sample
Tergitol Scrub	Solvent bench	2	Scrub samples in tergitol with swabs to get rid of any residual scum	
Scribe	Bench	3	Scribe topside to mark the c- side of the sample	
Clean	Solvent bench	4	3' Ace, 3' Iso, 2' DI (sonicate on high) N2 dry	
Reactivate	MOCVD lab furnace	5	Reactivate 15' at 600 °C (or use RTA 600C 15 min N2/O2)	
Ridge Formation and SiO2 Deposition				
Ridges Litho	Solvent bench	6	3' Ace, 3' Iso, 2' DI (sonicate on high) N2 dry	
	PR Bench	7	Dehydration bake on hotplate at ≥110 °C for ≥2', cool 1'	
		8	Spin **LOL 2000**, 2 krpm, 10 krpm/s, 30s (~250 nm thick)	mount small samples on blue tape, can spin multiple samples simultaneously
		9	Clean backside with EBR 100	if needed
		10	Bake on center of LH hotplate at **210 °C for 5'**, cool 1'	Actual center T ~194 °C
		11	Spin **955CM-1.8**, 3 krpm, 10 krpm/s, 30 s (~1.8 μm thick)	
		12	Clean backside with EBR 100	if needed
		13	Soft bake on hotplate **95 °C for 90 s**	
	Stepper #2 (30+')	14	Load mask #1A/B/C/D/E - Ridges	1D has all 5 um widths and various lengths
		15	Load sample onto 2" 500 μm chuck with 130 μm shim with *c*+ pointing up	
		16	"EDIT RIDGESV4B" Check: die size and column number	
		17	"EXEC RIDGESV4B", PASS: "RIDGES"	no pass shift
		18	Expose 0.75 s, focus = -1	
	PR Bench	19	Post-exposure bake on hotplate at **110 °C for 90 s**	
	Develop Bench	20	Develop in **726MIF for 65 s**, DI Rinse, N2 dry	63 s if using the 2.5 um ridges
	Microscope	21	Inspect (0.3-0.5 um undercut on LOL 2000) develop more if necessary	

	UV Ozone	22	1200 s (~6 Å/min)	
Ridges Etch	RIE #5 (2+ hr)	23	Load bare carrier wafer	
		24	Run DAN_01 O2 clean: 20.5 sccm, 10', 5 mTorr, 150 W RF; BCl3/Cl2 pretreat: 20.5 sccm BCl3, 5.2 sccm Cl2, 3', 10 mTorr, 15 W RF; Cl2 etch conditions: 10.2 sccm, 2', 5mTorr, 200 W RF	no He cooling
		25	Repeat DAN_01	
		26	Load sample onto carrier wafer (no mounting oil)	
		27	Run DAN_03, 04 or 05 BCl3 pretreat: 10 sccm, 10', 2', 10 mTorr, 100 W RF; Cl2 Etch: 10 sccm, 5', 5 mTorr, 200 W RF	Dan_03 is 5'
		28	Soak sample in DI water, N2 dry	
	Microscope	29	Inspect	
	Laser Microscope	30	Image RIDGES pad	
	Sputter #3 (3+ hr, start at same time as RIE)	31	Load silicon calibration piece	
		32	Login: Earl Check and run recipe: COH_Ratetestdep for 2100" (35')	
SiO2 Dep & Liftoff	Ellipsometer	33	Measure SiO2 on Si calibration thickness and index	should be ~ 125 nm (dark blue colored), n=1.47
	Sputter #3	34	Load sample(s) with silicon monitor	
		35	Calculate dep time for 225 nm SiO2. Update and run recipe: COH_SiO2 Sidewall Dep	
	Ellipsometer	36	Measure SiO2 on Si monitor thickness and index	should be ~ 225 nm (gold colored), n=1.47
	Solvent bench	37	Soak sample in 1165 pre-heated to 80 °C for 15'	place sample face-down in beaker
		38	Move sample to 2nd 1165 pre-heated to 80 °C	
		39	Sonicate in bath at frequency: 8, intensity: 8, power: low, time~20-30 s	
		40	swish for 30" Iso, 30" DI, N2 dry	
		41	Inspect, repeat steps 37–40 if necessary	
P-Contact Formation				
	Solvent clean	42	2' in each ACE/ISO/DI swishing or sonicating on lowest settings	
	PR Bench	43	Dehydration bake on hotplate ≥110 °C ≥2', cool 1'	
		44	Spin **HMDS**, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)	
		45	Spin **OCG825**, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)	

Contact Pads Litho		46	Clean backside of sample with EBR 100	if needed
		47	Bake on hotplate at **95 °C for 2'**	
	MJB-3 aligner	48	Load sample onto one of the black chucks	left aligner only
		49	Flood expose 1 s	
	PR Bench	50	Let sample outgas on benchtop for 5' (VERY IMPORTANT)	otherwise, bubbles form in the resist after spinning 2nd layer
		51	Bake on hotplate at **95 °C for 2'**, cool 1'	
		52	Spin **955CM-1.8**, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)	
		53	Clean backside with EBR 100	if needed
		54	Softbake on hotplate at **95 °C for 90 s**	
	Stepper #2 (30+')	55	Load mask: EF V5.gds - Layer 6 Thin Pmetal BackN	for 2-litho p-contact process
		56	Load sample onto 2" 500 µm chuck with 130 µm shim with *c*+ pointing up	
		57	"EDIT RIDGESV4B" Check: die size, column number, right alignment die position	
		58	"EXEC RIDGESV4B", PASS: "PCONTS"	no pass shift
		59	Expose 0.75 s, focus= -1	
	Develop bench	60	Develop in **726MIF for 60s** (~2 µm undercut on OCG825), DI Rinse, N2 dry	
	Microscope	61	Inspect, develop more if necessary	
	UV Ozone	62	1200 s (~6 Å/min)	
p-Contact Dep	Acid Bench	63	Mix 1:1 HCl:DI, etch 30 s, DI rinse, N2 dry	removes native oxide, do immediately before contact deposition
	E-Beam #3 (2+ hr)	64	Deposit 300/800 Å Pd/Au narrow metal p-contacts	for adhesion, start dep at 5e-7 torr (use a Ti burn if needed). Pd dep at 0.5 Å/s, ramp to 1 Å/s at 100 Å over 30"
	Solvent bench	65	Place upside-down in 1165 heated to 80 °C for 10+', then liftoff using pipette agitation	for adhesion, do not leave overnight in hot 1165
		66	Move sample to fresh beaker of 1165 and agitate until visibly clean pattern (no Au strands)	
		67	swish for 30" Iso, 30" DI, N2 dry	
	Microscope	68	Inspect, repeat steps 65–67 if necessary	
P-Pad Formation				
	Solvent clean	69	2' in each ACE/ISO/DI swishing or sonicating on lowest settings	
	PR Bench	70	Dehydration bake on hotplate ≥110 °C ≥2', cool 1'	

		71	Spin **HMDS**, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)	
		72	Spin **OCG825**, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)	
		73	Clean backside of sample with EBR 100	
		74	Bake on hotplate at **95 °C for 2'**	
	MJB-3 aligner	75	Load sample onto one of the black chucks	left aligner only
		76	Flood expose 1 s	
		77	Let sample outgas for 5' (VERY IMPORTANT)	
	PR Bench	78	Bake on hotplate at **95 °C for 2'** let cool 1'	
		79	Spin **955CM-1.8**, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)	
		80	Clean backside with EBR 100	if needed
		81	Softbake on hotplate at **95 °C for 90 s**	
Contact Pads Litho	Stepper #2 (30+')	82	Load mask #2 - "EF V5.gds-Layer 7: PContPads"	
		83	Load sample onto 2" 500 µm chuck with 130 µm shim with *c*+ pointing up	
		84	"EDIT RIDGESV4B" Check: die size, column number, right alignment die position	
		85	"EXEC RIDGESV4B", PASS: "PCONTS"	no pass shift
		86	Expose 0.75 s, focus= -1	
	Develop bench	87	Develop in **726MIF for 60s** (~2 µm undercut on OCG825), DI Rinse, N2 dry	
	Microscope	88	Inspect, develop more if necessary	
	UV Ozone	89	1200 s (~6 Å/min)	
p-Pad Dep	E-Beam #3 (2+ hr)	90	Deposit 300/10,000 Å Ti/Au	
	Solvent bench	91	Place upside-down in 1165 heated to 80 °C for 10+', then liftoff using pipette agitation	do not leave overnight in hot 1165
		92	Move sample to fresh beaker of 1165 and agitate until visibly clean pattern (no Au strands)	
		93	swish for 30" Iso, 30" DI, N2 dry	
	Microscope	94	Inspect, repeat steps 91-93 if necessary	
C+ Facet Formation				
	Solvent bench	95	2' in each ACE/ISO/DI swishing	
	PR Bench	96	Dehydration bake on hotplate at ≥110 °C for ≥2', cool 1'	
		97	Spin **HMDS**, 3.5 krpm, 10 krpm/s, 30 s	
		98	Spin **SPR220-7.0**, 3.5 krpm, 10 krpm/s, 45 s (~6 µm thick)	
		99	Clean backside with EBR 100	if needed
		100	Soft bake on hotplate **115 °C for 120 s**	

C+ Facets Litho	Stepper #2 (30+')	101	Load CAIBE mask	
		102	Load sample onto 2" 500 µm chuck with 130 µm shim with ***c+* pointing up**	orientation very important!
		103	"EDIT RIDGESV4B" Check: die size, column number, right alignment die position	
		104	Under CAIBE pass, Y Pass Shift = +0.016 (first etch, shifts pattern DOWN and exposes the c+)	Adjust pass shift if p-pad alignment was off by more than 400 nm in Y. Must align to metal in Y
		105	"EXEC RIDGESV4B", Pass: "CAIBE"	
		106	Expose 1.35 s, focus= -1	
	PR Bench	107	Let sample **outgas for 35'** IMPORTANT	preheat the hotplate at 50 °C
	PR Bench	108	Post-exposure bake on hotplate at **50 °C for 60 s**, then immediately move to **115 °C for 90 s**	
	Develop Bench	109	Develop in **726MIF for 105 s**, DI rinse, N2 dry	
	Microscope	110	Inspect lithography. Check that facets mask aligned in y does not expose any metal. Check that it is the C+ side that is exposed for etching first	
	UV Ozone	111	1200 s (~6 Å/min)	
SiO2 Wet Etch1	Acid Bench	112	Etch piece of Si Monitor #1 in BHF (~200 nm/min)	
		113	Inspect monitor for hydrophobicity every 10-15s, record total etch time (should take 50 s – 1')	
		114	Etch sample in BHF for double the monitor etch time, DI rinse, N2 dry	
C+ Facets Etch	Oxford Ion Mill (2+ hr)	115	Mount samples on chuck with Cu tape such that facets to be etched (c+ side) face LHS	when chuck is mounted into system, it rotates 180°, so the facets will then face the beam
		116	Run: "Speck-Std_Ar_Cl2_norotate_7x" 35', 7x5' etch steps with 6x5' cool steps ; Gases: Ar 5 sccm to Neutralizer; Ar 10 sccm to Beam; Cl2 20 sccm to Chamber; Beam etch source 200 mA Neutralizer, 200 W RF, 150 mA, 250 Vb, 500 Va; Platen drive "Posn", Platen "Cool" 10 C chiller, Chamber "heat" 40 C	etch rate 50-60 nm/min cools substrate and heats chamber walls
	Solvent bench	117	Strip mask in 1165 heated to 80 °C for 10+', agitate with pipette	place sample upside-down in beaker
		118	Move sample to fresh beaker of 1165	
		119	Soak sample in 1165 heated to 80 °C for 2', agitate with pipette	

		120	swish for 30" Iso, 30" DI, N2 dry	
	Microscope	121	Inspect that the surface is clean and that the correct side has been etched	
	Laser Microscope	122	Confirm the etch depth and profile	
C- Facet Formation				
C- Facets Litho	Solvent bench	123	Swish or sonicate on lowest settings 1' Ace, 1' Iso, 1' DI, N2 dry	
	PR Bench	124	Dehydration bake on hotplate at ≥110 °C for ≥2', cool 1'	
		125	Spin **HMDS**, 3.5 krpm, 10 krpm/s, 30 s	
		126	Spin **SPR220-7.0**, 3.5 krpm, 10 krpm/s, 45 s (~6 µm thick)	
		127	Clean backside with EBR 100	if needed
		128	Soft bake on hotplate **115 °C for 120 s**	
	Stepper #2 (30+')	129	Load CAIBE mask	
		130	Load sample onto 2" 500 µm chuck with 130 µm shim with ***c*+ pointing up**	orientation very important!
		131	"EDIT RIDGESV4B" Check: die size, column number, right alignment die position	
		132	Under CAIBE pass, Y Pass Shift = -0.016 (2nd etch, shifts pattern DOWN and exposes the c-)	Adjust pass shift if p-pad alignment was off by more than 400 nm in Y. Must align to metal in Y
		133	"EXEC RIDGESV4B", Pass: "CAIBE"	
		134	Expose 1.35 s, focus= -1	
	PR Bench	135	Let sample **outgas for 35'** IMPORTANT	preheat the hotplate at 50 °C
	PR Bench	136	Post-exposure bake at **50 °C for 60 s**, then immediately move to **115 °C for 90 s**	
	Develop Bench	137	Develop in **726MIF for 105 s**, DI rinse, N2 dry	
	Microscope	138	Inspect lithography. Check that facets mask aligned in y does not expose any metal. Check that it is the c- side that is exposed for etching	
	UV Ozone	139	1200 s (~6 Å/min)	
SiO2 Wet Etch2	Acid Bench	140	Etch piece of Si Monitor #2 in BHF (~200 nm/min)	
		141	Inspect monitor for hydrophobicity every 10-15s, record total etch time (should take 50 s – 1')	
		142	Etch sample in BHF for double the monitor etch time, DI rinse, N2 dry	

C- Facets Etch	Oxford Ion Mill (2+ hr)	143	Mount samples on chuck with Cu tape such that facets to be etched (c- side) face LHS	(when chuck is mounted into system, it rotates 180°, so the facets will then face the beam)
		144	Run: "Speck-Std_Ar_Cl2_norotate_7x"	etch rate 50-60 nm/min
	Solvent bench	145	Strip mask in 1165 heated to 80 °C for 10+', agitate with pipette	place sample upside-down in beaker
		146	Move sample to fresh beaker of 1165	
		147	Soak sample in 1165 heated to 80 °C for 2', agitate with pipette	
		148	swish for 30" Iso, 30" DI, N2 dry	
	Microscope	149	Inspect that the surface is clean and that the correct side has been etched	
	Laser Microscope	150	Confirm the etch depth and profile	
N-Contact Formation				
N-contact Dep & Liftoff	PR Bench	151	Mount sample upside down on Si wafer with a drop of AZ 4110	
		152	Bake on hotplate at 105 °C for >5'	
	E-beam #3 (1+ hr)	153	Deposit 500/1000/3000 Å Al/Ni/Au Wait 5' after Ni dep before rotating turret to Au pocket	Al rate < 3 A/s. Ni necessary for heat sink soldering
	Solvent bench	154	Soak sample in 1165 heated to 80 °C until sample detaches from Si wafer	place upside-down in beaker. Do not try to slide or pry samples off
		155	2' Iso, 2' DI, N2 dry (swish or sonicate on lowest settings)	
	Microscope	156	Inspect, repeat 1165 if necessary	
Preliminary Testing	Test lab	157	Test devices prior to facet coating (optional)	
HR Back Facet Coating				
HR Back Facet Coating	Solvent bench	158	3' Ace, 2' Iso, 1' DI, N2 dry (sonicate on lowest settings)	
	Gasonics	159	Recipe 2, multiple runs if desired	
	E-beam #1	160	Blanket deposit 500 Å of Ge with tilt & rotation on, with Si Monitor	
	PR Bench	161	Dehydration bake on hotplate 110 °C 2', let cool 1'	
		162	Spin **HMDS**, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)	
		163	Spin **OCG825**, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)	
		164	Clean backside of sample with EBR 100	

Litho				
		165	Bake on hotplate at **95 °C for 2'**, let cool 1'	
	MJB-3 aligner	166	Load sample onto one of the black chucks	left aligner only
		167	Flood expose 1 s	
	PR Bench	168	Let sample **outgas for 5'** (VERY IMPORTANT)	
		169	Bake on hotplate at **95 °C for 2'**, let cool 1'	
		170	Spin **955CM-1.8**, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)	
		171	Clean backside of sample with EBR 100	
		172	Softbake on hotplate at **95 °C for 90 s**	
	Stepper #2	173	Load mask # 5 - Facet Coatings to coat both facets at once, or mask # 5b HR facet coatings (to coat the back HR mirror only)	
		174	Load sample onto 2" 500 µm chuck with 130 µm shim with *c*+ pointing up	
		175	Run "EX RIDGESV4B"	
		176	Pass: DBRS (pass shift = 0)	
		177	Expose 2.20 s, focus=0	
	Develop bench	178	Develop in **726MIF for 60 s** (~2 µm undercut on OCG825), DI rinse, N2 dry	
	Microscope	179	Inspect, develop more if necessary	
	PE II	180	30 s, 300 mT, 100 W	or UV/ozone 1200"
Ge wet etch	Acid Bench	181	Etch piece of Si Monitor in Hydrogen Peroxide to get etch rate	
		182	Etch sample for double the monitor etch time (~60 s), DI rinse, N2 dry	
IBD cals	Veeco IBD	183	Nakamura 12, pwd: "nitrides"	
		184	Calibrate SiO2 dep rate on Si for 1200" (tilt and rotate throughout), measure n and t in ellipsometry	~0.8 A/s, n=1.47
		185	Calibrate Ta2O5 dep rate on Si for 1200", measure n and t in ellipsometry	~1.2 A/s, n=2.27
		186	Calibrate SiO2-centered fabry-perot (λ/4n Ta2O5, λ/2n SiO2, λ/4n Ta2O5)	"12_LD_SiO2_FP_3PD_45deg"
	Filmetrics	187	Measure R vs. λ, "notch" is at λ/2n, adjust the SiO2 time for the refined dep rate	Repeat if off by >5nm
	Veeco IBD	188	Calibrate Ta2O5-centered fabry-perot (λ/4n SiO2, λ/2n Ta2O5, λ/4n SiO2)	"12_LD_Ta2O5_FP_3PD_45deg"
	Filmetrics	189	Measure R vs. λ and adjust Ta2O5 time	Repeat if off by >5nm
		190	Load samples	

Back Facet Coating	Veeco IBD	191	Calculate new dep times to account for field vs facet coverage ratio for 45 ° platen angle: SiO2 time = 1.55*(calibrated SiO2 time); Ta2O5 time = 2.30*(calibrated Ta2O5 time); grid cleans 15' in the beginning and 5' in between steps NOTE: Facet Coatings have had problems 2015-2016, consider process in BETA	HR coatings: start periods with λ/4n SiO2 then λ/4n Ta2O5
		192	Set number of periods (normally 5–8), run recipe	2 um facet etch depth allows for ~5 period DBR
	Solvent bench	193	Liftoff in 1165 heated to 80 °C for 10+', agitate with pipette	
		194	Move sample to fresh beaker of 1165	
		195	Soak sample in 1165 heated to 80 °C for 2', agitate with pipette	
		196	2' Iso, 2' DI, N2 dry	
	Microscope	197	Inspect, repeat 1165 if necessary	
HR or AR Front Facet Coating				
	Solvent bench	198	1' Ace, 1' Iso, 1' DI, N2 dry	
	PR Bench	199	Dehydration bake on hotplate ≥110 °C 2', let cool 1'	
		200	Spin **HMDS**, 3 krpm, 10 krpm/s, 30 s (let HMDS sit for 20 s before spinning)	
		201	Spin **OCG825**, 3 krpm, 10 krpm/s, 30 s (~1.5 µm thick)	
		202	Clean backside of sample with EBR 100	
		203	Bake on hotplate at **95 °C for 2'**	
	MJB-3 aligner	204	Load sample onto one of the black chucks	left aligner only
		205	Flood expose 1 s	
	PR Bench	206	Let sample **outgas for 5'** (VERY IMPORTANT)	
		207	Bake on hotplate at **95 °C for 2'**, let cool 1'	
		208	Spin **955CM-1.8**, 3 krpm, 10 krpm/s, 30 s (~1.8 µm thick)	
		209	Clean backside of sample with EBR 100	
		210	Softbake on hotplate at **95 °C for 90 s**	
Output Facet Coating Litho	Stepper #2	211	Load mask # 5c - Front facet coatings (if used #5b above)	
		212	Load sample onto 2" 500 µm chuck with 130 µm shim with *c*+ pointing up	
		213	Run "EX RIDGESV4B"	
		214	Pass: DBRs	
		215	Expose 2.20 s, focus = 0	

	Develop bench	216	Develop in **726MIF for 60 s** (~2 μm undercut on OCG825), DI rinse, N2 dry	
	Microscope	217	Inspect, develop more if necessary	
	PEII	218	30 s, 300 mT, 100 W	
	Acid Bench	219	Etch piece of Si Monitor in Hydrogen Peroxide to get etch rate	
		220	Etch sample for double the monitor etch time (~60 s), DI rinse, N2 dry	
Front Facet Coating	Veeco IBD	221	Re-calibrate IBD if it has been more than 2 days since the HR facet coating	
		222	Load samples	
		223	Calculate new dep times: SiO2 time = (1.59*calibrated SiO2 time), Ta2O5 time = 2.50*(calibrated Ta2O5 time)	
		224	Set number of periods (normally 2 – 3 for HR/HR coating or single SiO2 for AR coating), run recipe	AR coatings: SiO2 single layer
	Solvent bench	225	Liftoff in 1165 heated to 80 °C for 10+', agitate with pipette	
		226	Move sample to fresh beaker of 1165	
		227	Soak sample in 1165 heated to 80 °C for 2', agitate with pipette	
		228	2' Iso, 2' DI, N2 dry	
	Microscope	229	Inspect, repeat 1165 if necessary	
Cu Heat Sink Mounting				
Heat Sink Mounting	Packaging Lab Dissecting Microscope	230	Materials: heater and probe mount, wide Cu stub mount, screw for stub, Pb Sn Ag solder foils, superior flux #3- (glutamic acid, HCl), optical table screws, razor blade, Q-tips	for cw testing. Parts in drawer to right of microscope
		231	file Cu stub to size of substrate with 400 grit sandpaper	
		232	screw down heater and probe setup to scope stage	
		233	screw stub to heater	
		234	place sized solder foil on stub and press foot pedal to start heater and melt foil, use some flux to help	takes ~90 s to heat up
		235	scrape solder and reflow until it stops migrating	remove foot from pedal because takes a while to cool
		236	let cool, add some more flux, then add sample	
		237	use probe mount to push down on the LD sample in the center of pattern to hold it in place	
		238	heat until reflow and wets, let cool	

Appendix D. LED Process Development

D.1. Mesa Etch Redeposition and Grassing

After the GaN mesa etch, two problems were often observed: (1) poorly defined edges and (2) grassing. Optical microscope images in Fig. D.1. (a) and (b) show that the surface is clean and well-defined after the ITO etch, but not after the GaN mesa etch. The issues arose after etching by either ICP and RIE. The two problems had two different solutions.

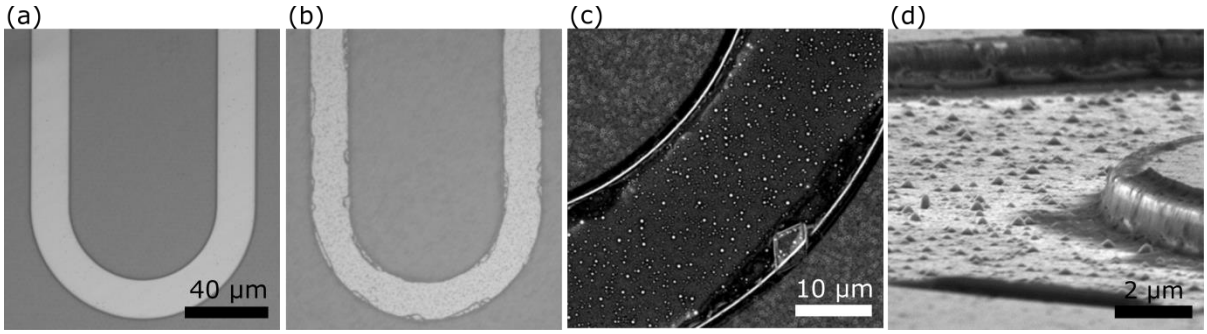

Figure D.1. Process development on the GaN etch step with optical microscope images (a) after ITO etch but prior to GaN mesa etch (b) after GaN mesa etch, there are poorly defined edges and grassing visible. SEM images show in more detail (c) grass and redeposition that appears to show crystal faceting and (d) an angled view of the mesa etch to show the grass and the sidewall cleanliness.

The grassing Fig. D.1 (c) was resolved by increasing the time of overetch during the ITO etch step. Notably, increasing the oxygen clean time was not helpful. Thus, it was concluded that the grassing was caused by incomplete methane-hydrogen-argon (MHA) etching of the ITO, which led to micromasking and grassing during the GaN etch step. A 35% ITO overetch (compared to a previously prescribed 20% overetch) was sufficient to eliminate the issue.

The poorly defined edges were attributed to redeposition of material on the mesa sidewalls during etching. The problem was resolved by performing a one minute dip in buffered HF (BHF) following the PR mask removal. No cleans designed for organics were successful (gasonics, solvents, stripper), so it was concluded that the redeposition was inorganic material. The redeposition was not attributed to ITO because it occurred even on samples with no ITO. It is tentatively attributed to a polycrystalline GaN redeposition, which appears to be soluble in BHF.

D.2. Post-Mesa Etch Photoresist Removal

Photoresists can sometimes become rigid and difficult to remove after dry-etching steps, especially negative photoresists. This project requires pristine LED mesa surfaces to maximize the LEE potential. Complete PR removal was ensured by incorporating a 30 nm sacrificial SiOx layer prior to the mesa lithography (See App. B for details). After patterning, the SiO_2 was cleared from the etch target area with a brief BHF dip. The etch was performed and the resist was removed as usual. The SiOx layer ensures complete liftoff of the resist and a pristine surface for subsequent processing and testing.

D.3. Acceptable Cleaning Procedures

Sonication in room temperature baths at the lowest frequency and intensity settings is safe and effective throughout the entire fabrication process, including after die singulation. Gasonics remote oxygen plasma ashing is safe when performed at low temperatures (recipes one – three) and is sometimes effective in removing organic contaminants. High temperature ashes are avoided to prevent unintentional metal anneals.