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Heterogeneous Integrated Photonic Transceiver on Silicon

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

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March 2017

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This thesis is dedicated to my parents.

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ABSTRACT

Heterogeneous Integrated Photonic Transceiver on Silicon

by

Chong Zhang

The demand for high-speed and low-cost short-distance data links, eventually for chip-level optical communication, has led to large efforts to develop high density photonics integrated circuits (PICs) to decrease the power consumption and unit price. Particularly, silicon based photonic integration promise future high-speed and cost-effective optical interconnects to enable exascale performance computers and datacenters. High-level integration of all photonics components on chip, including high speed modulators and photodetectors, and especially lasers, is required for scalable and energy efficient system topology designs. This is enabled by silicon-based heterogeneous integration approach, which transfers different material systems to the silicon substrate with a complementary metal–oxide–semiconductor (CMOS) compatible process.

In this thesis, our work focuses on the development of silicon photonic integrated circuit in the applications of high speed chip level optical interconnects. A full library of functional devices is demonstrated on silicon, including low threshold distributed feedback (DFB) lasers as a low power laser source; high extinction ratio and high speed

electroabsorption modulators (EAM) and ultra-linear Mach-Zehnder interferometer (MZI) modulators for signal modulation in the data transmitter; high speed photodetectors for the data receiver; and low loss silicon components, such as arrayed waveguide grating (AWG) routers and broadband MZI based switches. The design and characterization of those devices are discussed in this thesis.

A highly integrated photonic circuit can be achieved with co-design and co-process of all types of functional photonic devices. Selective die bonding method is performed to integrate multiple III-V dies with different band-gap onto a single photonic die. A reconfigurable network-on-chip circuit was proposed and demonstrated, with state-of-the-art high-speed silicon transceiver chip. With over 400 active and passive components heterogeneously integrated on silicon, photonic circuit with multiple-wavelength-division multiplexing (WDM) transceiver nodes achieved a total capacity up to 8×8×40 Gbps. This high capacity and dense integrated heterogenous circuit shows its potential as a solution for future ultra-high speed inter- and intra-chip interconnects.

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Chapter 1

Introduction

Efficiently processing, transmitting, and storing massive amounts of data is the most important technical topic and one of the major driving forces for the development of a modern information society. As an enabling technology, optical communication has been playing critical roles since those significant inventions in the last century such as lasers, optical fiber, Erbium doped fiber amplifier (EDFA), etc. The traditional electrical cables have gradually given the way to optical fibers or optical cables, from long haul communications, to short interconnects e.g. in the datacenter or supercomputer. With the fundamental advantages of large bandwidth and low power loss, optical interconnects are believed to be able to replace the electrical wires in meter, centimeter or even millimeter scales. Eventually, chip level interconnects for future high performance computers require small volume and large capacity optical link to overcome the limit copper wires and I/O pins.

The challenges to the photonic interconnects are the required power and the ability to scale. The energy consumption of 10-100 pJ/bit, which are common for optical and electrical interconnects today, must shrink to 100-500 fJ/bit within a few years for large bandwidth exascale systems. For long haul systems, the power required for

photonic transmission has been dramatically reduced over the past 40 years, suggesting a reduction in energy/bit/distance by a factor of 10,000 has occurred in the past twenty years [1]. This progress can be further extended into data centers and supercomputers by continuing to reduce the energy per bit by another factor of 10-100 and by reducing the size of the transmitters by a factor of 10-100 while simultaneously increasing their capacity from 10 Gbps to 200 Gbps or more. Hence, the strong motivation is to transition the discrete components and modules to integrated transponders and monolithic photonics – following the massive success of the industry of very-large-scale integration (VLSI) of electronic integrated circuits (EIC). The rising demand for high speed communication in short distance, such as in data centers and super computers, is driving this need.

In order to proceed on this route, the integration platform is experiencing significant transitions from the group III-V semiconductor materials, such as indium phosphide (InP) or gallium arsenide (GaAs), to silicon that is commonly used in the EIC industry. III-V materials have been intensely studied for decades and favored for photonic integration – due to their direct bandgap and high carrier mobility nature, and also their well-developed epitaxial growth of defect-free compound materials with flexible bandgap design catering to the applications of fiber optics [2-4]. However, the photonic integration on III-V suffers from the high cost of the substrate as well as the lack of large wafers – which is one of the major driving force of EIC industry to continuously decrease the unit price. The lack of the low-loss waveguide is also a bottleneck for large scale integration when the power budget is limited by the high light transmission loss within the circuit.

Since the end of last century, silicon based photonic integration has been of great interest, because of the availability of cheap material and the mature CMOS fabrication techniques inherited from electrical integration industry. Large silicon wafers, up to 450 mm in diameter, are available in the market, while the III-V substrates are limited to 100 mm or 150 mm with about 100 times larger price per unit area compared with silicon [5]. As another advantage, low-doped silicon and its dielectric compound has low material absorption at the optical communication wavelength window, enabling low loss waveguide (sub-dB/cm) and ultra-low loss waveguide (sub-dB/m) [6-8]. A series of other important components required for optical links have been demonstrated on silicon, including modulators, photodetector, and a full library of other passive units [9-12].

However, silicon is not an appropriate material for light emission due to its indirect band-gap nature. The poor radiative recombination efficiency prohibits an on-chip laser source or optical amplifier with silicon. This is a major obstacle for an on-chip laser on silicon, causing great difficulties in high density photonic integration designs. With other approaches, such as using the stimulated Raman scattering effect in silicon, the first continuous wave (CW) silicon laser was demonstrated in 2005 by Rong et al. [13, 14], but an electrical driven silicon laser was still missing, and the low efficiency makes it impractical as the light source in optical transceivers. Given this fundamental material limit of silicon, intense efforts have been carried out to make on-chip laser source by taking the advantages of other material systems to extend the capacity of silicon photonics. Three major approaches were mainly adopted, as summarized below.

(1) Hybrid assembling

Here, by means of hybrid assembly, a III-V chip with laser source and silicon chip with waveguide and other units are assembled into a single photonic circuit [15]. The device performance on each side can be optimized individually by designing and fabricating them separately. The light can be coupled laterally in free space when two chips are assembled with facets in parallel [16-18], or vertically with grating couplers or surface emitting laser and photodetectors [19-21]. The use of stacking of laser circuits and routing circuits with an optical interposer is of great interest to 3-D integration with electrical circuit with through silicon via (TSV) [19, 20].

However, this hybrid method requires high precision process on coupling and assembling. Most importantly, the fabrication and package of two photonic chips will boost up the total cost of the integrated circuit, which is not affordable for the application of short distance optical links.

(2) Heteroepitaxy

To epitaxially growing direct-bandgap materials on large size silicon substrates is believed to be the key to achieve high performance and low cost photonic devices on silicon [22-25]. However, the fact is that the lattice constant mismatch and thermal expansion coefficient mismatch in the heterogeneous system causes materials degradation in the grown layers – high density threading dislocations in the quantum wells (QWs) behave as trap centers and cause nonradiative recombination.

Ge and Ge/Si alloys grown on Si with Molecular Beam Epitaxy (MBE) has been well studied for its good compatibility with silicon substrate. High speed Ge photodetectors on silicon have been developed for integrated optical receivers [26-28]. By engineering

the doping in the Ge layer to enhance direct gap transition, an electrical pumped Ge laser CW operating at room temperature has been achieved in 2012 [29, 30], although the threshold current densities are 1000 times higher than demonstrated in this work [31], and further performance improvement is required for its practical application.

Unlike Ge, growth of III-V materials is more challenging. The grown material quality is sensitive to growth conditions such as temperature, pressure, V/III ratio and substrate treatment prior to growth. Many techniques have been proposed for heteroepitaxy of III-V on silicon, among which the epitaxial lateral overgrowth (ELO) method with metalorganic vapor phase epitaxy (MOCVD) has shown its potential to grow high quality III-V material on Si [32-34]. By trapping the dislocation generated from the growth interface with high aspect-ratio dielectric pattern, the overgrown III-V material coalesces and forms high quality III-V layer for device fabrication [35, 36]. Electrically pumped InP and InGaAs distributed feedback laser grown on Si has been achieved with ELO method [37, 38].

Recent research on growth of quantum dots (QDs) on silicon with MBE method have shown encouraging progress. Benefitting from the fact that with two orders of magnitude of higher dot density than dislocation density, QDs layers, compared to QWs, are more tolerant to anti-phase domain and threading dislocations penetrating into the III-V layers from the heterogeneous interface [39-41]. QDs lasers grown on silicon have shown low threshold current density and high temperature operation [40], low noise [42], and long working lifetime [43].

Over the longer term, heteroepitaxy will take the place of homoepitaxial growth on the expensive III-V substrate and provide gain material on large wafers. But in terms of

photonic integration, the quality of the III-V materials grown on Si is still deficient in device performance. In addition, the growth on silicon normally requires a thick spacer [38] or buffer layer [40], which makes it difficult to couple the light between the laser and silicon waveguide. The device structure needs to be carefully designed for the light coupling, such as the butt-joint regrowth method.

(3) Heterogeneous integration by materials bonding

Since the heterogeneous integration platform, also well known as the hybrid silicon or evanescent silicon platform, was firstly proposed in 2006 [44], it has drawn great attention due to its ability to combine the mature III-V material growth with rapidly growing silicon photonic technology. With a low-temperature bonding technique, various material systems, such as InP, GaAs, $LiNbO_3$, Yttrium iron garnet, etc., can be transferred to the silicon on insulator (SOI) substrate and integrated with pre-patterned silicon waveguides and other components on silicon layer [45-49].

Similarly, Skorpius Inc. developed a heterogeneous transmitter structure, by opening an etched window on SOI substrate by etching through the device and BOX layer, and then bonding III-V materials with QWs layers aligned with the silicon waveguide [50]. Amorphous silicon is deposited in the gap for light coupling between III-V and silicon waveguide. High speed transmitters have been demonstrated on this platform [51]. With the metal bonding of III-V layers directly on silicon substrate, the major heat source at the laser source has a low thermal barrier to the heat sink. However, 3-D like inset structure complicates the process of active devices after bonding and limits the chip design. The lossy α-Si bridging waveguide limits the efficiency of the laser source or the coupling efficiency.

In contrast, the heterogeneous integration platform discussed in this thesis, doesn't require precise alignment in the blank materials transfer step. In the heterogeneous section, as shown in *Figure 1-1*, the optical mode is confined both in silicon waveguide and III-V layers. The waveguide width and III-V mesa width are extra tuning knobs in the device design in performance optimization. The top down fabrication starts after the wafer bonding with no extra assembling required. This process is compatible with CMOS fabrication. This enabling technique brings great flexibilities on large scale photonic integration with complex functionality.

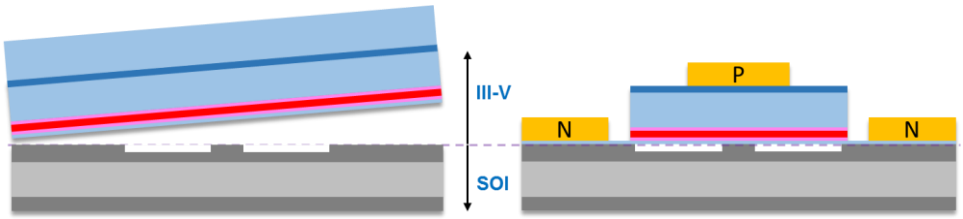

Figure 1-1. Heterogeneous integration on silicon

Additionally, multiple bandgap materials can be integrated on one chip with either quantum well intermixing [52] or multiple die bonding method [31]. Therefore, the laser can now be integrated along with a modulator or other III-V active devices on silicon with CMOS driver and control circuits.

This thesis demonstrates these devices and demonstrates the integration of these devices into the highest capacity and most complex PIC demonstrated anywhere. This thesis is organized as follows: in Chapter 2, the heterogeneous integration method is introduced, as well as the efforts that have been carried out on high temperature regrowth on the bonded III-V layer on Si; Chapter 3 demonstrates short cavity DFB lasers on silicon with low threshold current, and discusses the thermal management of heterogeneous microring lasers on silicon; Chapter 4 introduced two types of

integrated modulators on silicon: high speed electroabsorption modulator and linearized Mach-Zehnder modulator; in Chapter 5, a fully integrated photonic network-on-chip circuit is proposed, addressing the applications of heterogeneous integration in chip level interconnects; Chapter 6 summarizes this thesis and bring up outlooks for further development.

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Chapter 2

Heterogeneous III-V/Si integration

The bonding technique is the key step in the process used for the heterogeneous integration platform. With a CMOS-compatible low-temperature molecular bonding process, direct bandgap III-V layers can be transferred to pre-patterned SOI substrate with high yield, providing the gain section required for an on-chip laser and amplifier [1-2]. The bonding technique used in this work and the high temperature test on the bonded film are introduced in this chapter.

2.1 Plasma-assistant bonding process

Wafer bonding approach is widely used to joint homogeneous or heterogeneous materials into a defect-free system regardless of their crystalline structure and lattice constant [1-8]. Depending on the applications, varied wafer bonding techniques have been developed in terms of the medium at bonding interface or the surface treatment prior bonding. Adhesive bonding method is mostly used, which uses an adhesive substance (dielectrics, metal, polymer, etc.) to joint two solid materials together. To compare, metal bonding improves the electrical and thermal conductivity at the bonding interface, but the optical waveguides have to be kept away for low optical

absorption loss [8]; polymer bonding has been widely used in the III-V/Si integration due its simple surface planarization and tolerance on the material choice, but its defiance include the poor thermal conductivity of the bonding wet layer [7]; dielectric bonding has precise control on the thickness of deposited or native grown dielectric spacer layer with a smooth surface which is of help for high bonding yield [4, 5].

In this work, a plasma-assistant dielectric bonding method is used [1-5]. The hydrophilic bonding process uses either a native grown or deposited layer of dielectric material at the bonding interface. The oxygen plasma treatment on the dielectric layer generates dangling bonds, which improves the bonding strength with the relative low annealing temperature.

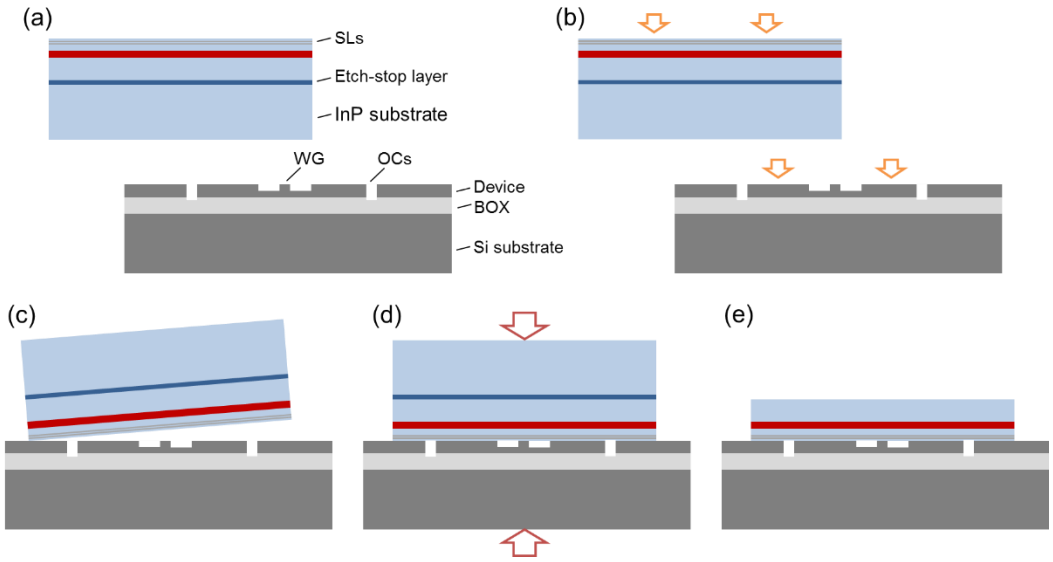

Figure 2-1. Procedure of plasma assisted wafer bonding. (a) wafer preparation with outgassing channel etch; (b) O2 plasma treatment; (c) Physical bonding; (d) Anneal at 300 °C with high pressure; (e) Remove InP substrate.

The bonding process with plasma-assistant dielectric layer is illustrated in *Figure 2-1*. The SOI wafer is acid cleaned and then patterned with passive components and outgassing channels. The III-V sample is also brush cleaned in solvent. Both clean

samples are located in a vacuum chamber for oxygen plasma treatment. A thin oxide compound layer is formed on both III-V and silicon by the O_2 plasma activation step. Then the III-V sample is physically bonded to the patterned SOI die with or without precise alignment. Afterwards the bonded sample is applied with high pressure in a graphite fixture and then annealed at 300 °C for 45 min. The InP substrate is mechanical thinned and then etched down to the InGaAs etch-stop layer by etchant with hydrochloric acid.

Gas byproducts are a major issue in the bonding process when polymerization reactions taking place. The main reactions during the molecular wafer bonding process are shown below, indicating that water vapor and hydrogen gas are the main gas byproducts generated [2]:

$$\mathrm{Si-OH + OH-M \longrightarrow Si-O-M + H_2O\uparrow} \quad (2\text{-}1)$$

$$\mathrm{Si + H_2O \longrightarrow SiO_2 + H_2\uparrow} \quad (2\text{-}2)$$

where M represents In or P in this case for InP bonding. The reaction is temperature sensitive, and gas generation rate increases drastically with elevated temperature after the physical bonding typically at room temperature. Dense outgassing channels, by etching through the device layer into the buried oxide (BOX) layer, improve the bonding yield by effectively trapping the gas byproducts at the bonding interface [2].

Another challenge in bonding process is the residue strain in bonded film caused by thermal expansion mismatch between III-V and silicon. Assuming an equilibrium state after the post-bonding anneal at 300 °C, and no strain relaxation through layer transformation, the strain change in the bonded InP film stack can be estimated by the material thermal expansion coefficients, as shown in *Figure 2-2*. The critical thickness

of InP on this hetero-system was calculated with such mismatch[9], showing that the critical thickness decreases fast with increasing temperature, but this modal possibly under-estimates the critical thickness [10] with the energy equilibrium assumption. Although the practical situation of the bonding system with oxide intermediate layer is more complex, it is intrinsically critical to keep bonded film thin when the heterogeneous system tolerates large temperature variation. Therefore, all high temperature process was performed after substrate removal step after wafer bonding, with only certain thickness normally ~2 μm left on silicon for a laser structure. For those materials with larger thermal expansion coefficient mismatch with silicon, such as GaAs, a lower post-bonding anneal is required to maintain high bonding yield.

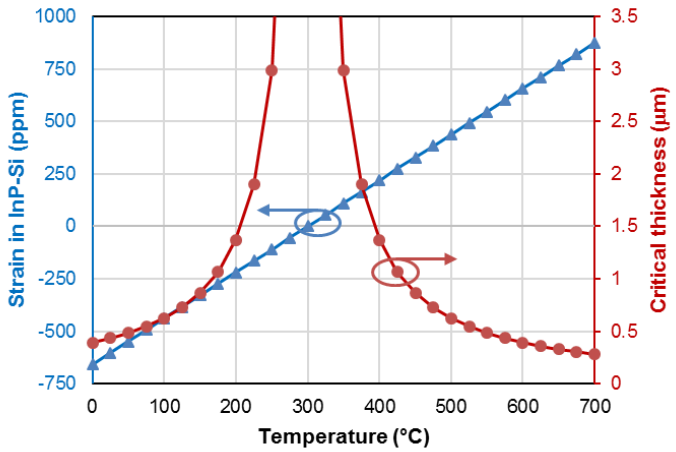

Figure 2-2. Strain in bonded InP film with changing temperature (positive sign means compressive strain; negative sign is tensile strain); and the critical thickness calculated with assumption of thin InP film on silicon substrate.

This bonding approach is flexible on the photonic circuit design. Selective die bonding on the required area is to save the expensive III-V substrate, and to individually design and optimize the III-V epi structure for each type of devices. As shown in *Figure 2-3*(a), both the laser and modulator epis are bonded on each die on a

four-inch SOI wafers for optical transmitters. *Figure 2-3* are the photos of bonded InP, GaAs and $LiNbO_3$ samples on SOI substrate with similar process, showing the capacity of such method in integrating different material systems to silicon photonic platform.

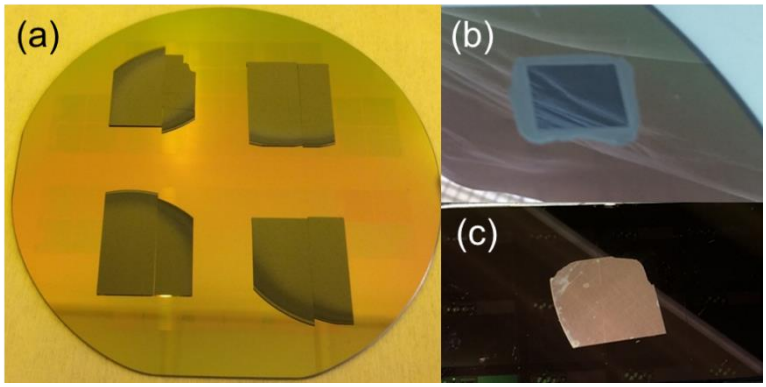

Figure 2-3. Bonded die on SOI substrates of (1) InP with QWs designed for laser and modulator, respectively. The sample was annealed at 300 °C for 2 hours. (2) GaAs with QDs for lasers at 1310 nm. The GaAs side has 25 nm deposited SiO2 layer before the bonding. The sample was annealed at 250 °C for 1 hour. (c) Z-cut $LiNbO_3$ bulk sample with 150 °C anneal over 10 hours.

2.2 Anneal test after wafer bonding

The bonding process discussed here is well compatible with most well developed III-V process techniques (e.g. InP or GaAs based), however, except the epitaxial regrowth which is a widely used technique in multi-functional III-V PICs [11, 12]. Particularly, selective area regrowth (SAG) is commonly adopted to provide multiple band-gaps materials on single chip for multiple purposes: e.g. optical mode confinement, components with different colors, etc. [13, 14] and butt-joint regrowth for flexible multi-section active-passive designs [15]. It is of practical significance to transfer the regrowth technique to the heterogeneous integration platform to improve design flexibility, increase integration level and improve overall chip performance.

Improved carrier confinement and laser injection efficiency should result from this regrowth capability specific for integrated laser case [16, 17].

Epitaxial regrowth on the heterogeneous integration platform, however, is generally considered impossible either before or after wafer bonding. If regrowth is performed on the III-V chip prior to bonding, accurate alignment is required for localized epitaxial structure. The surface topography after deposition also prohibits the molecular wafer bonding unless well-controlled chemical mechanical polishing (CMP) is used. In term of III-V regrowth after wafer bonding, as previously discussed, the elevated epitaxial temperature becomes the main problem. In MOCVD growth a high ambient temperature is necessary to reach the mass transportation regime of reactants to achieve high quality materials [18]. For InP and related compounds, this temperature is typically above 550 °C depending on the precursors that are used. But such a relatively high temperature could damage the III-V-to-silicon bond in the hetero-structure due to the mismatch of coefficients of thermal expansion, and the outgassing of byproducts in the wafer bonding polymerization reaction, both leading to bubble formation and delamination at the bonding interface [4].

The molecular bonding technique was modified to survive in the high growing temperature, as the outgassing channel design to facilitate gas byproduct diffusion away from bonding interface was found to play a critical role to avoid film delamination and material degradation. As demonstrated in previous work in the low temperature bonding process, outgassing channels improve the bonding efficiency (process time and wafers scale) by effectively trap the generated gas byproducts at the bonding interface [4]. But bubble formation caused by the trapped gas in VOCs is

observed at elevated temperature. To deal with such issues, in-plane outgassing channels (IPOCs) are found to be more efficient – the gas can tunnel out through the long trenches across the whole bonded epi. As shown in *Figure 2-4*, the IPOCs can be etched through the III-V stack to the InGaAs contact layer (*Figure 2-4* (b)), or on the SOI side until to the buried oxide layer (*Figure 2-4*(c)). The gap width of IPOCs and their pitch were variables in this experiment to study the mechanism of outgassing channels during the high-temperature anneal or epitaxial growth.

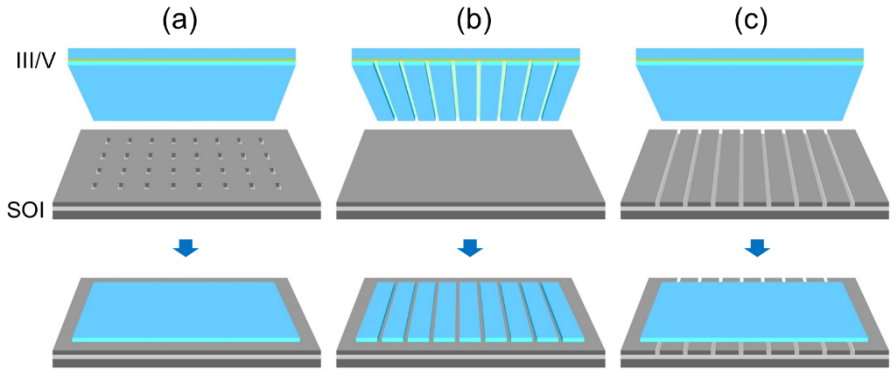

Figure 2-4. Illustration of outgassing channels pre- and post-bonding with (a) vertical outgassing channels; (b) in-plane outgassing channels on III-V side and (c) on silicon side

High-temperature anneal and regrow tests were performed on the direct bonded heterogeneously integrated III-V layer on Si, and the quality of the grown film was studied. The SOI substrate used in this test includes 700 nm silicon device layer and 1 μm buried oxide (BOX) layer, as shown in *Figure 2-5*. The MOCVD grown III-V layer stack used in this work contains InGaAsP multiple quantum wells (MQWs) with photoluminescence (PL) wavelength centered at 1550 nm. At the bonding interface, unstrained InGaAsP/InP super lattices (SLs) were grown to trap the point defects propagating through the bonding interface [5]. InGaAs that is lattice-matched with InP

was used as wet etch stop layer and the p-type contact layer for the device design. The total thickness of the III-V stack is about 2 μm.

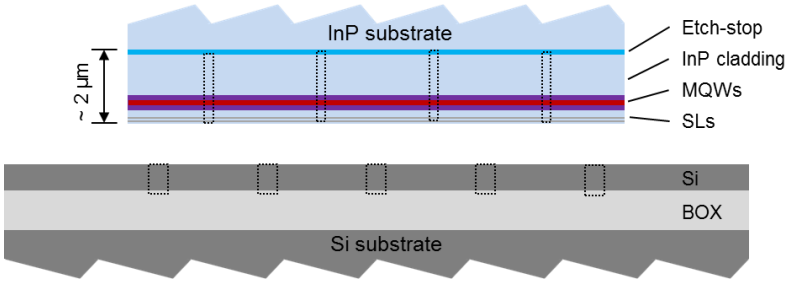

Figure 2-5. Structure of layer stack of III-V and SOI substrate. The dash box indicates the position of outgassing channels.

Outgassing channels on either the SOI or III-V wafer were etched prior to the wafer bonding process, as shown in *Figure 2-5*. After 300 °C bonding anneals followed by the InP substrate removal, a high-temperature annealing tests at 600 °C and 645 °C were carried out in a reduced pressure horizontal reactor MOCVD reactor. Trimethylindium (TMIn) and Tertiarybutyl phosphine (TBP) were used as precursors with H_2 as the carrier gas. The reactor pressure was kept at 300 Torr. The reactor temperature change was ramped slowly under Group-V gas flow to prevent the decomposition of the III-V compounds. InP regrowth was carried out under the same conditions.

This may cause serious gas bubbles and bonding film delamination. Discrete VOC array on the SOI with proper size and density assist to trap the gas inside the void, and diffuse the gas though less-dense BOX layer at 300 °C [4]. As shown in *Figure 2-6*(a), the bonded film with VOCs was annealed 45 minutes at 300 °C and a void-free, high quality bonded film was achieved (with a few particles in the microscope image). In comparison, serious deformation happened at same sample after being annealed at 600 °C for 10 minutes in a MOCVD reactor. The trapped gas in VOCs plus newly

generated byproducts from further reaction at bonding interface caused gas bumps above VOCs and delaminated and broken film, shown in *Figure 2-6*(b).

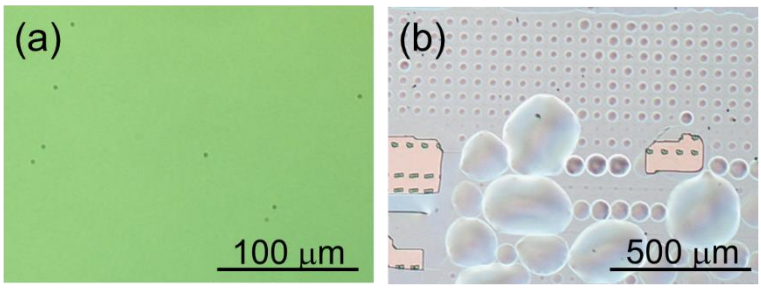

Figure 2-6. (a) Bonded thin III-V film after 45min anneal at 300°C and substrate removal, and then (b) annealed for 10min at 600°C in MOCVD reactor

To solve this problem, IPOCs were investigated, which have an advantage to expel the gaseous reaction products rather than trapping them particularly in a vacuum environment, and keep the pressure balanced at each side of the bonded film. IPOCs shown in *Figure 2-7*(a) were fabricated on the III-V side, corresponding to the type (b) in *Figure 2-4*(b). By either wet- or dry-etch, the III-V film is patterned with through trench before physical wafer bonding. Here, the substrate removal process, which involves wet-etch step, requires a careful control to avoid undercut into the bonding interface and cause yield degradation. As an alternative approach, VOCs were first applied on SOI for high-quality bonded film at 300 °C, and then the III-V was etched through to silicon surface to form IPOCs with VOCs exposed. In this way, the pressure imbalance is released at the local III-V layer boned on top of VOCs. *Figure 2-7*(a) shows results of bonded InP/Si sample with IPOCs annealed at 600 °C for 10 min. The distance between the neighbor IPOCs is 50 μm and the width of the channels is 30 μm. No void or gas bubble was seen after the anneal.

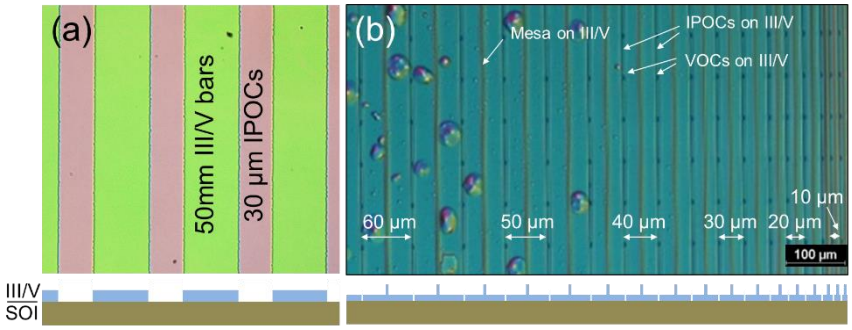

Figure 2-7. Heterogeneous integration samples with IPOCs on III-V side annealed for 10 min at (a) 600 °C and (b) 645 °C, respectively.

Figure 2-7(b) shows different structure: the bonded III-V film was etched down to form narrow ridges (2 µm width), with most area thinned below 300 nm, which is below the critical thickness at higher temperature (645 °C). The pattern has a series of III-V film width from 10 µm to 60 µm with a fixed IPOC width (1 µm). From the microscope image gas bubbles only appeared on III-V bars wider than 50 µm; micro-voids can be seen on the III-V bars wider than 30 µm. This agrees with the assumption that an increasing releasing rate of gas byproduct generation per unit time at high process temperature. At this point a higher density of outgassing channels is necessary, equivalent to a shorter diffusion length for newly generated gas at bonding interface. An III-V bar width of 30 µm is the upper limit to achieve bubble-free high-temperature anneal in this case.

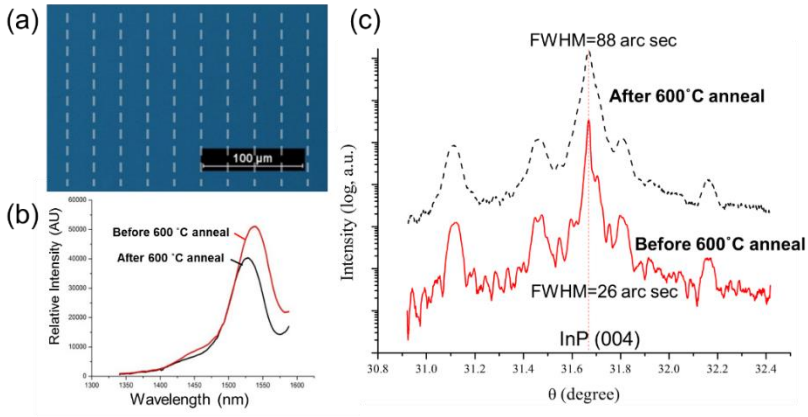

Figure 2-8. (a) Heterogeneous integration samples with IPOCs on SOI side annealed for 10min at 600°C and its (b) PL result and (c) XRD ω-2θ scan result

As another type of IPOC shown in Fig. 2, the trenches are directly etched on the SOI side. *Figure 2-8*(a) shows the bonded sample with IPOCs at SOI side annealed at 600°C for 10min. The dashed line in *Figure 2-8*(a) indicates the position of the straight IPOCs underneath the III-V stack. A benefit of having the IPOCs on the silicon side is that an unbroken and void-free film with smooth surface was obtained after annealing. Materials quality was evaluated with photoluminescence (PL) and high-resolution x-ray diffraction (XRD) measurements as shown in *Figure 2-8*(b) and (c), respectively. The PL signal of the MQWs inside the III-V stack retained 80% of the original intensity after the annealing. A 10 nm blue shift indicates a strain change in the system probably due to residual thermal strain. The XRD ω-2θ scan data shows the InP (004) peaks with satellite peaks representing the MQWs layers. Both the main peak and the sub-peaks are slightly broadened, which can be caused by degeneration in the III-V epi-layers. The positions of the satellite peaks are well aligned to that of sample before 600 °C anneal, indicating that residual strain in the system is not strong enough to alter MQW integrity.

2.3 Epitaxy on heterogeneous III-V/Si platform

The heterogeneously integrated III-V layer on Si is exposed to high ambient temperature for extended durations in the epitaxial regrowth due to the slow deposition rate (~0.4 nm/s). *Figure 2-9*(a) shows the top-view scanning electron microscope (SEM) 1 μm InP regrowth on top of bonded sample with 30μm wide IPOCs with 50 μm space, the corresponding cross-sectional view SEM image is shown in *Figure 2-9*(b). Bumps caused by gas expansion were observed at the center of the wide III-V stripe, indicating that the transition distance is too long for gases to diffuse to IPOC trenches. Precursor molecules reacted on top of the exposed silicon surface and formed poly-crystal clusters the wide IPOC trench. Due to these two factors, the width of both III-V bars and IPOCs need to be shrunk. As shown in *Figure 2-9*(c) and (d), the same bonded III-V-Si sample with 8 μm wide IPOCs and 30 μm III-V bars shows bubble free regrown surface. The larger aspect ratio of III-V areas to the exposed Si resulted in less poly-crystal deposition.

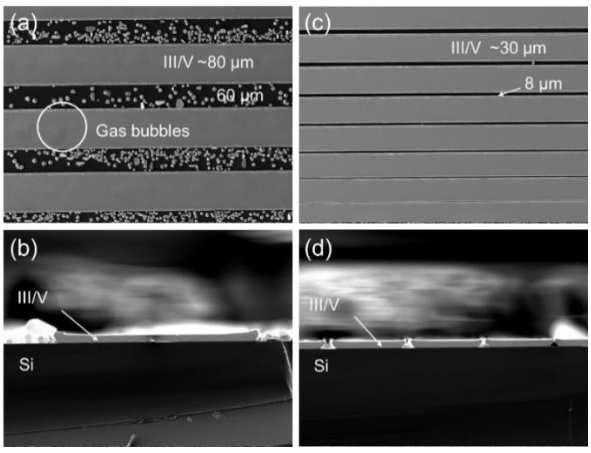

Figure 2-9. Top- and cross-sectional view of SEM images of 1μm InP regrowth on heterogeneous integration platform with IPOCs. Sample in (a) (b) has wide III-V stripes and sample in (c) (d) has narrow III-V stripes.

A major application to perform epitaxial regrowth onto heterogeneous integration system is to achieve low threshold lasers for high energy-efficiency applications. Selective regrowth of semi-insulating InP on laser ridge to form buried ridge structure could increase laser differential efficiency by well confining both electrical carriers and photons [16]. The nonradiative recombination happened at etched MQWs ridge sidewall can be improved with good regrowth interface [19, 20]. For this application, both VOCs and IPOCs are adopted which are compatible with a top-down heterogeneous III-V/Si process. As shown in *Figure 2-10*(a), "standard" VOCs designs were utilized for initial III-V epitaxial transfer. A laser mesa was then etched through the MQWs structure to form a deep ridge structure, using SiO_2 as the etch hard mask as well as cap layer for selective regrowth. IPOCs were subsequently patterned on III-V and to expose VOCs on SOI prior the high temperature regrowth step.

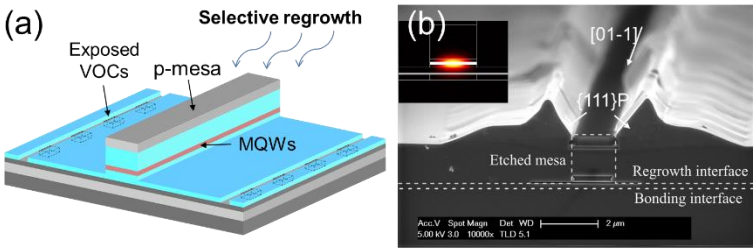

Figure 2-10. (a) Illustration of mesa patterned heterogeneous integration substrate and (b) the cross-section SEM result after selective InP regrowth on it. Insert: simulation of the optical mode in this system.

With such strategy, selective regrowth of 1 μm un-doped InP was performed at 600 °C on the mesa-patterned heterogeneously integrated III-V on Si. As shown in *Figure 2-10*(b), a clean and clear regrowth interface can be seen. Flat and uniform regrown films show no gas bubbles underneath in the area away from the ridge. It's notable that a "rabbit ear" shape was formed after the epitaxy on the III-V ridge, which is an

orientation dependent morphology that caused by the crystalline plane dependent growth rate. Particularly at the growth condition (e.g. temperature, V/III gas ratio), the growth rate at low index planes such as (100) is smaller than that of some high index planes such as (31-1) [21]; the growth rate at rate at {111}A plane is virtually zero which makes a deposition-free opening on top of SiO_2 hard mask. The insert in *Figure 2-10*(b) shows the simulated optical fundamental TE mode profile in this regrown waveguide structure. The mode is well confined, similar to regrown laser structure on pure III-V counterpart.

Due to the orientation-dependent growth morphology, regrowth on laser ridge with different orientations was also studied. *Figure 2-11*(a) compares the PL mapping data across the III-V ridge before and after the deposition. The mapping traces are shown as the dash line in the inset SEM image. The peak relative PL signal intensity of regrown III-V ridge oriented in [0-1-1] is about 40% of that of the ridge before the regrowth, but it's 10 times larger than the peak intensity of regrown ridge oriented in [0-11]. The corresponding inset SEM images show the difference of growth morphology at two orthogonal orientations: the regrown InP coalesced above the SiO_2 hard mask on the [0-11] ridge, and big opening can be seen on [0-1-1] ridge. In this case the scattering or absorption caused by the rough regrown film could be one of the main reasons of the big PL signal degeneration. Considering the scattering effect by the fluctuant morphology of regrown materials above the mesa, the active materials were believed to maintain a high quality after the high temperature regrowth.

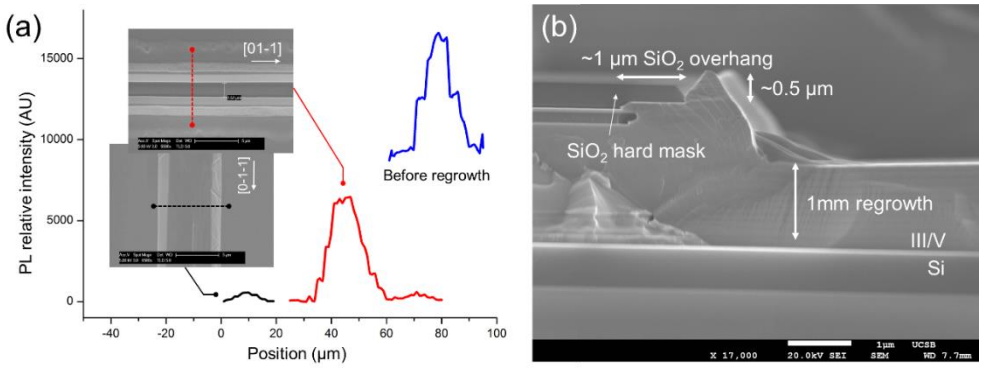

Figure 2-11. (a) PL density scanning across the III-V ridge before/after regrowth on heterogeneous integration substrate (with the same intensity scale). The insertion plain-view SEM images show the InP regrowth on the laser bars at two orthogonal crystal orientations. (b) Regrowth on the heterogeneous integration platform with selectively etched mesas with SiO_2 overhang.

The regrown morphology in orientations [0-1-1] is preferred for process convenience, but the "rabbit ear" kind of morphology in this orientation need to be suppressed. As one of the effective method, the hard mask overhang formed by selective etching can suppress the growth rate at perpendicular direction [22]. In the regrowth shown in *Figure 2-11*(b), ten InP regrowth of 100nm each and alternating with 2 nm InGaAs growth, and a clear growth contour can be seen on the cross-section SEM after a quick stain by wet etch. It shows that 1 μm SiO_2 overhang suppressed the first 600 nm InP regrowth and effectively decreases the height of the InP bump by over 60%.

2.4 Summary

This chapter has shown that wafer bonding is an efficient approach to integrate functional materials on passive silicon wafer. The low temperature bonding process is compatible with CMOS process, ensuring a flexible PIC design and high yield

fabrications. With a proper outgassing channel design, the bonding process is compatible with all the current low temperature wafer bonding and heterogeneous integration process.

The ability of epitaxial growth and regrowth will provide large freedom for photonics integration chip design on this heterogeneous integration device platform. As an example, the buried ridge stripe (BRS) device architecture can be applied to the InP/InGaAsP/Si system, which can help make ultra-low threshold current density lasers on silicon by confining the carriers and optical mode, and decreasing the surface recombination of the active region. More passive III-V structures can be integrated to the heterogeneous integration platform to increase the integration level and enrich the functionalities. Future work involves further enhancing the III-V quality after regrowth and fabricating heterogeneous photonic devices with the regrowth process.

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Chapter 3

Heterogeneously integrated lasers on silicon

The laser is the key component as the light source for semiconductor photonic integrated chips. Heterogeneous integration on Si, as introduced in previous chapter, has shown great potential as solutions of efficient and reliable laser source on silicon. Since Fang et al. demonstrated the first heterogeneously integrated laser on silicon in 2006 [1], there have been continuous efforts on developing laser diodes on the heterogeneous integration platform [2]. Fang et al. demonstrated single wavelength emission heterogeneous DFB lasers with a 25-mA threshold current and 5.4 mW maximum output power at 10 °C [3]. Liang et al. reported heterogeneous micro-ring laser with a threshold current as low as 5.4 mA and sub-mW output [4]. Keyvaninia et al. reported integrated DFB lasers on silicon with the wall plug efficiency higher than 9% [5]. Integrated multi-channel transmitters with DFB laser diodes and high-speed modulators on the heterogeneous integration platform were achieved with the quantum well intermixing method [6, 7]. In this chapter, a low threshold and low power consumption DFB laser on silicon is discussed for the application of chip-level optical interconnects. Furthermore, the thermal limit of the SOI substrate is discussed,

with novel thermal shunt proposed to improve the thermal performance of heterogeneous integrated micro-ring lasers.

3.1 Heterogeneous DFB laser on silicon

An integrated laser source with single wavelength emission as well as low power consumption is highly desirable in a cost-efficient WDM system [2]. Therefore, low threshold and high wall-plug efficiency is one of the key aspects for the laser source. DFB laser diodes have been proven to be a good candidate for the laser source used in WDM optical networks, due to its reliable structure and single wavelength operation. A single-frequency emission from a DFB is ensured by appropriate Bragg gratings in gain section, which are usually etched corrugations on silicon waveguide in the heterogeneous integration. This is one of the advantages of this platform: the grating fabrication only involves in silicon process with no epitaxial regrowth or other complex process.

3.1.1 Device design and fabrication

Considering the power budget of a chip-level communication system, normally a mW-level output power is required for the laser source. Therefore, a short cavity DFB (SC-DFB) is preferred, not only to minimize the threshold current, and to enhance the wall-plug efficiency at low output power range. A small cavity area also helps improve the dynamic performance for lasers' direct modulation [8].

The structure of the heterogeneous SC-DFB laser is shown schematically in *Figure 3-1*(a). The devices were fabricated with a III-V epitaxial wafer and an SOI wafer with a 500-nm device layer and a 1 μm buried oxide (BOX) layer. The III-V layer stack has

seven strained InAlGaAs QWs with graded index separate confinement hetero-structure (GRIN-SCH) layers, as shown in *Table 3-1*. The insert in *Figure 3-1*(a) is in cross-section view of the calculated fundamental transverse electric (TE) mode. The confinement factor in the QW region is about 5.6%. 50% of the optical mode is confined in the silicon slab waveguide, and consequently gratings on silicon provide strong coupling constants.

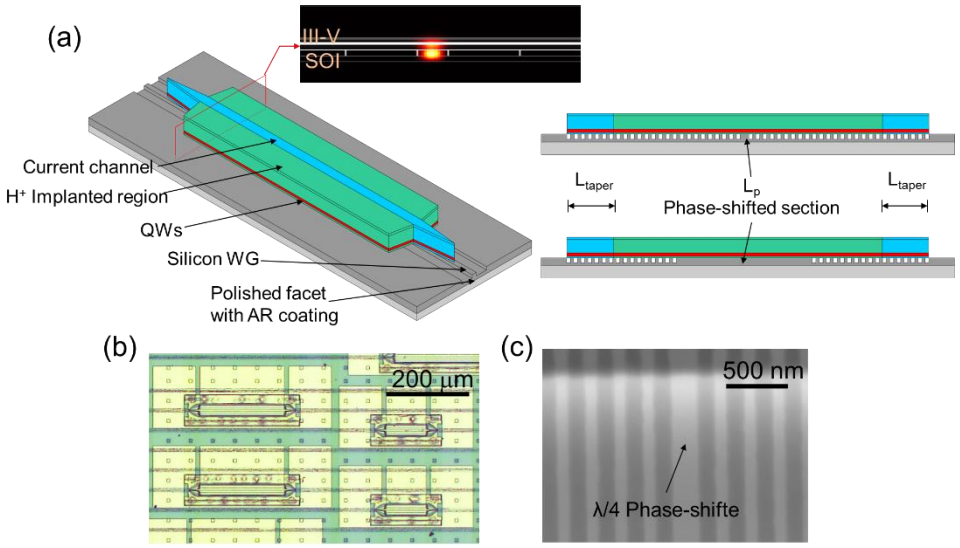

Figure 3-1. (a) Illustration of a heterogeneous DFB laser and a schematic lateral view with a grating on the waveguide; (b) a microscope image of the laser chip after fabrication; (c) SEM image of a first order grating with a λ/4 phase shift.

Table 3-1. The epitaxial III-V layer structure

Layer composition	Doping level	Thickness
P-type contact $In_{0.53}Ga_{0.47}As$	Zn: 1×10^{19}	200 nm
P-type cladding InP	Zn: 1.5×10^{18}->5×10^{17}	1500 nm
GRIN-SCH $In_{0.53}Al_xGa_{0.47-x}As$ (x:0.34->0.155)	UID	100 nm
QW $In_{0.6758}Al_{0.06}Ga_{0.2642}As$ (7×)	UID	6 nm
Barrier $In_{0.4411}Al_{0.085}Ga_{0.4739}As$ (8×)		9 nm
GRIN-SCH $In_{0.53}Al_xGa_{0.47-x}As$ (x:0.155->0.34)	UID	100 nm
N-type contact InP	Si: 1×10^{18}	110 nm
$In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$/InP (2×)	Si: 1×10^{18}	7.5/7.5 nm
Bonding layer InP	Si: 1×10^{18}	10 nm

The 1.5 μm wide silicon waveguide was etched 280 nm deep from a 500-nm thick device layer on the SOI substrate. The first-order grating sections on the silicon waveguide were defined with a JEOL JBX-6300FS E-beam lithography (EBL) system. Cleaved III-V pieces were bonded to a pre-patterned SOI substrate with a low temperature hydrophilic bonding process [10]. A reactive ion etching (RIE) tool was adopted to etch the III-V mesa down into the QW layer and then a selective wet etch was used to etch to the n-type contact layer. Pd/Ti/Pd/Au and Pd/Ge/Pd/Au metal stacks were deposited as contact metals for p- and n- type contacts, respectively. With the transmission line measurement (TLM) method the specific resistance of the n-contact was measured to be about 5×10^{-5} $\Omega\cdot cm^2$ and that of the p-contact was about 6×10^{-6} $\Omega\cdot cm^2$. As shown in *Figure 3-1*(a), the different color in the center of the 24-μm mesa indicates the 4-μm current channel that was defined by proton implantation. 20 μm III-V tapers on the front and rear end of cavity work as the mode converter between the III-V/Si section and a 2 μm wide passive waveguide. This wide waveguide is then tapered back to 800 nm to make sure a single mode transmission. This approach minimizes coupling losses between III-V/Si section and passive waveguide [11].

The samples were diced into columns with DFB laser arrays, after processing. The diced silicon waveguide facets were mechanically polished and then coated with bi-layer anti-reflective (AR) films to reduce the facet reflection around the lasing wavelength. *Figure 3-1*(b) shows the top-view microscope image of the finished devices, and *Figure 3-1*(c) shows the scanning electron microscope (SEM) image of the dry-etched grating on silicon. The duty cycle (DC) of the grating is defined by the ratio

of the etched groove width relative to the pitch of grating. The first order grating we used has a DC of about 60%, as shown in *Figure 3-1*(c).

The grating pitch Λ and coupling constant κ of first-order Bragg gratings can be estimated with the coupled mode theory [12],

$$\Lambda = \frac{\lambda}{2\bar{n}_{eff}} \tag{3-1}$$

$$\kappa = \frac{2\Delta\bar{n}_{eff}}{\lambda}\sin(DC \cdot \pi) \tag{3-2}$$

In the equations, λ is the center wavelength defined by the Bragg grating pitch. $\bar{n}_{eff}$ and $\overline{\Delta n}_{eff}$ are the average effective refractive index of the cavity and the perturbation by the grating corrugation, respectively. The first-order surface gratings were etched 90 nm deep on the silicon slab waveguide and a strong grating κ was achieved to be about 1000 cm^{-1} at 1550 nm, which provides flexibility in the short cavity design. The mirror loss of the DFB cavity can be tuned over a large range by choosing the length of the phase shift section in a fixed length cavity. Meanwhile it varies κL_g value that represents the reflection strength of the DFB cavity.

Two designs with different types of the phase-shifted section were adopted for 100 μm and 200 μm DFB cavities. The upper image in *Figure 3-1*(c) shows the quarter-wavelength phase-shifted DFB cavity design, which is widely used in DFB cavity designs since it is able to avoid the detuning away from the resonant wavelength of the grating and the degeneration of fundamental mode [13, 14]. The lower image in *Figure 3-1*(c) shows another strategy with a longer phase-shifted section. By changing the grating length from 5 μm to 40 μm, κL_g values of the DFB cavity were tuned from 0.5 to 4, and then leave a relative long blank phase-shifted section. In comparison, a quarter-

wavelength phase-shifted section design has a stronger grating with κL_g of about 10 for 100 μm cavity and 20 for 200 μm.

The transmission characterization of these two kinds of DFB cavity could be calculated with the fundamental matrix method [15]. *Figure 3-2* shows the calculated theoretical threshold modal gain condition. Γ_{QW}, g_{th}, α_i and L represent the confinement of optical mode in the quantum wells, threshold gain coefficient, internal loss of cavity and cavity length, respectively. L breaks down to phase-shifted section length L_p and grating length L_g. The horizontal coordinate represents the detuning factor $\delta L = (\beta - \beta_0)L$, where β and β_0 are the average propagation constant and Bragg wavenumber, respectively. *Figure 3-2*(a) shows the cavity modes in a cavity with quarter-wavelength phase-shifted section, corresponding to a $\pi/2$ phase shift for Bragg wavelength. With a larger κL_g, by increasing coupling coefficient of gratings, the threshold modal gain drops down both for the center optical mode ($\delta L=0$) and the neighboring side mode, with an increasing wavelength shift from Bragg condition.

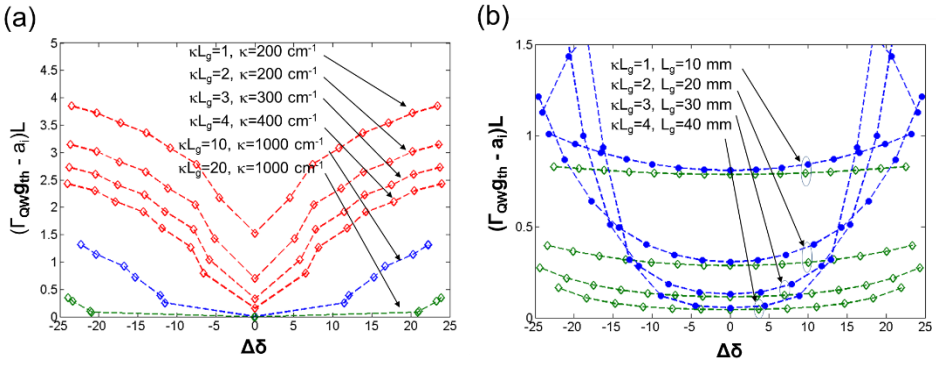

Figure 3-2. Relationship between threshold modal gain and threshold wavelength for cavity modes with (a) constant quarter wavelength phased shifted section with varying κ or (b) constant κ = 1000 cm^{-1} with varying L_p to get a κL_g=1,2,3,4. The blue circles and green diamond curve in (b) represent total cavity length of 100 μm and 200 μm, respectively. L_g is the length of grating section.

3.1.2 Characterization

After fabrication, the laser bars with polished and AR coated waveguide facets were mounted onto a temperature controlled measurement stage. Then the output light was collected into a calibrated integrating sphere with InGaAs photo-detector. An optical spectrum analyzer (OSA) was used to take the spectrum data by coupling the light into a lensed fiber. *Figure 3-3*(a) shows the light-current (L-I) and current-voltage (I-V) characteristics of heterogeneous DFB laser with 100 μm and 200 μm cavity lengths under continuous-wave (CW) operation. Both lasers have quarter wavelength phase-shifted section in the center of the cavities with a grating pitch of 238.6 nm for 100 μm DFBs and 240.1 nm for 200 μm DFBs. From the I-V curves, the series resistance of the heterogeneous DFBs is about 2 Ω·mm for the 24 μm wide cavity with 4-μm current channel. The threshold current for 200 μm DFB laser was measured to be 8.8 mA and it corresponds to a threshold current density of 1.1 kA/cm^2. The maximum CW output power is about 3.75 mW from both waveguide facets. The 100-μm DFB laser has a threshold current of 10 mA and threshold current density of 2.5 kA/cm^2. The increase in threshold current density in the 100-μm cavity is due to the increasing mirror loss in a shorter cavity, because of weaker grating reflection. The lasers can maintain a single longitude mode operation up to 1 mW output. *Figure 3-2*(a) indicates the threshold modal gain conditions between neighbor modes are close in a strong reflection (high κL_g) cavity, so mode competition occurs when current injection or temperature fluctuates in the active region. The output spectra of the SC-DFB lasers are shown in *Figure 3-3*(b). These spectra indicate that both lasers have single wavelength emission at wide wavelength range with a side mode suppression ratio (SMSR) larger than 55

dB. The low power level was due to the coupling loss between lens fiber and silicon waveguide. The kinks at higher injection current relate to longitude mode hopping. As shown in the insert in *Figure 3-3*(a), the large SMSR of 100 μm is only associated within a small injection current range due to mode hopping, and a stable and single wavelength output was observed within this current range. 200 μm DFBs, otherwise, has consistent hop-free single mode output and large SMSR up to 40 mA.

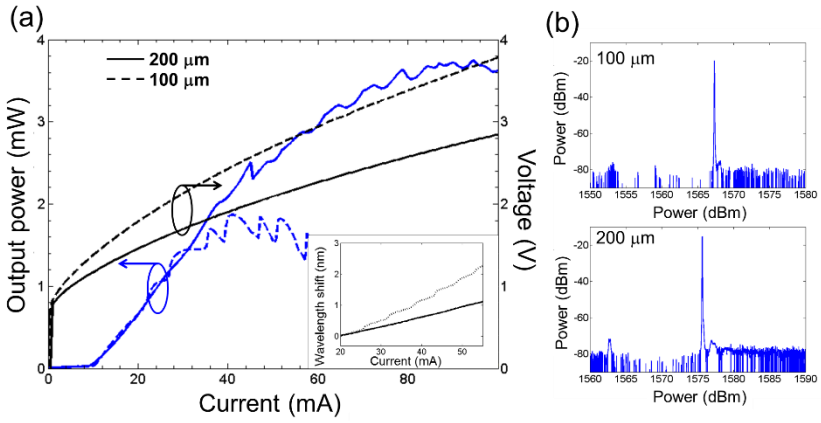

Figure 3-3. (a) L-I and I-V curves of 200 μm (solid line) and 100 μm (dash line) heterogeneous DFB lasers with quarter phase-shifted section and (b) the corresponding lasing spectrum at 20mA injection current; The insert in (a) is the central wavelength shift with injection current.

The wide stop bandwidth of the heterogeneous SC-DFBs is corresponding to the strong coupling coefficient of the gratings. With the fundamental matrix method as shown in *Figure 3-2*(a), the stop band of 200 μm and 100-μm heterogeneous DFB with quarter wavelength phase- shifted section is about 22.9 nm and 25.2 nm, respectively. The measured stop band from the amplified spontaneous emission spectrum of these two lasers are 25.6 nm and 27.6 nm. But this measured stop band was also affected by the materials gain bandwidth.

The performance of SC-DFB with long phase-shifted section, on the other hand, depends on the cavity mirror loss that is decided by κLg value. Since it is a DBR-like cavity, the cavity mirror reflection can be estimated by:

$$R \sim (\tanh(\frac{\kappa L_g}{2}))^2 \quad (3\text{-}3)$$

Figure 3-4(a) and (b) show experimental data of threshold current and wall plug efficiency at 1 mW output for the 100 μm and 200 μm DFB lasers with a cavity varying κL_g. They were compared with calculated curves assuming the internal loss of the cavity is 25 cm^{-1}, materials gain is 966 cm^{-1} and injection efficiency is 60%. Both the calculation and measured data show a trend that the threshold current decreases with increasing κL_g for both cavity lengths and the optimum wall plug efficiency is around κL_g =1.5 with a compromise between slope efficiency and threshold current. The calculations show a lower threshold and higher wall plug efficiency is predicted for shorter cavity length but the experimental data behaves otherwise. Thermal degenerations are thought to be the main reason for this deviation other than device process variations.

Figure 3-4(c) and (d) show the optical spectrum of SC-DFB lasers with κL_g = 4 and a drive current of 30 mA. The corresponding phase-shifted section length is 60 μm for 100 μm cavity and 160 μm for 200-μm cavity. The mode spacing is narrower, and multiple longitudinal mode peaks are observable, but a SMSR larger than 40 dB is still achieved.

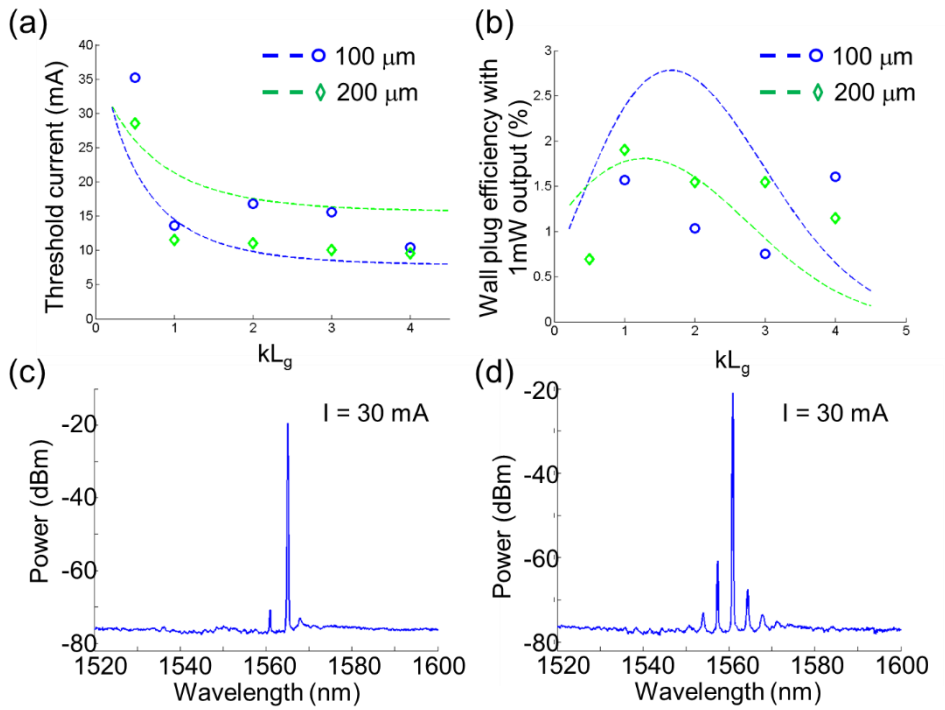

Figure 3-4. (a) Threshold current and (b) wall plug efficiency at 1mW output power for the 100 μm and 200 μm DFB lasers with phase-shifted section. Dash line: simulated results. The lasing spectrum of (c) 100 μm and (d) 200 μm cavity length with κL_g =4 at 30 mA injection current.

In the heterogeneous silicon platform, one large barrier to improve the energy efficiency is the thermal performance of active devices due to the low thermal conductivity of BOX layer. Laser diodes with shorter cavities have worse thermal impedance, which needs to be compensated by lower working power consumption. The laser threshold degenerates exponentially with rising stage temperature [12]. By measuring the threshold of short cavity DFB lasers with pulse injection, the temperature factor T_0 of 200 μm and 100-μm quarter wavelength phase-shifted DFB lasers were 41.5 K and 30 K, respectively.

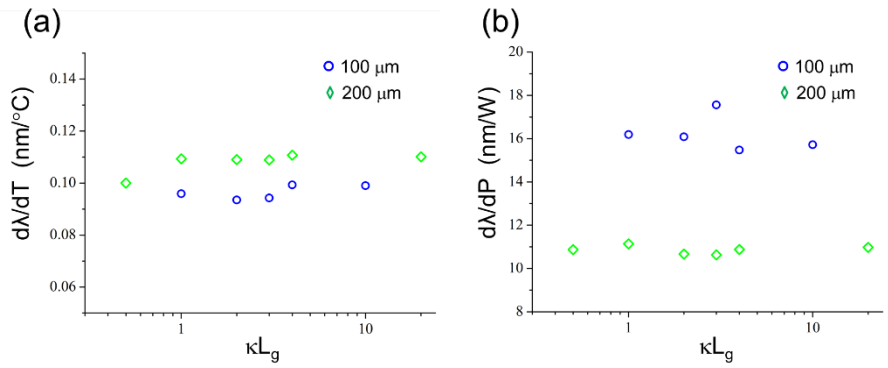

Figure 3-5. (a) Ratio of lasing wavelength shift with the change of stage temperature at CW lasing condition and (b) ratio of lasing wavelength shift with the input electrical power of the laser.

Additionally, the thermal performance of SC-DFB lasers with varying phase-shifted length is compared. The ratio of lasing wavelength shift with the change of stage temperature for all the designs are concentrated at 0.10 – 0.11 nm/°C for SC- DFBs, as shown in *Figure 3-5*(a). The lasing wavelength shift with the input electrical power of the laser was also measured to be 16 nm/W for 100 μm DFBs and 11 nm/W for 200 μm DFBs, which is shown in *Figure 3-5*(b). These two ratios are related to the thermal impedance of heterogeneous cavity and behave independently with grating strength, and no distinguishable thermal performance influenced by the length of phase-shifted section in short DFB cavity.

The high-speed characterization of SC-DBR laser was also studied. The small-signal intensity modulation was measured at 20 °C stage temperature with a light-wave component analyzer (LCA, Agilent N4373C) with a GSG probe. The electro-optical (EO) response of the 200-μm heterogeneous DFB with quarter wavelength phase-shift is shown in *Figure 3-6*(a). The maximum 3 dB bandwidth of the device is about 9.5 GHz with 56 mA driving current. *Figure 3-6*(b) shows the linear relation between the relaxation oscillation frequency (f_r) with the square root of bias current above the

threshold. The slope of f_r curve is about 1.185 GHz/mA$^{1/2}$. The EO response of 100 μm heterogeneous DFB and its higher slope of 1.452 GHz/mA$^{1/2}$ are shown in *Figure 3-6*(c) and (d).

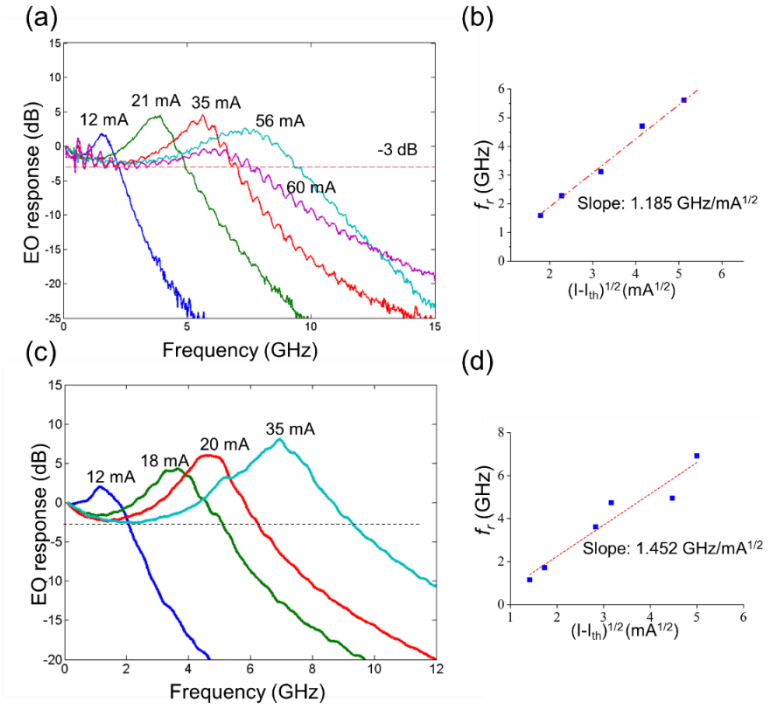

Figure 3-6. Small signal response of (a) 200 μm and (c) 100 μm heterogeneous DFB laser with quarter wavelength phase shifted section at different driving currents; the dependence of relaxation oscillation frequency on the driving current of (b) 200 μm and (d) 100 μm heterogeneous DFB laser.

To evaluate the high bit rate performance of the heterogeneous SC-DBR, a large signal transmission measurement was carried out at 20 °C with 2^{31-1} non-return-to-zero (NRZ) pseudorandom bit sequence (PRBS) pattern. The 200 μm DFB was driven above the threshold and the bias was tuned to reach the optimized eye diagram when the driving current was 62 mA. The driving electrical signal with a 1.5 V swing on the voltage is shown in *Figure 3-7*(a) with a 6-dB attenuator. *Figure 3-7*(b)-(d) indicate open eye diagrams up to 12.5 Gbps.

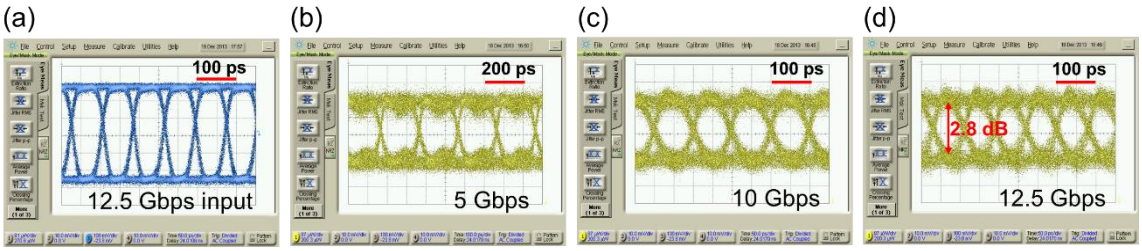

Figure 3-7. Eye diagram of (a) diving voltage signal and the digital modulation of 200 μm DFB with the bit rate of (b) 5 Gbps (c) 10 Gbps and (d) 12.5 Gbps.

3.2 Heterogeneous ring laser and thermal management

A reliable photonic communication circuit is normally required to work properly at a wide range of ambient temperatures, for example, close to the processor core or inside the server stacks in a datacenter. This, therefore, is a challenge for integrated lasers, which are temperature sensitive elements. Specifically, the heterogeneous integrated laser on silicon has prominent thermal issues due to the thick buried oxide (BOX) layer in the SOI substrate. This thick oxide layer, with a thickness from 1 to 3 μm in general, is necessary for low waveguide loss from substrate leakage. *Table 3-2* lists selective materials available in photonic integration, showing that the common used dielectric in Si photonics, SiO_2, Si_3N_4 and polymers, have about two orders smaller thermal conductivity compared with silicon or InP. Therefore, the poor thermal conductivity of thick BOX layer in SOI forms a barrier for heat generated in the device layer to be dissipated in the silicon substrate, which is a major obstacle for the heterogeneous silicon platform to achieve higher energy efficiency and higher integration density [16].

Table 3-2. Thermal conductivity of selective materials

Materials	Thermal conductivity (20 °C, W/m·K)
Dry air	~ 0.02
Thermal SiO2	1.38
PECVD Si3N4	1.5
Polymer (SU8, BCB)	0.3
Silicon	130
InP	68
Sapphire	27
Copper	401
Gold	318

The previous discussion of short cavity DFB lasers on Si shows a fast thermal rollover on the L-I curve, and a performance degradation with shorter cavity length with the device thermal impedance scaling with the cavity length. This is one of the major issues for lasers on SOI substrate, especially for those with a compact footprint and large thermal impedance, e.g. micro-ring type ridge lasers.

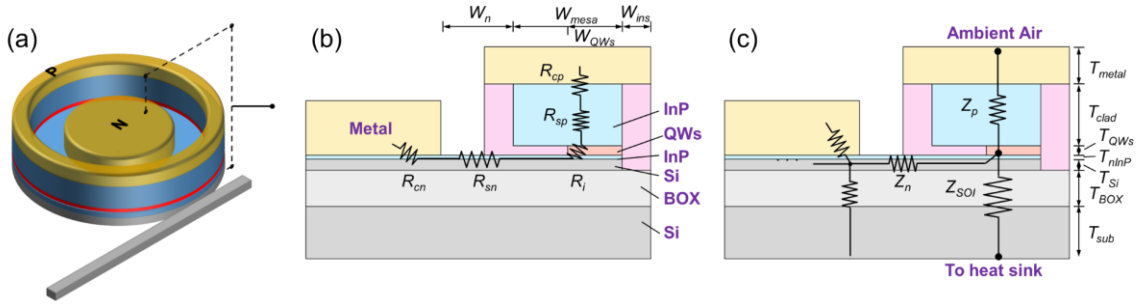

Figure 3-8. (a) Diagram of a HSMR laser and schematic device cross-section with (b) electrical resistance model and (c) thermal resistance model

The heterogeneously integrated silicon micro-ring (HSMR) laser (*Figure 3-8*) has a small footprint and small threshold current, which makes it a good candidate for the application of large capacity optical interconnection [4, 17]. However, HSMR lasers are with larger thermal impedance due to large series resistance of small cavity volume. Their performance degrades rapidly with increasing input power and at rising ambient

temperatures. Previous research shows a maximum CW lasing temperature at 65 °C for a 50 μm diameter device [18], which limits its use in many applications.

Efforts have been made to improve the thermal performance of integrated lasers on SOI substrate. Creazzo et al. proposed a heterogeneous structure where III-V materials were placed in an etched slot/hole in SOI substrate and bonded with its silicon substrate directly with a metal layer [19]. This structure avoids the buried oxide thermal barrier issues we intend to resolve in this section, so naturally has better thermal performance than devices built on the heterogeneous platform. However, its manufacturing efficiency and improved performance are yet to be seen due to requirement in process accuracy and loss related to light coupling between Si and III-V waveguide. For HSMR lasers with small cavity volume, the injection efficiency was improved by undercutting the active region [18], and device heating was reduced with a metal shunt design [20]. The idea of thermal shunt is to utilize the thermal conductive material (e.g. metal) as bridge between high temperature core and the substrate. Here a novel double-shunt design is proposed and demonstrated to improve the thermal performance of HSMR lasers.

3.2.1 Thermal analysis of heterogeneous ring lasers

When the active region temperature of the quantum well (QW) laser increases, the bimolecular recombination rate decreases and the Auger recombination rate increases [21], so the quantum efficiency of the laser is reduced. The correlation between temperature and laser threshold can be described by the empirical equations [12]:

$$I_{th} = I_0 e^{T/T_0} \tag{3-4}$$

$$\eta_d = \eta_{d0} e^{-T/T_\eta} \tag{3-5}$$

The above equations indicate that both the threshold current I_{th} and differential quantum efficiency η_d typically degrade exponentially with temperature, with characteristic temperatures T_0 and T_η. Both characteristic temperatures are related to thermal impedance of the device, Z_T, which is dependent on device materials, structure geometry, and the location of heat source.

The major heat source in semiconductor QW lasers is Joule heating [22]. The equivalent model of electrical resistance of cross-section of in shown in *Figure 3-10*(b). *Table 3-3* lists the cross-section geometric dimensions of HSMR laser used in calculations and designs, as labeled in *Figure 3-10*(b) and (c). The total series resistance is broken into several components: contact resistance (R_{cp}, R_{cn}), cladding resistance (R_{sp}, R_{sn}), and intrinsic layer resistance (R_i). *Table* 3-4 lists the typical values for each component. Their contribution to the overall Joule heating can vary depending on the device geometry and doping concentration. It's noted that the n-type contact resistance and cladding resistance usually dominate, because of limited contact region in the center of the ring, and the small thickness of the n-InP contact layer.

Table 3-3. Cross-section geometric dimension for HSMR laser

W_{QWs}	1.5 μm	T_{QWs}	260 nm
W_{mesa}	3 μm	T_{nInP}	110 nm
W_{ins}	0.8 μm	T_{Si}	300 nm
W_n	2 μm	T_{BOX}	1 μm
T_{metal}	1 μm	T_{sub}	600 μm
T_{clad}	1.7 μm		

Table 3-4. Series resistance of a typical HSMR laser

Components		Resistance (Ω)
P	R_{cp}	2.5
	R_{sp}	2.4

Intrinsic	R_i	2.9
N	R_{cn}	3.2
	R_{sn}	3.7

Figure 3-8(c) shows the simplified impedance model from thermal prospective, where Z_n, Z_p, and Z_{SOI} represent the thermal impedance when heat transmits through n-contact layer as well as the silicon layer underneath, p-mesa and the SOI substrate with thick BOX layer, respectively. The position of heat sink relative to heat source is important here, which affects the heat flux as well as the involved thermal impedance components. The heat sink is usually set underneath substrate for the normal chip placement in testing setup and device package. It turns out that the BOX layer with small thermal conductivity dominates in the overall thermal impedance of the device.

A commercial 2-D finite element modeling tool [23] was used to numerically simulate heat-transmission inside the device structures, as shown in *Figure 3-9*. The thermal conductivities of materials used in a HSMR laser structure are listed in Table III. Metals normally have much larger thermal conductivity compared with most semiconductor materials. Most dielectric materials used in silicon photonics have poor thermal performance.

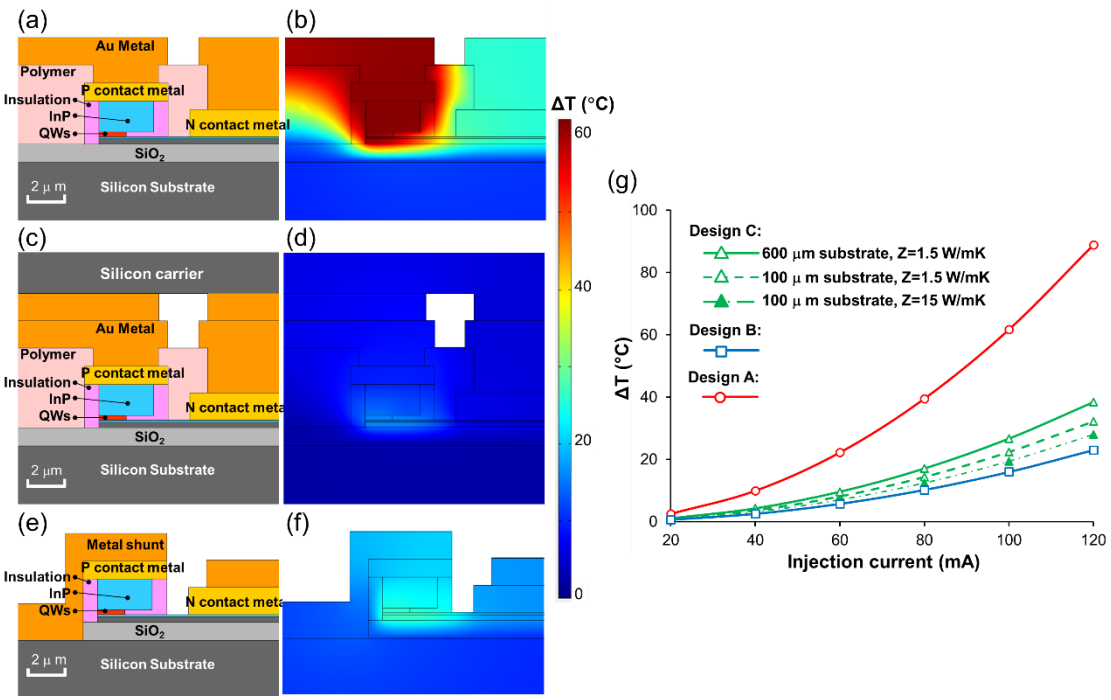

Figure 3-9. Diagrams of cross-section structures of HSMR lasers and the simulated temperature contour for (a) (b) design A, (c) (d) design B, and (e) (f) design C. All results are simulated for a 50 μm diameters ring with 100 mA injection current; (b) (d) and (f) share a same temperature scale which is shown at the right side; (g) shows the maximum temperature changes at the laser active region with varied injection current for three designs.

Three types of structures were compared in *Figure 3-9*. They share the same active region and mesa claddings with different strategies on thermal management. A constant temperature was used as boundary condition at the bottom of silicon substrate, which represents an ideal thermal sink.

1) Design A: The standard HSMR laser structure with polymer passivation, as demonstrated in *Figure 3-9*(a)(b). Both polymer around the p mesa and SiO_2 in the substrate have poor thermal conductivity, confining the thermal energy in the limited volume of III-V materials. The active region temperature is raised by 62 °C with 100 mA injection current.

2) Design B: A ‘flip-chip bonding’ design. To bypass the SOI substrate, the device was flip-chip bonded to a 200-μm silicon carrier wafer with the heat sink underneath, as shown in *Figure 3-9*(c)(d). The p-type and n-type metal were connected to metal wires on the carrier wafer and served as the heat conduction media. The heat generated at active region dissipates into heat sink through the p-mesa into carrier wafer efficiently and the active region stays cool.

3) Design C: A ‘p-metal thermal shunt’ design, as shown in *Figure 3-9*(e)(f). The 1 μm BOX layer was etched through with metal filled in. Thick metal covers the entire III-V mesa including the steep sidewall, efficiently "shorting" the heat from active region, p-mesa all the way to the silicon substrate.

Thick Si_3N_4 was used as dielectric layer to isolate the active region with metal to avoid a large absorption loss. The simulation results indicate an effective heat transmission between heat source and heat sink with the maximum temperature at the active region much lower than design A.

The active region temperature for all three designs is shown in *Figure 3-9*(g). Design A has the worst thermal performance. The overall impedances for each design with 50 μm diameter are 420 °C/W, 109 °C/W and 181 °C/W, respectively.

The flip-chip bonding approach has the best cooling efficiency. But it normally requires high-precision position alignment and is incompatible with integration with electronics and external optical fibers. The difficulties in process and package make it less desirable.

It is worthwhile to note that further optimization can be done by tuning the device structures. As shown in the plots in *Figure 3-9*(g), a thinner SOI substrate (100 μm)

improves the thermal impedance by 16% compared with a 600-μm substrate [24]. An additional 12% improvement could be achieved by improving the thermal conductivity of insulation layers from 1.5 W/(m·K) to 15 W/(m·K), although the availability of these materials in our fabrication facilities were limited in this work.

In addition, the above simulations were based on a simplified model that neglects the boundary thermal resistance. The multiple layer system in practice has more complex heat transmissions and larger thermal impedance based upon the surface treatment process as well as the deposition techniques.

3.2.2 Device design and fabrication

There are two aspects to optimize the thermal performance of a HSMR laser based on the previous discussion: heat sources and heat-flux path. The former requires improving the injection efficiency and the device series resistance; the latter requires optimization of the metal thermal shunt design. A double thermal-shunt structure is investigated here to improve the previous design [20] (*Figure 3-10*(a)). A p-metal thermal shunt with 50-μm width was connected with the ring mesa. The n-metal thermal shunt with a 20-μm width was connected to the n–metal across the bus waveguide. 1 μm dielectric layer was used to insulate the p-shunt and mesa as well as between the n-shunt and p-contact. Gold was used for metal shunts in this experiment. The active region of the III-V ring mesa includes five InAlGaAs QWs with center photoluminescence peak at 1310 nm. Compressive strain in the QW layer was used to further decrease internal loss in cavity and increase the differential gain.

HSMR lasers with diameter of 20 μm, 30 μm and 50 μm were fabricated with the heterogeneous integration process using the process flow shown in *Figure 3-10*(b)-(j). A low temperature hydrophilic bonding technique was used to transfer III-V thin layer with gain materials to a patterned SOI substrate [25]. No precise position alignment was required for the wafer bonding process. A standard top-down III-V process was followed to fabricate mesa structure with metal electrodes deposited. As the last step of the process, the SOI substrates were thinned down to 150 μm.

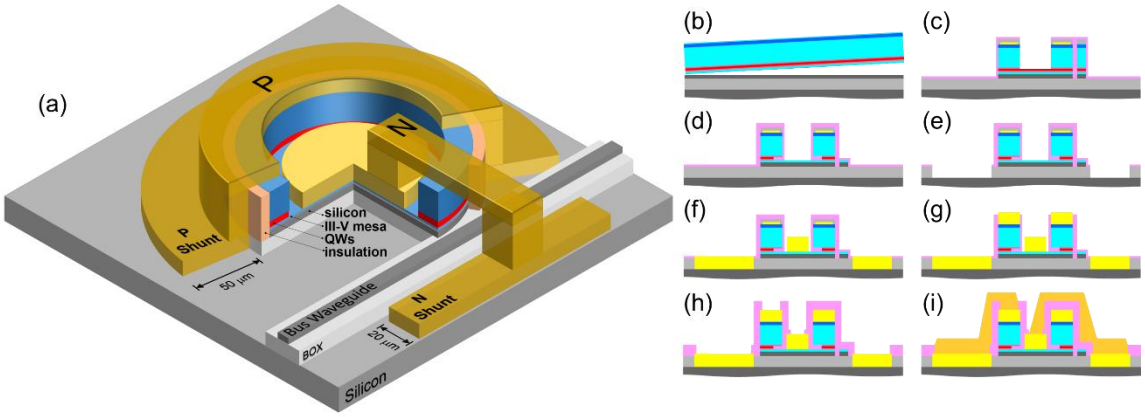

Figure 3-10. (a) The diagram of a HSMR laser with double thermal shunt design. (b) to (j) illustrate the heterogeneous integration process flow: (b) passive components were etched on SOI then bonded with III-V film; (c) Ring mesa was defined by dry etches; (d) active region was undercut by wet etches; (e) BOX layer was etched through with dry etching method; (f) n-contact metal deposition; (g) p-contact metal deposition; (h) device was passivated by thick dielectric materials deposition and via openings were etched; (i) Shunt metal as well as probe metals were deposited.

Figure 3-11 shows the plain-view scanning electron microscope (SEM) and optical microscope images of the fabricated HSMR lasers with thermal shunts highlighted. A control design without thermal shunt structure was processed on same wafer in parallel, as shown in *Figure 3-11*(b), for which the mesa structures were same except the BOX layer was left un-etched. *Figure 3-11*(c) shows the cross-section SEM image of

the ring mesa with thermal shunt design. It shows that the 3 μm thick p-metal shunt fully covers the entire mesa with a top to sidewall thickness ratio of 3:1. 1 μm SiO2 served as the insulation layer between the shunt and active region. It also shows the 700-nm undercut at the active region to increase the injection efficiency. But the undercut is not uniform inside the ring due to an anisotropic wet etch. *Figure 3-11*(d) shows the 3-D view microscope image of the device with the large height contrast from margin area with the mesa top that was capped by thick metal.

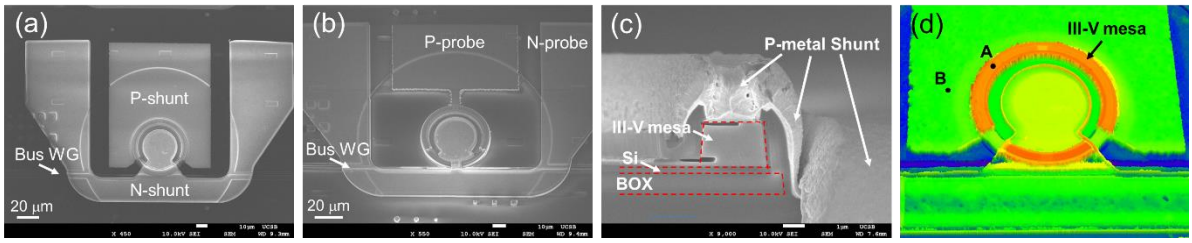

Figure 3-11. Plain-view SEM images of (a) HSMR lasers with double thermal shunt design and (b) control design without thermal shunt; (c) cross-section SEM image of the laser mesa with highlighted metal shunt coverage at the mesa sidewall; (d) 3-D microscope image of the fabricated devices. The height contrast between the mesa top (spot A) and p metal shunt (spot B) is about 3.2 μm. Devices shown above are with 50 μm diameter.

3. Heterogeneous micro-ring laser with thermal shunt

The fabricated chips were placed p-side up on a copper heat sink with temperature stabilized by a thermoelectric cooler. The output light from one side of the bus waveguide was coupled into a cleaved fiber through vertical grating couplers, while the output from the other side was collected by the on-chip photodetectors. A calibrated external InGaAs photo-detector was used to detect the output power from grating couplers. An optical spectrum analyzer was used to detect the light spectrum.

Figure 3-12 compares the L-I and I-V curves of HSMR lasers with and without thermal shunt designs, corresponding to the devices shown in *Figure 3-11*(a) and (b),

respectively. The output power was measured from single side output. From the I-V curves it was seen that the series resistance of the devices was not affected by thermal shunts design, which implies an equivalent heat source for both structures. When the stage temperature was at 20 °C, both devices shared the same threshold current around 12.3 mA. The device without thermal shunt had earlier thermal roll-over in the output power, and its maximum CW lasing temperature was about 70 °C. The device with double thermal shunts, in contrast, was able to CW lase up to 105 °C. The L-I curves show a slower thermal roll-over at same stage temperature with the output power 8 to 10 dB higher.

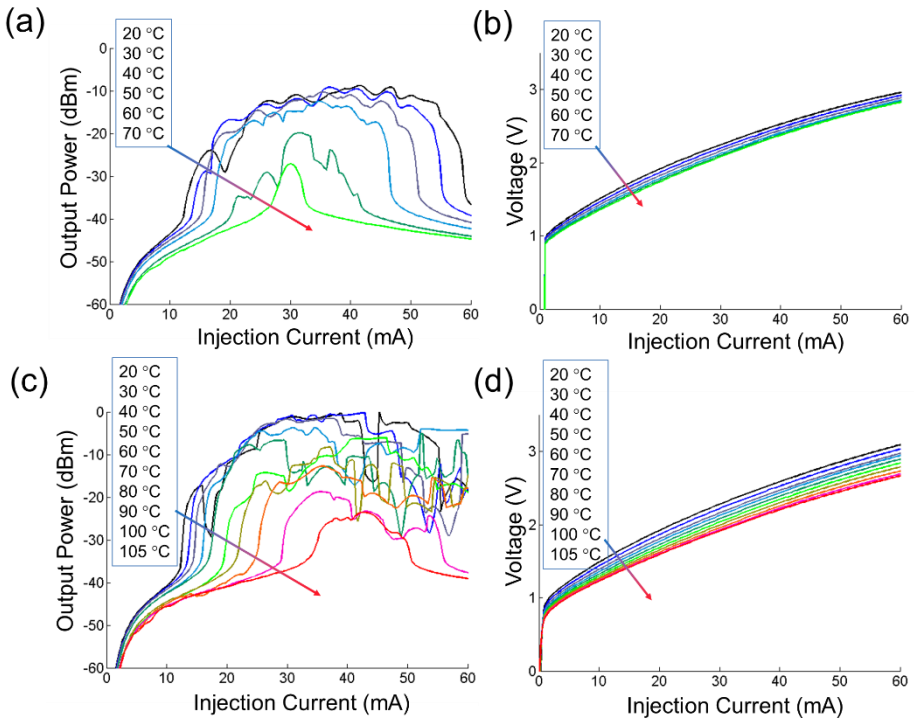

Figure 3-12. (a) L-I curves and (b) I-V curves of 50 μm diameter HSMR laser without thermal shunts at different stage temperatures; (c) L-I curves and (d) I-V curves of HSMR laser with same geometry as well as double thermal shunts at different stage temperatures.

A thermal reflection technique [26] was used to measure the temperature at the device surface. *Figure 3-13*(a) shows the thermal reflection images and temperature increment with injection current on the same devices shown in *Figure 3-11*. It shows that the 50 μm HSMR laser without thermal shunt had rapid temperature increase with higher injection currents. The heating was concentrated at the top of the ring mesa. The temperature change on the device with double thermal shunts was much less significant, with the heat spread into neighboring shunt regions. This gives clear evidence on the improvement of device thermal impedance by the thermal shunts designs.

Temperature monitoring spots were chosen at p-mesa top and center of the n-metal pads, with the temperature evolution curves shown in *Figure 3-13*(b). The trend of the temperature curves matches well with the simulation results in *Figure 3-9*(g). For the device without a thermal shunt, the big temperature contrast between p-mesa and n-metal indicates ineffective heat transmission mesa through the thin n-contact layer and silicon device layer. With the same injection current at 93 mA, the temperature at the p mesa top at the device with double thermal shunts was 17 °C, about 65 °C lower than that of the control design. The large temperature difference provides clear evidence on the improvement of thermal impedance by the effective heat transmission by thermal shunts.

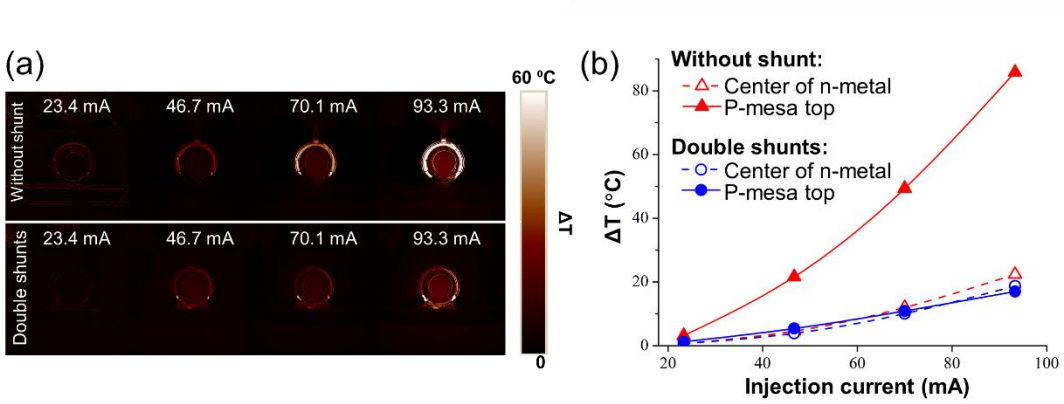

Figure 3-13. (a) Thermal reflection images of 50 mm HSMR lasers with and without thermal shunt designs which show the temperature increment and distributions with different injection current. (b) The temperature changes at the monitoring spots on the devices.

The thermal performance of HSMR lasers with smaller radii was also investigated. The total series resistance of device increases with smaller device geometry. SEM images of double thermal shunt HSMR laser with a 30 μm and 20 μm diameters were shown in *Figure 3-14*(a) and (b), respectively. The p-metal shunt coverage was limited by size of the ring as well as the position of bus waveguide. Similarly, the respective lasing characteristic of the devices were compared in *Figure 3-14*(b)(c) and (e)(f). Smaller HSMR lasers had lower output power roll-over compared with the 50 μm ones. Notable improvements on the output power as well as lasing temperature were observed with the thermal shunt design.

Figure 3-15(a) shows the spectra of HSMR lasers with thermal shunts. The free spectral range for 50 μm, 30 μm and 20 μm ring diameters were 3.11 nm, 5.18 nm and 7.81 nm, respectively. The CW output light wavelength shift with dissipation power and stage temperature of the HSMR lasers were studied, as shown in *Figure 3-15*(b) and (c). The temperature changes at the active region with self-heating by injected electrical power were shown in *Figure 3-15*(b). The slope of the fitting lines is listed in

Table IV. By ignoring the 1.2% change on series resistance for 10 °C temperature difference, the self-heating was assumed to be constant, and the wavelength shifts with stage temperature were independent on the size of ring and the thermal shunt designs, as shown in *Figure 3-15*(c).

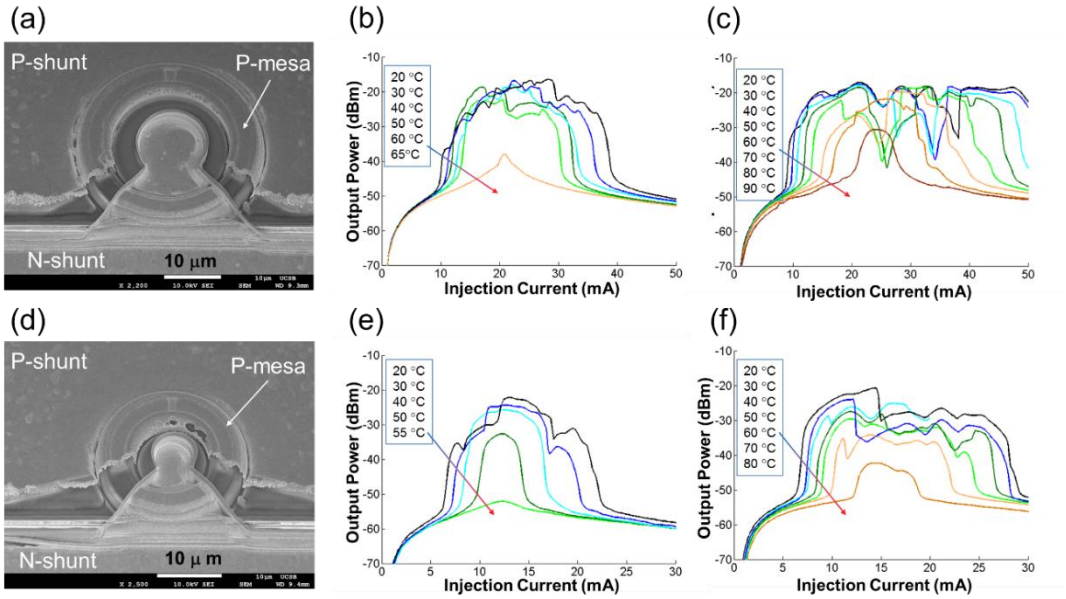

Figure 3-14. Plain-view SEM images of HSMR lasers with (a) 30 μm and (d) 20 μm diameters with thermal shunts. (b) L-I curves of 30 μm control design without thermal shunt and corresponding (v) thermal shunt design; (e) L-I curves of 20 μm control design without thermal shunt and corresponding (f) thermal shunt design.

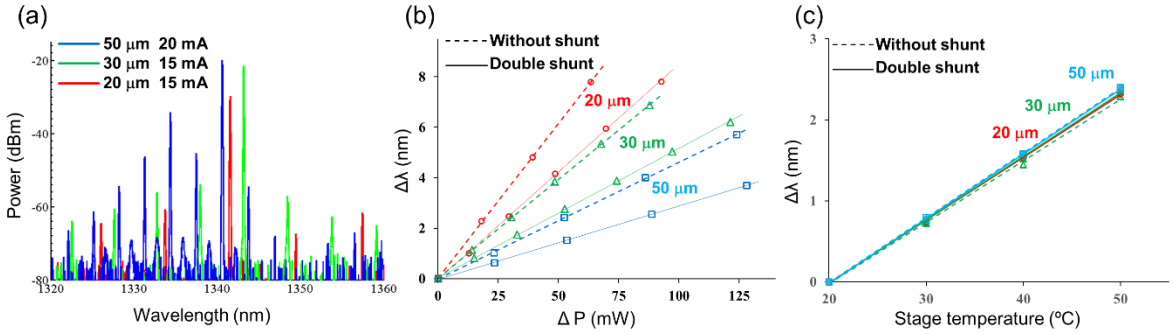

Figure 3-15. (a) The spectra of HSMR lasers with thermal shunts. (b) Wavelength shift with injection power increment for HSMR lasers with different diameters. (c) Wavelength shift with stage temperature for HSMR lasers with different diameters.

The thermal impedance of the HSMR lasers can be calculated with followed equation:

$$Z_T = \frac{d\lambda}{dP} / \frac{d\lambda}{dT} \tag{3-6}$$

The calculated thermal impedance values for the devices with and without thermal shunt with varying diameters were listed in *Table 3-5*. As can be seen that 30% to 40% improvement in thermal impedance was achieved on the devices with thermal shunts, with the maximum CW lasing temperatures raised by over 35 °C.

Table 3-5. Performance of HSMR lases with or without thermal shunt

	Diameter (μm)	**Maximum CW Temperature (°C)**	**dλ/dP (nm/W)**	**Z_T (°C/W)**
Without shunt	50	70	46.3	579.9
	30	60	78.4	1031.3
	20	50	122.5	1591.1
Double shunt	50	105	29.0	363.9
	30	90	51.3	653.2
	20	80	85.1	1105.1

With the help of reduced device heating from efficient thermal shunt design, devices now can operate at higher direct modulation bandwidth. *Figure 3-16*(a) is a comparison of small-signal direct modulation response for two devices with the same dimension of 50 μm in diameter, same injection current of 25 mA and similar output power. The one with thermal shunt shows a 3-dB bandwidth of 5.5 GHz while bandwidth for the other one without shunt is only 3 GHz. *Figure 3-16*(b) is the same measurement on the device with thermal shunt at different injection current. Higher injection current, corresponding to higher output power (before thermal rollover), leads to larger bandwidth, which is expected. A maximum bandwidth of 7.8 GHz is observed at 35 mA injection current. *Figure 3-16*(b) inset is a plot of resonance

frequency vs. square root of DC injection current, showing expected linear dependence. The slope is 0.81 GHz/mA$^{1/2}$, 3× better than previously demonstrated heterogeneous Si DBR lasers [27], although still lower than that of the heterogeneous DFB lasers with large cavity and higher output power that shown in previous section.

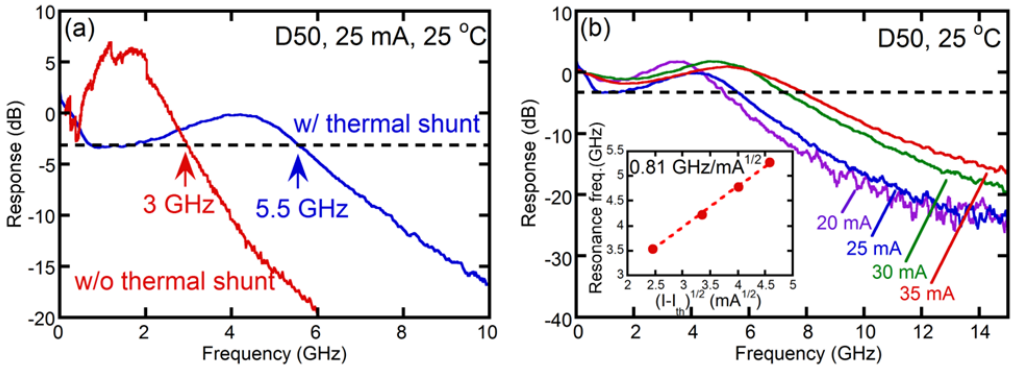

Figure 3-16. (a) Measured small-signal responses for D=50 μm devices at 25 mA injection current with and without thermal shunt design, and (b) small-signal response for thermal shunt microring laser at 20 to 35 mA injection current. Inset: resonance frequency as a function of square root of DC injection current.

We also measured the large-signal direct modulation response of the same device at a constant injection current of 30 mA at 25 °C. The measurement setup is schematically shown in *Figure 3-17*(a). Pseudo Random binary sequence (PRBS) electrical signal with a length of 2^7-1 and a voltage swing of 1 V from the pattern generator was combined with a DC bias corresponding to 30 mA injection current in a bias-tee and sent to the device. The output of the device was collected by a single-mode optical fiber and amplified by a semiconductor optical amplifier (SOA) at 1310 nm regime. To suppress amplified spontaneous emission (ASE) noise from SOA, a filter is required before the modulated signal was measured by the optical module of a digital communication analyzer (DCA). The clock between PRBS and DCA is synchronized to measure the eye diagram in DCA. *Figure 3-17*(b)-(d) are measured eye

diagram at 5, 10 and 12.5 Gbps, respectively. Open eye diagram is observed at all three data rates and the respective extinction ratio is 8.9, 8.6 and 7.9 dB, corresponding to respective power consumption is 13.2, 6.6 and 5.28 pJ/bit. The noise at "1" level is mainly from the stage temperature fluctuation between 25-27 °C because thermal electrical controller which was used for previously shown temperature-dependent LI measurement was not available when the dynamic measurement was performed. Furthermore, the 1 nm optical filter bandwidth is not narrow enough to filter out most of the ASE noise, which also contributes to the noise in the eye diagram.

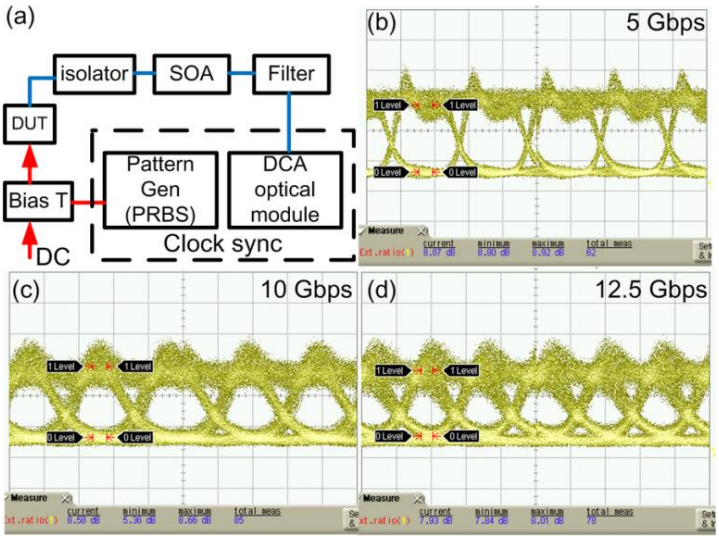

Figure 3-17. (a) Schematic of large-signal measurement setup, and measured open eye diagrams for a D=50 μm device at 5 (b), 10 (c) and 12.5 Gbps (d) modulation rate.

3.3 Summary

We demonstrated short cavity heterogeneous DFB lasers with low thresholds and showed that quarter wavelength phase-shifted sections show better performance than a long phase shift, both on mode stability and side mode suppression ratio. The large

direct modulation bandwidth of the heterogeneous SC-DFB shows its potential for an integratable low cost and low power laser source.

We also compared strategies to optimize the thermal management for HMSR lasers. We proposed novel double thermal shunts designs that effectively improve the thermal impedance of the device as well as the overall performance. The experimental results show that a compact HSMR laser with 50 μm diameter achieved a maximum lasing temperature at 105 °C, which matches the record of lasers on the heterogeneous integration platform [28]. This is important for HSMR lasers to be used in interconnection applications in un-cooled environment, such as data centers. Further improvement could be done by using metals with higher thermal conductivity, such as copper, which is also CMOS process compatible, to optimize the efficiency of the thermal shunts.

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Chapter 4

Heterogeneously integrated modulators on silicon

This chapter introduce the recent work on heterogeneously integrated modulators on Si. Two types of modulators were designed: electro-absorption modulators and Mach-Zehnder interferometer modulator (MZM) for different applications, with the devices design and characterizations discussed in the two sections, respectively.

4.1 High-speed heterogeneous electro-absorption modulator

4.1.1 Introduction

An optical modulator converts the electrical signal into an optical signal in an optical link, and its performance, such as the bandwidth, extinction ratio, and linearity, largely decide the overall performance of the optical communication. The modulation of optical beam can be realized by changing the refractive index of transmission media with electro-optic (EO) effects for a phase modulator or intensity modulator if combined with an interferometer or resonator structure; modulation can also be achieved by changing the absorption of the medium that the light propagates through, e.g. the EAM that will be discussed in this section.

Due to weak and largely nonlinear EO effects silicon is not an ideal candidate for optical modulation. In the case of refractive modulation, a pure silicon modulator utilizes mainly the plasma dispersion effect by switching the carrier density with carrier injection or depletion approach. An interferometer (e.g. MZM) or resonator architecture (e.g. ring modulator) is used for the intensity modulation. Silicon MZMs normally have a long phase section due to the inefficient refractive index tuning, so a high-speed operation requires traveling-wave electrode designs that are power hungry with the low loading resistance [1-5]; In comparison, a silicon ring modulator has compact footprint benefitting from the tight bending radius silicon waveguide. But silicon rings are very sensitive to the phase error caused by fabrication variation, so a channel tuning and stabilization mechanism is required for practical use, and the narrow optical bandwidth limits its modulation speed in an optical link [6-9].

Unlike silicon, III-V materials, such as InP and GaAs have stronger EO effects in first and higher order, including plasma effect, band filling effect, quantum confined Stark effect (QCSE), and Pockels effect [10, 11]. InP based phase modulators have shown efficient phase tuning with smaller V_π per unit length [12]. For intensity modulation, the format of III-V electroabsorption modulated laser (EML) has been widely used in products for commercial optical interconnects [13-15]. The mechanism behind EA modulators is mainly the QCSE effect – the energy bandgap of quantum-wells or quantum-dots and therefore its absorption edge can be manipulated by the external electric filed. The advantages of III-V EA modulators are their large bandwidth with compact footprint and high extinction ratio with small voltage swing V_{pp} compared with common silicon modulators [13-15].

With the heterogeneous integration method discussed in previous chapters, III-V materials can be combined with silicon waveguide to improve the modulator designs on silicon substrate. Similar to the heterogeneous III-V/Si laser, heterogeneous modulator has one/multiple heterogeneous sections serving as a phase tuning or absorptive section depending on the III-V active region design. In previous works, heterogeneously integrated MZMs with sectional travelling wave electrodes with low V_{π}·L [16] and high speed EAM with lumped [17, 18] and travelling-wave electrode [19] have been demonstrated, showing great advantages of heterogeneous integration on the silicon modulator applications. In following section, a silicon photonic circuit with lumped EA modulator array working in the C-band is designed and fabricated for the application of chip-level optical interconnects.

4.1.2 Device design and fabrication

Figure 4-1 shows the device structure and a top-view SEM image of our heterogeneous EA modulator. The EA modulator in *Figure 4-1* has three sections: adiabatic tapers, where the silicon waveguide tapers down from 1.5 μm wide to narrower width underneath the cavity; the main cavity with certain III-V mesa width and silicon WG width; and an isolation section where the p-InP mesa is passivated with proton implant to isolate between the modulator cavity with the long tapers.

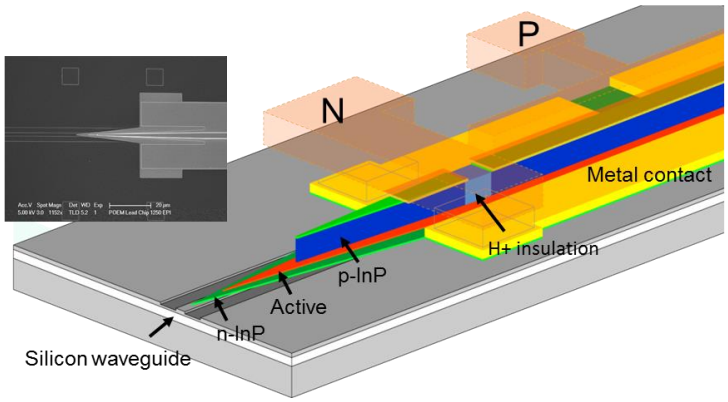

Figure 4-1. 3-D device structure of heterogeneous EAM. Insert: top-view SEM image of III-V taper.

The optical mode propagating in the silicon waveguide is coupled into a 'hybrid' optical mode in the III-V/Si section through adiabatic tapers. 60 μm multiple levels III-V taper length was chosen as a trade-off between the mode coupling efficiency and loss from active absorption. The III-V layer stack design of EAM shares the same cladding, contact and bonding SLs layers as the laser epi, as shown in *Table 4-1*. The QWs/SCH layers are specially designed, with 10 QWs with PL wavelength centered at 1480 nm, optimized for large extinction ratio and minimum insertion loss in the C-band wavelength range.

Table 4-1. The III-V epitaxial structure for EAM

Layer composition	Doping level	Thickness
P-type contact $In_{0.53}Ga_{0.47}As$	Zn: 1×10^{19}	200 nm
P-type cladding InP	Zn: 1.5×10^{18}->5×10^{17}	1500 nm
SCH $In_{0.5289}Al_{0.166}Ga_{0.3051}As$	UID	100 nm
QW $In_{0.4884}Al_{0.015}Ga_{0.4966}As$ (10×)	UID	11 nm
Barrier $In_{0.5702}Al_{0.284}Ga_{0.1458}As$ (11×)		7 nm
SCH $In_{0.5284}Al_{0.193}Ga_{0.2786}As$	UID	100 nm
N-type contact InP	Si: 3×10^{18}	110 nm
$In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$/InP (2×)	Si: 3×10^{18}	7.5/7.5 nm
Bonding layer InP	Si: 3×10^{18}	10 nm

Figure 4-2 shows the cross-sectional view of the III-V/Si mesa in the EAM. Its design is compromised for a few factors: optical confinement in the quantum wells,

propagation loss in the heterogeneous waveguide, and electrical properties such as series resistance and junction capacitance that is essential for the modulator's dynamic performance. The width of the III-V p-mesa and the silicon waveguide are set to 3 μm and 1 μm, respectively, with the confinement factor of the fundamental TE mode in the well/barrier region to be 41%, as shown in the mode profile in *Figure 4-2*.

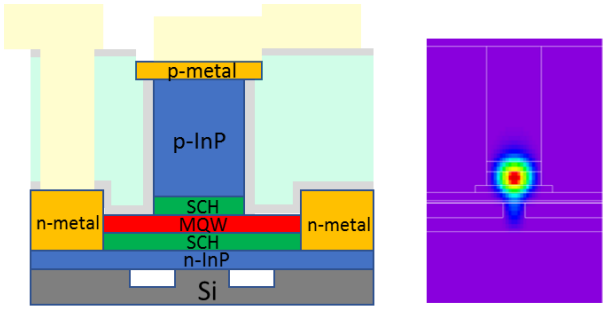

Figure 4-2. Cross-section view of the modulator heterogeneous section and fundamental TE mode profile.

The heterogeneous EA modulators were fabricated in house using the process flow shown in *Figure 4-3*. First, an SOI wafer with 500 nm device thickness and 1 μm buried oxide layer (BOX) was patterned with an i-line lithographic tool and then partially etched with C_4F_8/SF_6/Ar in a reactive ion etch (RIE) chamber. After III-V die bonding onto the SOI wafer and removing the InP substrate, the thin III-V film included the n-InP contact layer, InAlGaAs MQWs stack, p-doped InP cladding, and p-InGaAs contact layer (n-side down). It is worth noting that neither precise position alignment nor high temperature anneal was required for the wafer bonding process.

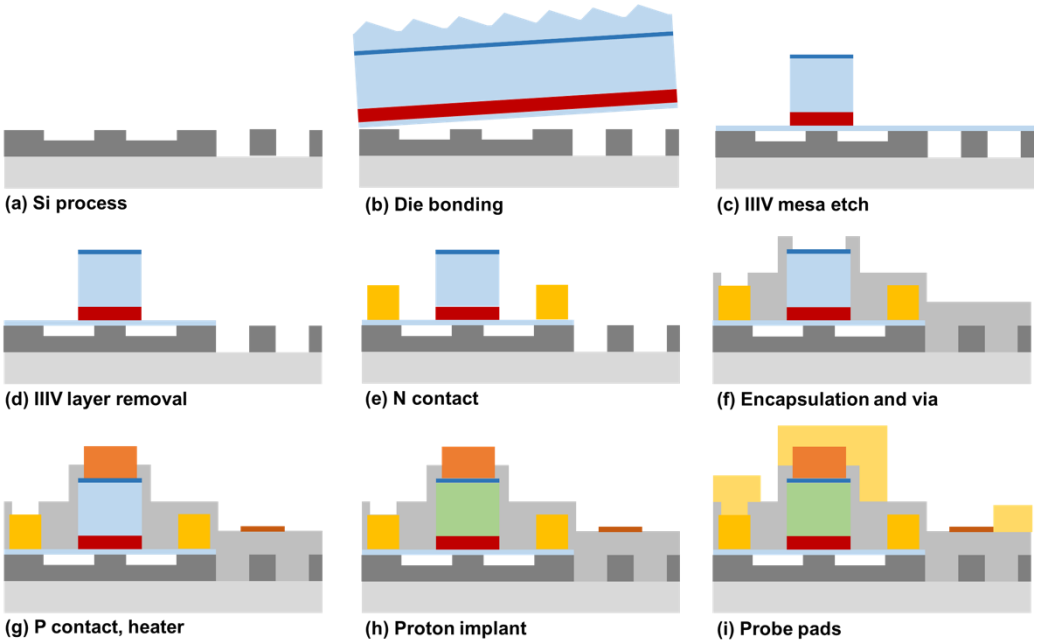

Figure 4-3. The process flow of heterogeneous EA modulator: (a) define the passive components on silicon; (b) transfer III-V layers to patterned SOI substrate, and remove the InP substrate through wet-etch; (c) etch the III-V mesa and QWs stack; (d) remove the III-V layer on the waveguide; (e) deposit n-type contact metal stack on n-InP; (f) encapsulate the surface with thick SiO_2 layer and etch deep via; (g) deposit p-type contact metal stack, deposit heater metal stack; (h) proton implant to isolate the taper and modulator cavity; and (i) deposit probe pads.

A CMOS compatible top-down III-V process was then performed. The 3 μm wide mesa was etched with methane/H_2/Ar RIE etch, and then the MQW layer was wet etched to expose the n-contact layer. After the n-type metallization, a thick SiO_2 layer was deposited to protect and isolate the electrodes. P-type metal was deposited after a deep via was etched on top of the mesa. Pd/Ti/Pd/Au and Pd/Ge/Pd/Au metal stacks were deposited as contact metals for p- and n- type contacts, respectively. Proton implant was adopted to isolate the mesa with the tapers. Finally, thick metal pads were deposited on both n- and p- contact metal for probe contact. The chip was diced into columns, and the waveguide facet was mechanically polished for fiber coupling and testing.

The DC characterization of the heterogeneous EAM was performed with a tunable laser source. The light is coupled into silicon waveguide through lensed fiber with 2 μm tip size. The input light is kept at TE polarization. *Figure 4-4*(a) shows the transmission power after the 100 μm long EAM with a series of input wavelengths at different reverse bias level from 0 to 6 V. The transmission-bias curves indicate a large extinction ratio at proper working voltage. Larger insertion losses are seen at shorter input wavelength as expected due to a higher absorption loss when it's closer to the PL wavelength of the QWs. This is supported in *Figure 4-4*(b), which shows the modulation extinction ratio per 1 V bias swing changing with the working point (the 1-level). It shows that the modulator has a larger extinction ratio at lower bias working point when it is operated at shorter wavelength. However, larger power penalty was seen at 1540 nm compared with longer wavelength. The best working point, after this trade-off, can be chose for each wavelength point. For 1550 nm and 1560 nm, the power penalty is 1.5-2 dB if 3 dB extinction ratio fulfills the requirement of error-free transmission.

This insertion loss breaks into two major parts: loss from active section of the EAM, mainly the QCSE effect of the MQWs layers, and loss from the taper, which includes both absorption loss and passive coupling loss, as shown in *Figure 4-4*(c) and (d), respectively. With a cut-back method, the active losses of the EAM cavity are 38 dB/cm, 62 dB/cm and 91 dB/cm at wavelength of 1560 nm, 1550nm, and 1540 nm, respectively. The deviation in *Figure 4-4*(c) is mainly caused by the poor repeatability of fiber coupler with 800 nm wide silicon waveguide and its facet reflection. The total loss per taper is about 0.3-0.42 dB per taper for those wavelengths. In summary, the

total insertion loss of the 100 μm long heterogeneous EAM is less than 1.5 dB in C-band, and 3-4 dB total loss at on-off key operation depending on the working point configuration.

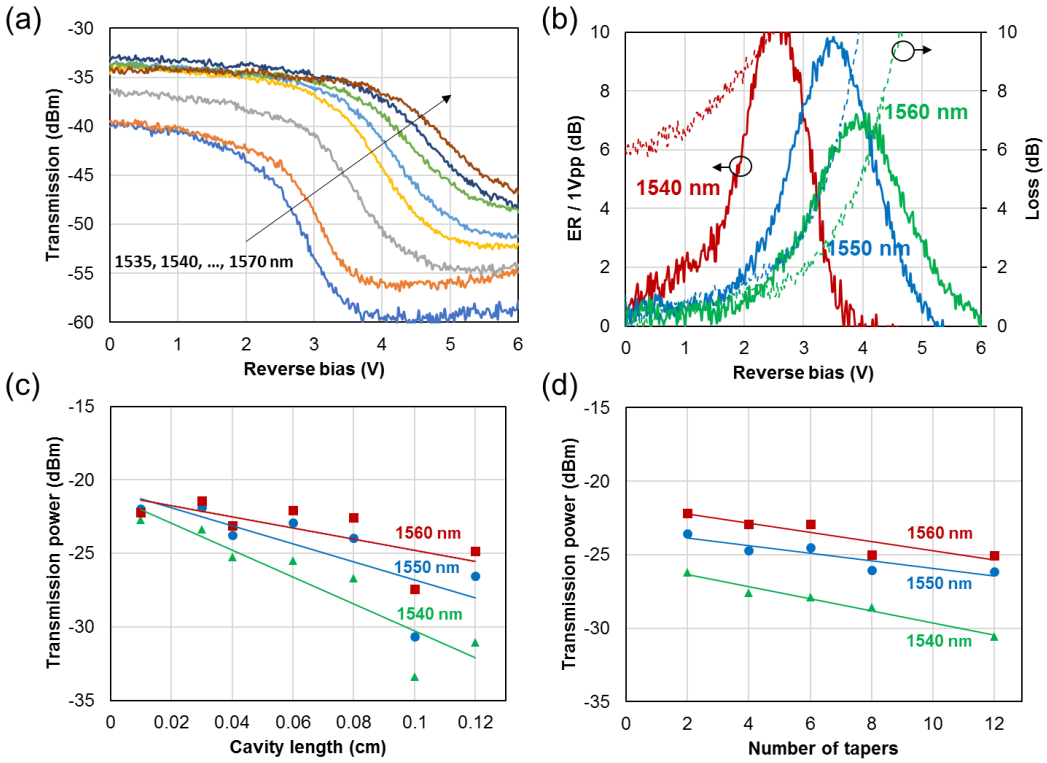

Figure 4-4. (a) Power transmission of 100 μm long EAM versus input wavelength and reverse bias; (b) the extinction ratio per 1 V_{pp} and insertion loss changes with reverse bias; (c) insertion loss changes with EAM cavity length; and (d) insertion loss changes with number of tapers.

The small signal frequency response of the heterogeneous EAM is performed with LCA, as shown in *Figure 4-5*(a). With thick oxide passivation and planarization, the EAM with 100 μm long and 3 μm wide cavity has 3-dB bandwidth up to about 20 GHz with 4 V reverse bias at 1560 nm. Large signal testing at C-band wavelengths, with a 2^{15}-1 PRBS input PRBS signal from pattern generator, is shown in *Figure 4-5*(b). 1 V bias swing is used in 12.5 Gbps and 1.6-2 V in 25 Gbps operations, with the bias point optimized for each condition. Clear eye diagrams are seen with 4-7 dB extinction ratio.

The noise in the eye diagram is mainly from the amplification of weak optical signal after the lossy fiber-waveguide couplings.

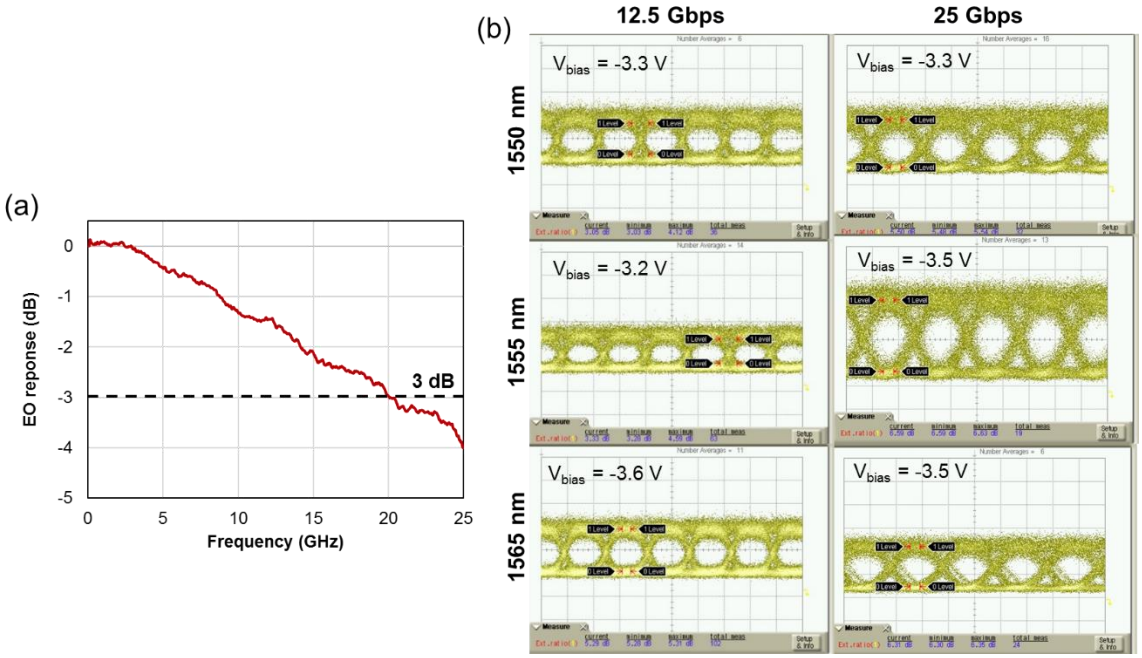

Figure 4-5. (a) EO response of heterogeneous EAM with 100 μm cavity and 3 μm mesa width at 1560 nm wavelength and 4 V reverse bias; (b) eye diagrams at 12.5 Gbps and 25 Gbps data transmission shown at different wavelengths.

4.1.3 Integrated transmitter with EA modulator

The co-design and 3-D integration of a photonic circuit with electrical driver circuit promise the solution for the next generation of low power optical transceiver [20-22]. This section the efforts to integrate the photonic circuit with heterogeneously integrated EAM array with CMOS drivers is introduced. The CMOS circuit, provided by Oracle labs [23], is designed and fabricated in 40 nm CMOS nodes [22]. The transceiver VLSI driver supports maximum a 12.5 Gbps data with up to 2.4 V bias swing. The size of VLSI circuit is about 4.5×5.2 mm^2.

The silicon photonic circuit is designed according to the driver circuit layout. As shown in *Figure 4-6*, the silicon PIC includes 1×16 heterogeneous 100 μm long EAM array with channel space fixed at 125 μm. 17×17 μm^2 bonding pads are used for flip-chip bonding, and also the metal contacts for the EAM array. In order to avoid damaging the III-V mesas, the Au bonding pads have large height up to 3.8 μm, deposited by an ebeam deposition tool.

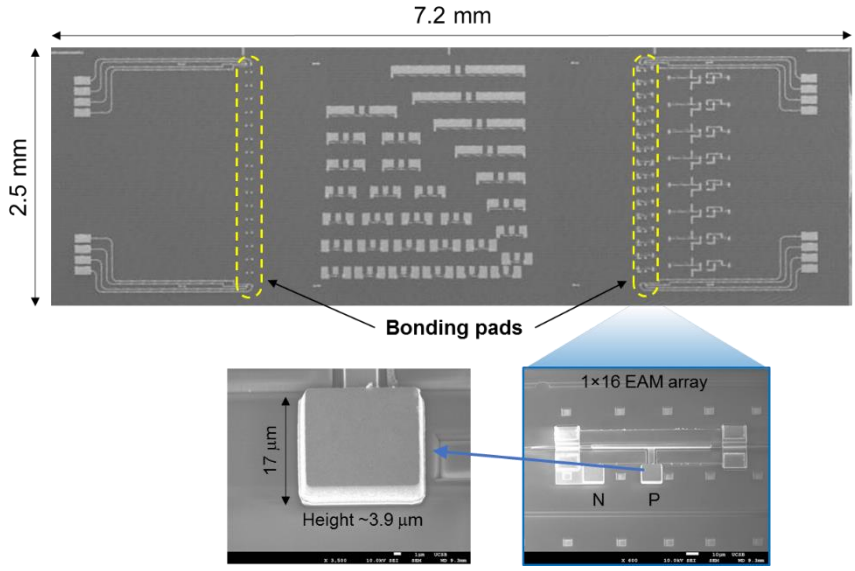

Figure 4-6. SEM image of PIC layout with heterogeneous EAM array with bonding pads.

The photonic circuit, with the top-view lateral-view and schematically shown in *Figure 4-7*(a) and (b), is integrated with the electrical driver circuit with a flip-chip bump bonding approach [24]. The microsolders on top of the metal pads, serve as both low resistance contact and adhesion layer between the metal bumps on both sides [24], as shown in *Figure 4-7*(c). The electrical driver circuit is then wire-bonded to a driving board which provides the DC voltage and PRBS signal for testing.

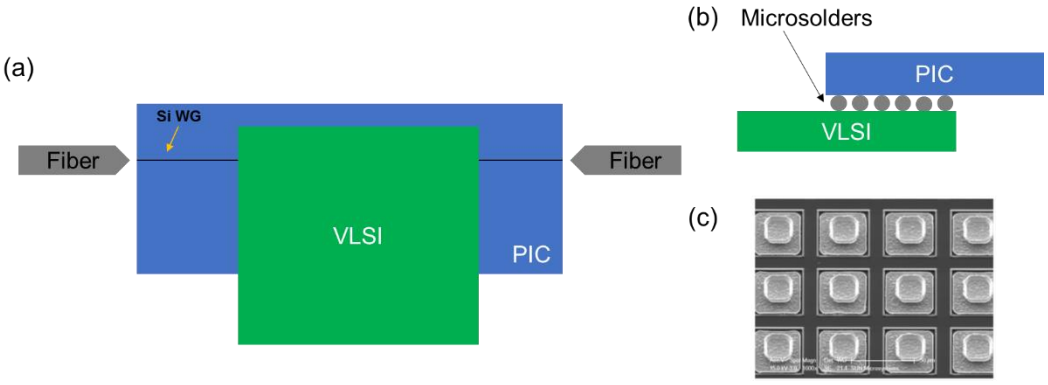

Figure 4-7. Schematics of (a) top view and (b) lateral view of the bump-bonding between photonic circuit and electrical circuit. (c) shows the SEM image of microsolders for the bump bonding [24].

The test setup of the photonic circuit after flip-chip bonding is shown in *Figure 4-8*(a). Because of the lack of on-chip lasers at this point, the testing is performed by an off-chip tunable laser through fiber couplings. After the EAM, the light is coupled back to fiber and input into DCA after a semiconductor optical amplifier (SOA) and tunable filter. Although the heterogeneous EAM with 100 μm cavity has shown a large extinction ratio up to 10 dB with 1 V bias, the current version of the CMOS driver only supports to 2.4 V reverse voltage, which is not enough to support a proper working point for the EAMs. Thus, reasonable extinction ratio is only achieved at wavelength below 1520 nm, as shown in *Figure 4-8*(b).

The experimental results have shown that heterogeneous EAM integrated with CMOS driver achieves an open eye at 12.5 Gbps with 3.5 dB extinction ratio at 1510 nm, with the maximum reverse voltage swing from 0 to 2.4 V, as shown in *Figure 4-8*(c). The asymmetric optical eye pattern was due to imbalance in the IC electric circuit delay-line. The high noise level was because 1) the high fiber coupling loss with an off-chip laser source, and 2) the limited drive voltage which required us to shift the

wavelength shorter to achieve larger dB/V and caused the total loss of photonics chip to increase.

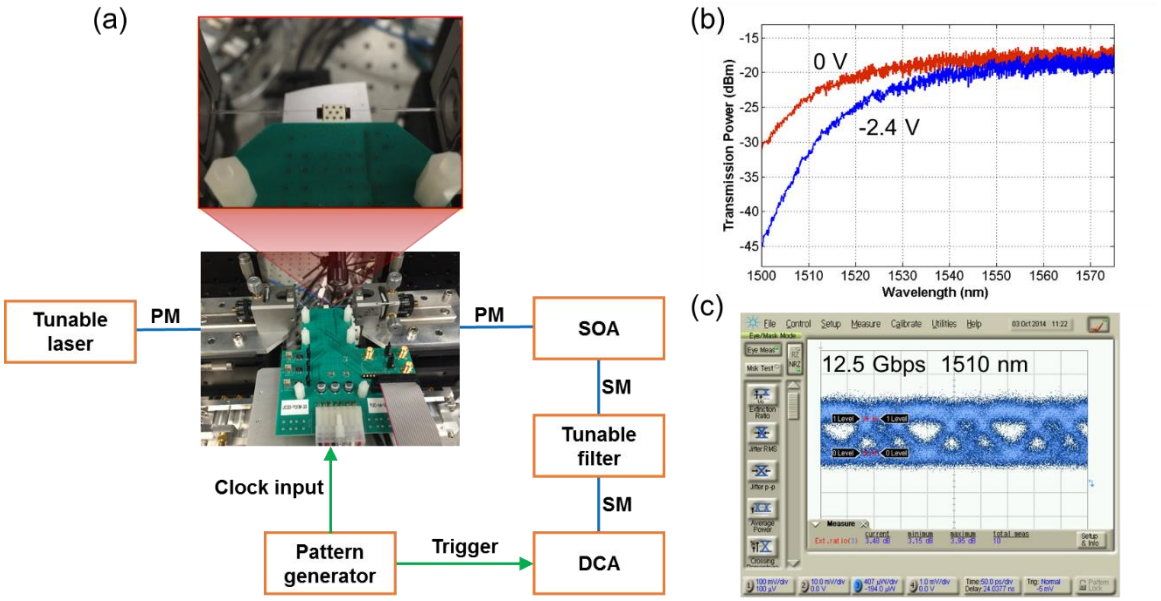

Figure 4-8. (a) testing setup of the EAM array integrated with CMOS driver; (b) transmission response of EAM channel with two reverse bias condition; (c) eye diagram at 12.5 Gbps operation with 1510 nm wavelength.

4.2 Ultra-linear heterogeneous modulator on Si

4.2.1 Introduction

A linear modulator is indispensable for radio frequency photonics or analog photonic link applications where high dynamic range is required. Commercial Lithium Niobate ($LiNbO_3$) MZM devices are widely used in such systems [25, 26], which are bulky and expensive, limiting addressable applications. Semiconductor based devices offer the chance to obtain highly linear performance together with small size, low cost, and the ability to integrate them with additional components to form photonic integrated circuit devices. High performance MZMs have been developed based on

GaAs [27] and InP [28], with the InP devices offering the opportunity to combine the MZM with other components (e.g. laser, photodetector) to develop photonics integrated circuits [29] for commonly used telecom bands.

The silicon photonics platform takes advantage of the tremendous investment and expertise in designing and fabricating devices on large Si wafers using standard CMOS foundry processes; enabling large scale integration with high repeatability, plus high volume manufacturing with low cost. A MZI modulator fabricated on a silicon photonics platform is therefore of great interest [3, 30]. Silicon MZMs, while significantly smaller than $LiNbO_3$ ones, are still relatively long for a semiconductor modulator due to low phase modulation efficiency [31], requiring either longer MZI lengths or higher modulation voltages. Additionally, and more importantly for analog systems, Si MZMs have shown significantly worse linearity than the $LiNbO_3$ MZMs used in RF photonics systems [32, 33], partially due to the inherent nonlinearity of the MZI transfer characteristic, but mostly due to the nonlinearity of silicon's electro-optic phase shift response. While a typical optical link using a $LiNbO_3$ MZM may have a spurious free dynamic range (SFDR) of up to 113 $dB \cdot Hz^{2/3}$ [34], much lower values have been found with Si MZM devices. Some improvement in the linearity of Si MZMs was achieved by using differential drive to reduce the non-linearity of the Si PN junction phase section, providing an SFDR of up to 97 $dB \cdot Hz^{2/3}$ at 1 GHz modulation frequency [35]. This is mainly because the index modulation in Si is achieved by a relatively weak mechanism; changes of carrier concentration, which is strongly nonlinear.

To overcome the nonlinearity from silicon based phase modulators, heterogeneous integration of materials with linear electro optic (EO) effect onto silicon was researched. Chen et al. reported the integration of LiNbO3, which has a strong linear Pockels effect. A silicon ring modulator with an adherently bonded LiNbO3 thin film achieved a SFDR of 98.1 $dB \cdot Hz^{2/3}$ at 1 GHz and 87.6 $dB \cdot Hz^{2/3}$ at 10 GHz [36]. Furthermore, linearization techniques can be used, typically some kind of electronic pre-distortion that increases the modulator complexity, power consumption and usually works only over limited bandwidth [37, 38]. A simple all-optical linearization technique, free of the above impediments, the ring assisted MZI (RAMZI) modulator was proposed in 2003 [39]. The RAMZI modulator uses the super-linearity of a ring phase modulator (with high coupling to the MZI arms) to balance the sub-linearity (sinusoidal transfer characteristic) of an MZI modulator. All-Si RAMZI modulators showed significant improvement over all-Si MZI modulators, demonstrating an SFDR of 106 $dB \cdot Hz^{2/3}$ at 1 GHz and 99 $dB \cdot Hz^{2/3}$ at 10 GHz [40]. However, because the index change of silicon has a third-order nonlinear term with the same negative sign as the inherent MZI nonlinearity, the combined negative nonlinearity is so high that canceling it with the opposite-signed nonlinearity of the ring is difficult, as relatively low coupling coefficients become necessary, causing an increase in the insertion loss and thus reducing SFDR. The all-Si RAMZI modulator still showed significantly lower linearity than a commercial $LiNbO_3$ modulator.

In this section, the linearity performance of silicon photonics based MZMs using heterogeneously integrated phase modulation sections fabricated from heterogeneous III-V multiple quantum-wells (MQW)/Si waveguides is investigated. The use of

heterogeneous III-V/Si phase modulation sections was chosen due to the lower nonlinearity of the III-V MQWs, together with the potential for higher optical power level operation, compared to Si based devices. In addition, we further improve the linearity of III-V/Si MZI modulators through the addition of ring phase modulators, using the RAMZI modulator design to linearize the MZI transfer characteristic. Two options for the RAMZI design are fabricated and tested, one with a weak-coupling to the rings, and one with a strong-coupling to the rings. In both cases, ultra-linear operation is achieved, higher than obtainable in the basic MZI design. Heterogeneous III-V/Si MZI and RAMZI modulator design, fabrication and characterization are discussed in detail in the following sections.

4.2.2 Device designs and fabrications

Unlike Si, the heterogeneously integrated III-V materials are not centro-symmetric and have a direct bandgap, therefore, in addition to the plasma and Kerr effects present in Si, they also exhibit a strong Pockels effect and quantum confined Stark effect [10, 11]. This provides extra degrees of freedom to achieve high linearity MZMs, and helps to increase the modulation efficiency (lower V_π plus provides for devices with larger bandwidth and a compact footprint. The refractive index in the heterogeneous waveguide changes as a function of the applied voltage as:

$$\Delta n(\lambda, f) = \sum_{m=1}^{4}\sum_{k=1}^{4} c_{mk}(\lambda) V^k \tag{4-1}$$

where m=1:4 refers to the mechanism of the index change, respectively plasma effect, band filling, QCSE and Pockels effect [10] and order k is truncated at 4 because it is the fourth order term that is responsible for the third order distortion. The applied

voltage consists of bias V_b and signal $V_s(t)$, hence the index change can be expanded near the bias point as:

$$\Delta n(\lambda, f) = \sum_{m=1}^{4}\sum_{k=1}^{3}\left[c_{mk} + (k+1)c_{m,k+1}V_b + \ldots\right]V_s^k(t) \tag{4-2}$$

The response of the MZI modulator biased at quadrature and operating in push-pull mode can be then written as,

$$P_s \sim \sin\left(\frac{2\pi\Delta nL}{\lambda}\right) \approx \frac{2\pi\Delta nL}{\lambda} - \frac{1}{6}\left(\frac{2\pi\Delta nL}{\lambda}\right)^3 \tag{4-3}$$

and substitution yields the third order distortion as,

$$P_s^{(3)} = \sum_{m=1}^{4}\left[\frac{2\pi L}{\lambda}\left(c_{m3} + 4c_{m4}V_b\right)^3\right]V_s^3(t) - \frac{1}{6}\left[\frac{2\pi L}{\lambda}\sum_{m=1}^{4}\left(c_{m1} + 2c_{m2}V_b + 3c_{m3}V_b^2 + 4c_{m4}V_b^3\right)\right]^3 V_s^3(t) \tag{4-4}$$

The coefficients c_{13}, c_{14} (plasma) and c_{23}, c_{24} (band filling) are negative, while the coefficients c_{33}, c_{34} (QCSE) are positive and large in absolute value [10]. In other words, the QCSE does not saturate with applied voltage, at least for reasonably small voltages. For the Pockels effect only the linear term c_{41} is non-zero. Since (with exception of the Pockels effect) coefficients are wavelength dependent, especially those associated with the QCSE, at one particular wavelength the positive third order distortion of the QCSE will compensate the negative distortions of band filling, plasma and the MZI itself.

To create a MZI modulator with an ultra-linear transfer characteristic, the extrinsic nonlinearity of the MZI, which transforms index modulation into modulation, should be balanced by the device design. When a standard heterogeneous MZI modulator is used, its extrinsic third-order nonlinearity is negative and rather large. To cancel it with the intrinsic nonlinearity of the index change would require operation at a wavelength close to the bandgap, which increases insertion loss causing the SFDR to suffer.

The operating principle of the RAMZI modulator has been described in previous publications [39, 40] under the assumption that the index modulation itself is perfectly linear, as is the case with the Pockels effect in $LiNbO_3$. In reality, the index modulation of the heterogeneous III-V/Si phase modulator is more complex as it involves inherently quadratic processes in the reverse biased P-I-N junction with band filling, QCSE, and, to a lesser extent the free carrier effect [41]. It is important to note that both band filling and the QCSE effects are by definition resonant phenomena and exhibit strong wavelength dependence. In the RAMZI modulator design, the total extrinsic nonlinearity of the MZI transfer characteristic is reduced, and the level of reduction is determined by the coupling coefficient κ. With the assumption that the phase section inside the ring changes linearly with bias, as κ is reduced from 1 to $\kappa_0 = 0.86$ the inherent negative nonlinearity of the MZI is reduced to 0, and for lower κ values this nonlinearity changes its sign becoming positive [39]. The RAMZI design therefore allows for the cancellation of the nonlinearity inherent in the MZI design, by judicious choice of coupling coefficients plus the use of phase modulation sections with zero, low and/or tunable nonlinearity. This compensation requires additional design complexity and a tuning process, but once the compensation is attained and the parameters assuring the highest SFDR are determined, the arrangement is proven to be quite robust, and, record-high SFDR can be repeatedly measured across modulator parameters and different operating wavelengths.

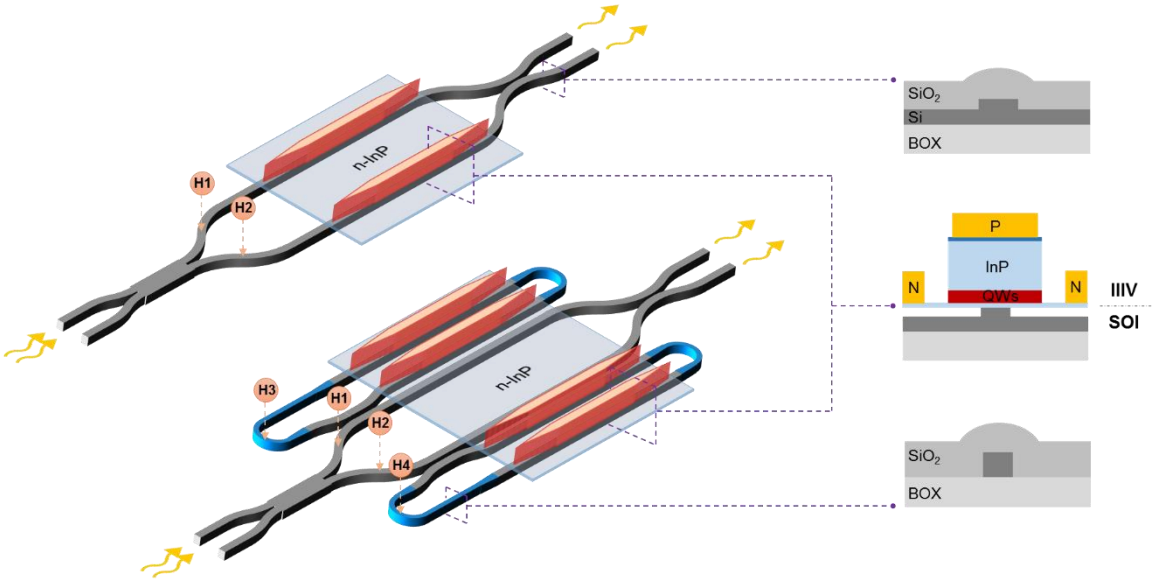

Figure 4-9. The schematic structure of heterogeneous MZI (top) and RAMZI (bottom) modulators on silicon, with varied color representing ridge/stripe/heterogeneous waveguide and their cross-sections. H1, H2 and H1-H4 indicate the thermal phase tuners in MZI and RAMZI, respectively.

The heterogeneous MZI and RAMZI modulators are shown schematically in *Figure 4-9*. The heterogeneous MZI modulator has balanced arms which include the III-V/Si phase sections. The symmetric interferometer is formed with 3-dB multimode interference (MMI) coupler and directional coupler as power splitter and combiner, respectively. H1 and H2 indicates the NiCr heaters that used within the arms of the MZI to thermally tune the operating point. Particularly, in the heterogeneous RAMZI, both arms of the MZI couple to a ring/racetrack resonator through a directional coupler with a specific coupling coefficient, κ. In each racetrack, the low loss silicon ridge waveguide adiabatically transits to two heterogeneous sections through a 50 μm long taper on one side, and on the other side transits to a fully etched nano-stripe waveguide, required for the tight bending radius of 15 μm.

Three types of waveguide, with cross-sections shown in *Figure 4-9*, form the total ring circumference. Both MZI arms and both rings have a separate heater for phase tuning (H1-H4), to control the device operation point. The two heterogeneous sections in each ring have a 250 μm long and 2.5 μm wide mesa. The silicon waveguide under the III-V mesa is 600 nm in width, to increase the optical mode confinement factor in the III-V MQW stack, which consists of 12 QWs with PL wavelength centered at 1360 nm. Two types of RAMZI modulator were fabricated: strong- and weak-coupled ring designs, with the as-fabricated coupling coefficients determined to be 0.79 and 0.55, representing the coupling coefficients to be 0.89 and 0.74, respectively. For both configurations, the cathodes of all active sections are connected as the bias port for push-pull operation [42].

Table 4-2. The epitaxial III-V layers

Layer composition	Doping level	Thickness (nm)
P-type contact ($In_{0.53}Ga_{0.47}As$)	Zn: 1.5×10^{19}	100
Band smoothing layer	Zn: 3×10^{18}	50
P-type cladding (InP)	Zn: 1.5×10^{18}->5×10^{17}	1500
SCH (InGaAsP 1.25Q)	Si: 1×10^{17}	100
12×QW ($In_{0.574}Al_{0.111}Ga_{0.315}As$)	Si: 1×10^{17}	8
13×Barrier ($In_{0.468}Al_{0.217}Ga_{0.315}As$)		5
SCH (InGaAsP 1.25Q)	Si: 3×10^{18}	50
N-type contact (InP)	Si: 3×10^{18}	110
Supper lattices	Si: 3×10^{18}	40

The fabrication of heterogeneous MZI and RAMZI devices is similar to that of the EAM circuit, as shown in *Figure 4-3*, except the silicon process step. The lithographic step for silicon layer is performed with a 248-nm DUV stepper, in order to define the high-resolution silicon waveguide with 600 nm width and carefully tune passive components such as directional coupler and MMI. The Si waveguide was etched with SF_6/C_4F_8 plasma, providing a propagation loss of 1.6±0.3 dB/cm for the 600-nm

waveguide width. A Ni/Cr heater layer with total thickness of about 100 nm was deposited on top of the Si waveguide with 1 μm SiO_2 spacer layer. The silicon waveguide is flared out to 5 μm with an 8-degree angle to reduce the facet reflection.

The bonded III-V layer stack includes an active region with 15 InAlGaAs QWs with a PL wavelength centered at 1360 nm; the details shown in *Table* 4-2. The QWs were slightly n-doped to improve the high-speed performance [10]. The doping level in the p-InGaAs layer was raised by 50% compared with a previously used, to lower the p-contact resistance, which normally dominates the series resistance of devices with a narrow p-mesa. In order to optimize the modulator efficiency, the III-V phase modulation sections were aligned parallel to the [011] crystalline orientation, so that the Pockels effect adds constructively to the other index changes. A high transverse electric (TE) optical mode confinement of 26.9% in the MQWs was achieved with a 600-nm wide Si WG and a 2.5 μm mesa, as shown in the cross-sectional plot in *Figure 4-10*(a). *Figure 4-10*(b) and (c) shows SEM images of the III-V mesa with a 50 μm long taper between this heterogeneous section and the Si waveguide. The taper tip width is smaller than 200 nm, providing low coupling loss between the Si waveguide and the heterogeneous section.

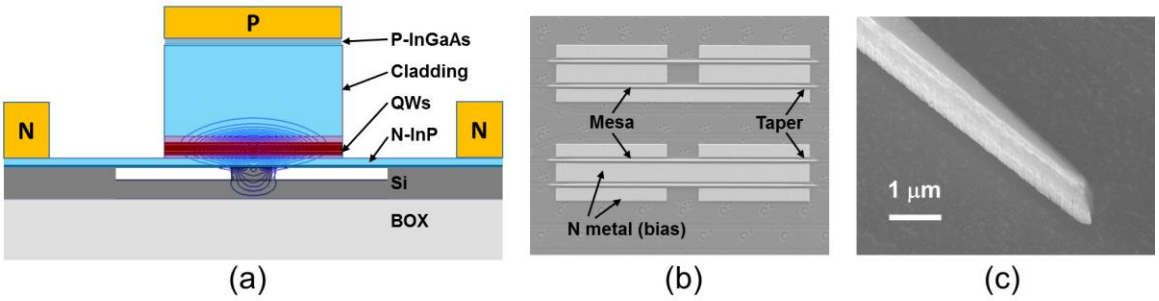

Figure 4-10. (a) The cross-section of the devices with intensity contour of fundamental TE mode; (b) top view SEM image of III-V sections; (c) SEM image of taper tip from angled view.

4.2.3 Linearized heterogeneous MZI modulator

The processed heterogeneous MZI modulator chips with polished facets were placed on a thermal heat sink which was temperature controlled at 25 ˚C for testing. A single drive push-pull electrical configuration was utilized in the devices for ease of modulation [3], requiring only one RF drive signal, and to take advantage of the reduced capacitance of that approach. A tunable laser source with TE polarization and polarization maintaining (PM) fiber output was coupled into the Si waveguide using a PM lensed fiber. The output of the heterogeneous MZI modulator was coupled into a fiber using a fiber lens, and for SFDR measurements was amplified by an Er-Doped Fiber Amplifier (EDFA) and coupled into a photo detector (PD), as shown in *Figure 4-11*. The input and output waveguides were angled to reduce optical reflections; however, the tapered design produces relatively high coupling loss (about 9 dB per facet) although with relatively easy alignment. Future devices will incorporate an inverse taper design [43] to provide much lower coupling loss, as required for a discrete modulator device.

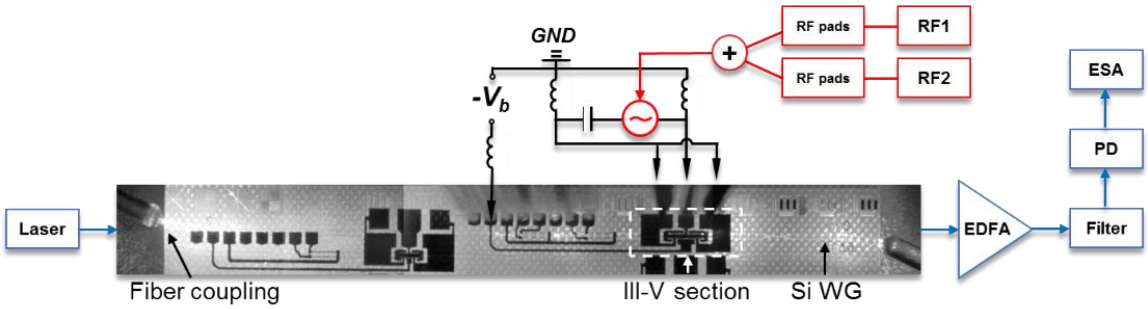

Figure 4-11. NIR image of an MZM device, and setup for SFDR measurement

DC measurements were taken under computer control to characterize single drive push-pull operation of the devices at multiple wavelengths. *Figure 4-12*(a) shows

measurements of the output versus the differential voltage between the two phase modulation sections, for a device with a short (100 μm) phase modulation section length, and for different input optical wavelengths of 1550 nm, 1500 nm and 1460 nm. Much higher modulation efficiency (lower V_π) is seen at the shorter wavelength, closer to the band-edge off the phase modulator epi material. The device is biased near quadrature for all the transfer characteristics shown in *Figure 4-12*(a). The $V_\pi \cdot L$ of the device can be fit from this measured data, which is a minimum of 1.5 V·mm at 1460 nm, and larger at longer wavelength. The actual V_π is higher in this particular device due to its short length. The larger V_π compared with previous results on similar heterogeneously integrated MZI modulators [10], probably results from a reduction of mode confinement in the QWs of a narrower III-V mesa, from undercut of the QWs layers in the wet-etch step, or the voltage drop on a higher series resistance due to the narrower mesa.

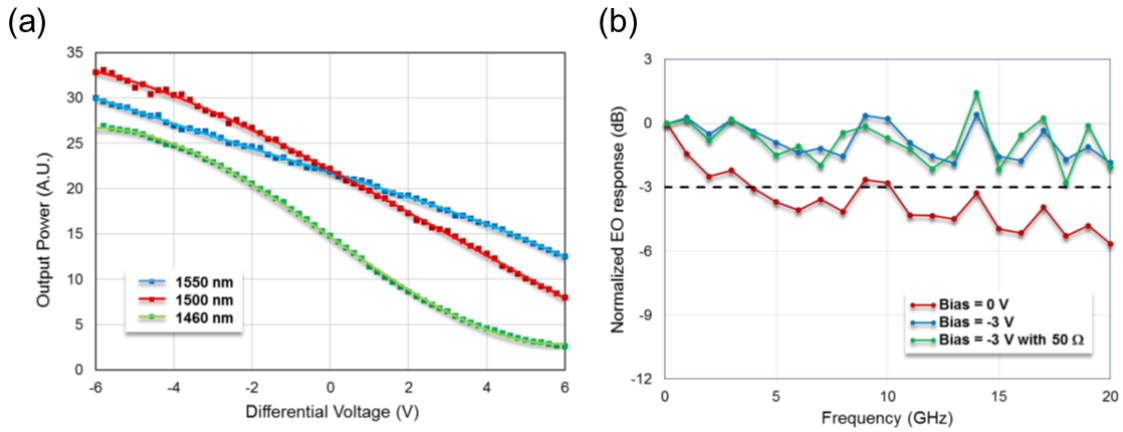

Figure 4-12. (a) Transmission measurement of heterogeneous MZI modulator with 100 μm phase section at multiple input laser wavelengths; (b) Measured Frequency Response for heterogeneous MZI modulator with 100 μm phase section.

The apparent linearity of the DC characteristics may change with wavelength, indicating a delicate interplay of the different phase modulation mechanisms described above, however, this is difficult to quantify from DC measurements alone. The third order nonlinearity, i.e. the third order term in the series expansion, of the sinusoidal-like response of the MZI is negative. Also negative are the third order terms in the series expansion of the plasma-like effect of free carriers and the state-blocking phase change effect. At the same time, the phase characteristics of the QCSE have a positive third order term, and a strong wavelength dependence. The fourth phase modulation mechanism, the Pockels effect, is largely linear. Thus, at some wavelength and modulator bias the positive nonlinearity of the QCSE phase response could become sufficient to cancel the negative nonlinearities of the plasma and state blocking effects, and potentially also the nonlinearity of the MZI itself. By choosing the optimum bias point this high linearity wavelength can be shifted towards the desired value of 1550nm, however, complete optimization, and therefore linearization of the response, may require an MQW design with a longer PL wavelength than used in these devices.

Frequency response measurements of the 100 μm device, demonstrating a bandwidth of over 20 GHz, are shown in *Figure 4-12*(b). Terminating the device with a 50 Ohm load shows little improvement in device bandwidth (up to 20 GHz), while reducing the efficiency by 3 dB compared to no matching load. Biasing the device at 0 V shows an increase in low frequency response, likely due to the small swing to positive bias from the sinusoidal input.

To assess linearity, measurements of the SFDR of this same device were carried out at a wavelength of 1550 nm, and a modulation frequency of 10 GHz. An EDFA was used

to overcome the loss of the two fiber couplings (18 dB), plus provide sufficient optical power at the PD to support high SFDR operation. The requirement to use an EDFA limited the wavelength range over which SFDR could be measured, limiting the possibility to further improve the performance by increasing the QCSE. As shown in *Figure 4-11*, two RF tones were combined using a power combiner and RF pads and applied to the device. The separation between two tones was set to 10 MHz, so the two signals were at 995 MHz and 1005 MHz for 1 GHz center wavelength. The generated third order intermodulation distortion signal were at 985 MHz and 1015 MHz, respectively. The fundamental and third order intermodulation products were measured on a high performance electrical spectrum analyzer.

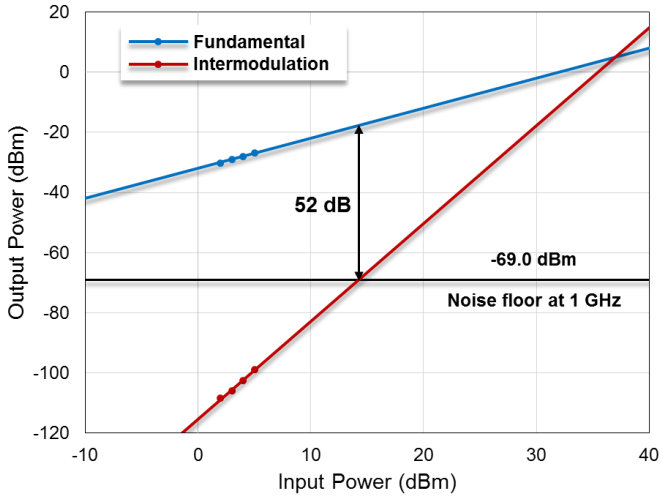

Figure 4-13. Measured SFDR for heterogeneous MZI modulator with 100 µm phase section. 52 dB for 1 GHz Bandwidth, or 112 dB·Hz$^{2/3}$

The SFDR was measured versus variations in the input optical power level to the MZM, modulator p-n junction dc bias voltage, and for different photodetector currents. A series of SFDR traces were taken, with the highest SFDR occurring for the highest optical input power level (+18 dBm laser output) and highest photocurrent (15.6 mA),

for a DC bias voltage of -2 V. The measured response in *Figure 4-13* shows the highest SFDR; in this case the plot has an SFDR of 52 dB for 1 GHz bandwidth, or an SFDR of 112 dB·$Hz^{2/3}$.

4.2.4 Linearized heterogeneous RAMZI modulator

The same approaches were used to test the heterogeneous RAMZI modulators: GSG probe provides the modulation signal for the device, modulating two straight sections of each ring in a push-pull configuration, with the n contact providing the DC bias level, as shown in *Figure 4-14*. Thermal tuners H1 and H2 are used to tune the MZI phase and set the bias point of the MZI, e.g. at quadrature. Thermal tuners H3 and H4 are used to tune the resonance frequencies of the two rings. A tunable laser was used to characterize the device. High laser output power, 15 or 18 dBm, was coupled into the on-chip modulator, however, due to the high coupling loss between the silicon waveguide and lensed fiber, which was ~ 9 dB per facet, a lower power level was present within the RAMZI modulator. Alternatively, an amplified spontaneous emission (ASE) source was used to monitor the transmission spectrum through the modulator.

The insertion loss of the strong-coupled RAMZI modulator itself (removing the coupling loss of the two fiber to waveguide couplings) was 9 dB, compared to 3.7 dB for the short (100 μm) MZI device, which had only 0.7 dB excess loss as the modulator bias was set to quadrature. This additional loss in the RAMZI is from absorption in the longer active sections, plus the optical loss from the four tapered mode convertors and the passive silicon waveguides; a much lower loss could be achieved in an optimized III-V/Si ring structure. Additional insertion loss is present when varying the bias

conditions of the rings. Figure 4-15 shows the effect of changing each phase tuner in the RAMZI modulator with strong-coupled rings (κ = 0.79). *Figure 4-15*(a) and (b) show the effects of MZI phase heaters H1 and H2 respectively. At zero voltage, the black traces in both figures show the unbiased device spectra, with the ring 'dips' clear; the device should be biased near the high point between these dips. Increasing bias voltage in H1 moves the MZI phase in one direction, while in H2, it moves it in the other direction. Increasing the bias voltage in H1, as shown in *Figure 4-15*(a), initially reduces the output power to its minimum level, and then it increases. Increasing the bias voltage in H2, as shown in *Figure 4-15*(b), provides a more symmetrical spectrum for small voltages, a value of 1 V providing also a reasonable output power.

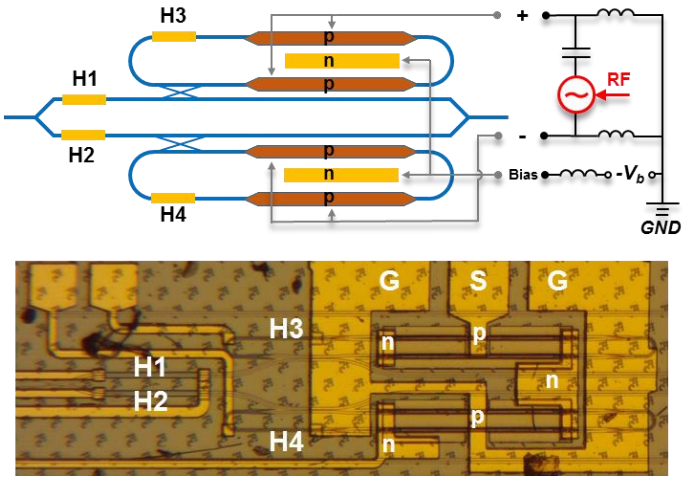

Figure 4-14. Heterogeneous RAMZI modulator with push-pull differential configurations and its microscope image.

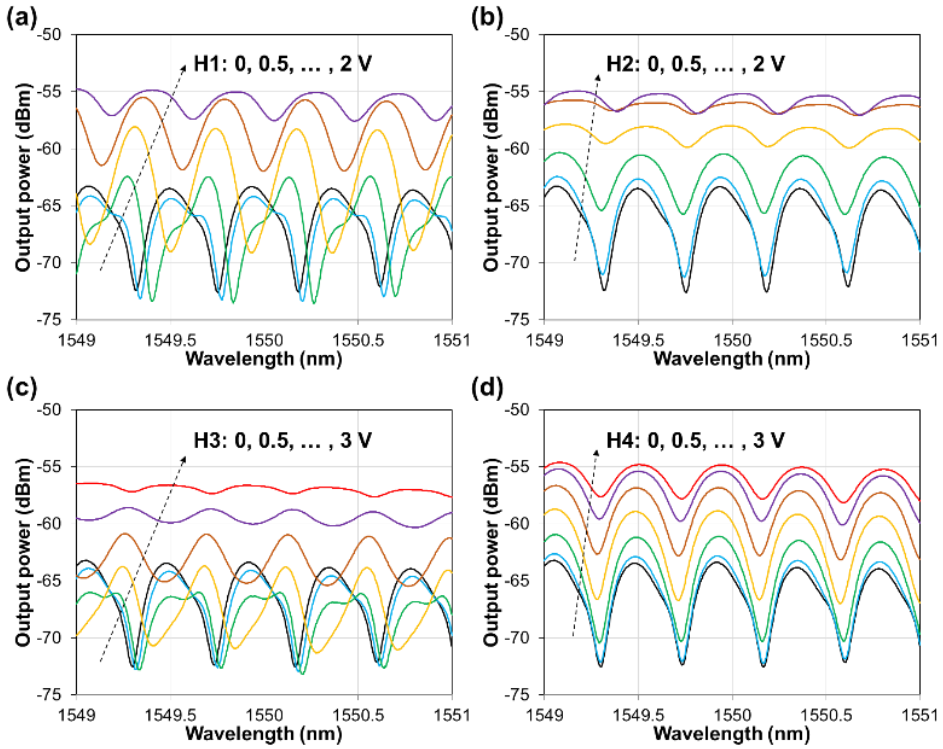

Figure 4-15. Transmission spectrum of the heterogeneous RAMZI modulator with strong-coupled rings with ASE input. (a) (b) (c) (d) show the operation point change by applying voltage on the thermal tuners H1-H4, respectively, with all other tuners unbiased.

Figure 4-15(c) and (d) show spectra changes from tuning the ring resonance heaters H3 and H4. Similar changes are seen in these spectra as for tuning the MZI phase, indicating that the heaters have thermal crosstalk and that in these devices all heaters affect both MZI phase and Ring Resonance frequency. From *Figure 4-15* the ring resonance frequencies tune a relatively small amount, much less than one free spectral range (FSR), while the MZI phase is more effectively tuned. This should be taken into account when looking at SFDR results for various heater values, e.g. H2 and H4 having a somewhat similar bias effect on the device.

The modulator linearity was characterized through measurements of SFDR at 1550 nm, for a modulation frequency of 10 GHz. The tunable laser was set at a wavelength

midway between a pair of dips in the optical spectrum. The modulator output is amplified in an erbium-doped fiber amplifier (EDFA) to overcome the large coupling losses of the device, followed by a narrow filter to reduce the ASE added by the EDFA. The modulator's SFDR was measured at different phase modulator bias voltages and heater voltages. By carefully tuning the thermal phase tuners H1-H4 and the modulator bias voltage, the highest SFDR for the RAMZI with strong-coupled rings was achieved for a modulator bias of -3 V and for H4 = 1.2 V, as shown in *Figure 4-16*; the measurement includes the fundamental, third order intermodulation products, and noise level for 1 GHz bandwidth (-69 dBm), providing an SFDR of 57 dB for 1 GHz bandwidth, equivalently an SFDR of 117 dB·Hz$^{2/3}$. This is a 5-dB improvement in SFDR compared to a commercial $LiNbO_3$ modulator measured on the same setup. With this strong-coupled device, this high value of SFDR was achieved at the lowest modulator loss, ~ 9 dB.

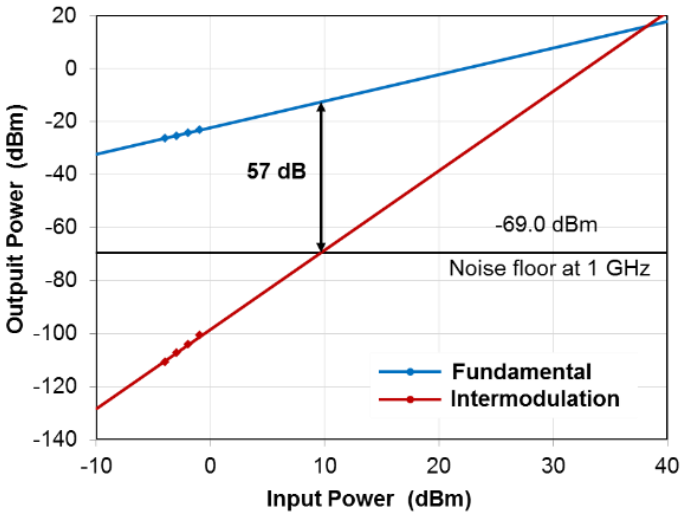

Figure 4-16. Measured SFDR of heterogeneous RAMZI modulator with strong-coupled rings: 57 dB for 1 GHz Bandwidth, or 117 dB·Hz$^{2/3}$.

Figure 4-17(a) and (b) shows a series of SFDR measurements for the strong-coupled RAMZI modulator as the MZI phase heaters and ring heaters were varied. The SFDR is very high near zero bias, over 115 dB·Hz$^{2/3}$. Varying the MZI phase heaters, H1 and H2 (with H3 and H4 =0V), a small maximum is found for H2 = 1 V, providing an SFDR of 116 dB·Hz$^{2/3}$. Varying the ring heaters, H3 and H4 (with H3 and H4 =0V), the maximum SFDR value of 117 dB·Hz$^{2/3}$ is seen for several H4 values of 1.2 V, 1.3 V and 1.4 V. *Figure 4-17*(c) shows a series of measured SFDR values versus the modulator DC bias level, for laser input powers of 15 dBm and 18 dBm. At the lower laser power level of 15 dBm, the SFDR peaks near a bias of -2.5 V, whereas at the higher laser power of 18 dBm the SFDR peak moves down to -3 V. Both the SFDR and the modulator output power P_{out}, i.e. the internal power before output fiber coupling, vary as the input laser wavelength is varied over more than a full FSR of the ring spectrum, as shown in *Figure 4-17*(d). The central point with an SFDR peaked just above 116 dB·Hz$^{2/3}$ shows the wavelength where all other measurements were taken, i.e. centered between two dips of the transmission spectrum. In this figure heater H2 was set to 1 V while the other heaters were 0 V.

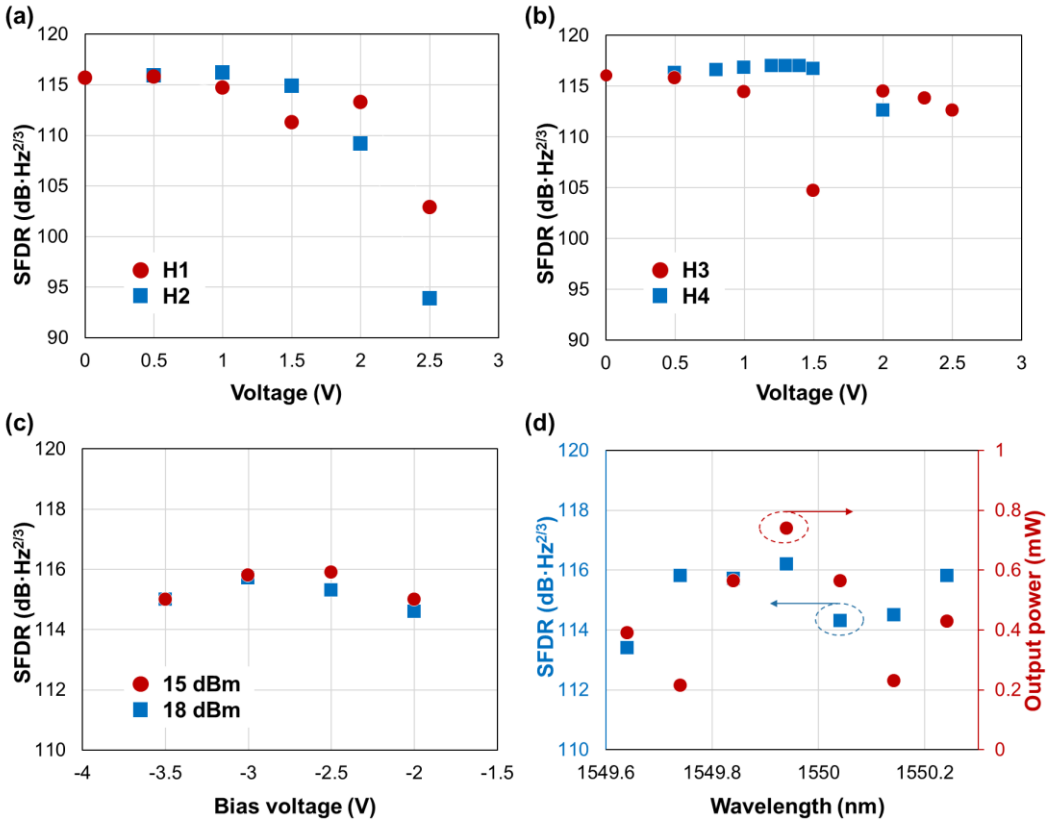

Figure 4-17. SFDR measurements of strong-coupled heterogeneous RAMZI modulator for (a) changing the voltage in one of the heater H1 or H2 (with all others = 0 V); modulator bias = -3 V, input power = 18 dBm; (b) changing the voltage in one of the heater H3 or H4 (with all others = 0 V); modulator bias = -3 V, input power = 18 dBm; (c) changing modulator bias voltage with input power of 15 and 18 dBm, with the voltage in H1=H2=H3=H4=0 V; and (d) changing laser wavelength with corresponding output power, with the voltage in heaters H1=H3=H4=0 V, H2=1 V and input power = 18 dBm.

A high SFDR value is found versus wavelength across a full FSR from the rings in the RAMZI structure. From a peak value at the center wavelength (1549.941 nm) of 116.2 dB·Hz$^{2/3}$, it drops to a worst-case value of 113.4 dB·Hz$^{2/3}$, still higher than the best result from an MZI style modulator, either a heterogeneous MZI or a standard LiNbO3 MZI modulator. This indicates that the device could be operated at any wavelength and still provide an SFDR of larger than 113 dB·Hz$^{2/3}$, whereas centering the wavelength within the ring FSR provides the highest SFDR. Additionally, the

highest SFDR occurs at the condition with the highest modulator output power Pout; in this case Pout is estimated to be 0.74 mW. The output power Pout varies more versus wavelength than the SFDR, due to the dips in the optical transmission spectra of the device, with much lower output power when aligned with these dips.

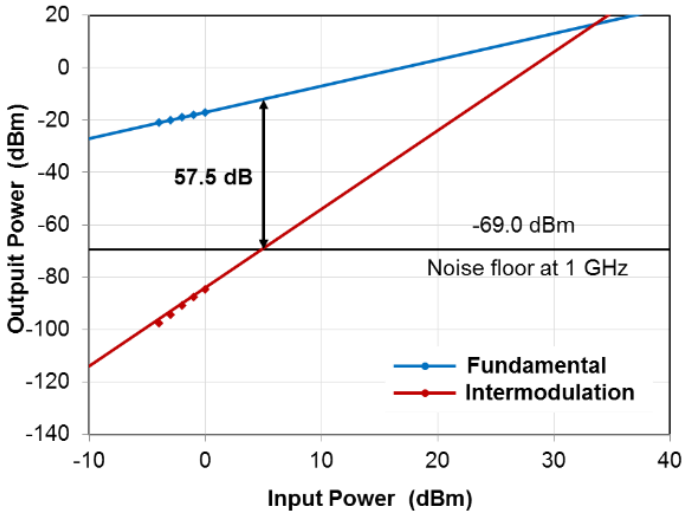

Figure 4-18. Measured SFDR of heterogeneous RAMZI modulator with weak-coupled ring design: 57.5 dB for 1 GHz Bandwidth, or 117.5 dB·Hz$^{2/3}$.

The RAMZI modulator with weak-coupled rings also shows high linearity. The measurement in *Figure 4-18* shows an SFDR of 57.5 dB for 1 GHz bandwidth, or 117.5 dB·Hz$^{2/3}$, which is the record high linearity achieved from a silicon based modulator. However, this was achieved in a high insertion loss regime, with only 0.07 mW Pout (an insertion loss of 20 dB), making this result less practical than the similar SFDR with higher power from the strong-coupled RAMZI modulator.

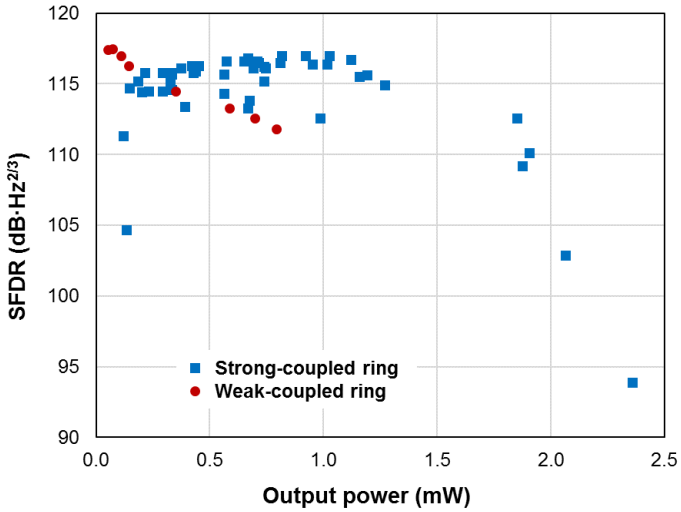

Figure 4-19. SFDR measurement of heterogeneous RAMZI modulators with strong- and weak-coupled rings versus modulator output power. The laser input power and the DC bias voltage of the modulator were fixed at 18 dBm and -2.5 V, respectively.

Figure 4-19 compares all the SFDR measurements taken for the devices with strong- and weak-coupled rings using the same laser input power of 18 dBm and the same modulator bias of -2.5V, with various heater bias conditions. A clear trend between SFDR and output power can be seen for each device. For the weak-coupled RAMZI modulator higher linearity is achieved at low output power. By comparison, the strong-coupled RAMZI has high SFDR over a wide range of power output, with the peak value occurring at an output of about 1 mW. This provides 11 dB of difference in modulator insertion loss between the two designs when operated near maximum SFDR. The fast fall of SFDR with output power and high insertion loss makes the weak-coupled RAMZI less practical, as it requires significant optical gain to achieve the high linearity. Conversely, the strong-coupled RAMZI modulator provided very high SFDR, over 116 dB·Hz$^{2/3}$ over a very wide range of operating parameters and output powers.

Figure 4-20 compares major results of recent works on the linearity of modulators fabricated on a Si, CMOS compatible platform. Both the heterogeneous MZI and RAMZI modulators surpass the previous record for a linearized modulator on Si, obtained using the all-Si RAMZI modulator design [40]. It is significantly higher than any Si MZM result. This result demonstrates that heterogeneously integrated III-V/Si modulators, using wafer bonded III-V material for phase modulation sections, can produce performance similar to $LiNbO_3$ devices, eliminating the nonlinearity added by using Si phase modulators, and provides an ultra-linear integrated modulator for the silicon photonics platform, supporting high dynamic range analog optical systems, and integration with other components to form complex RF Photonic PICs.

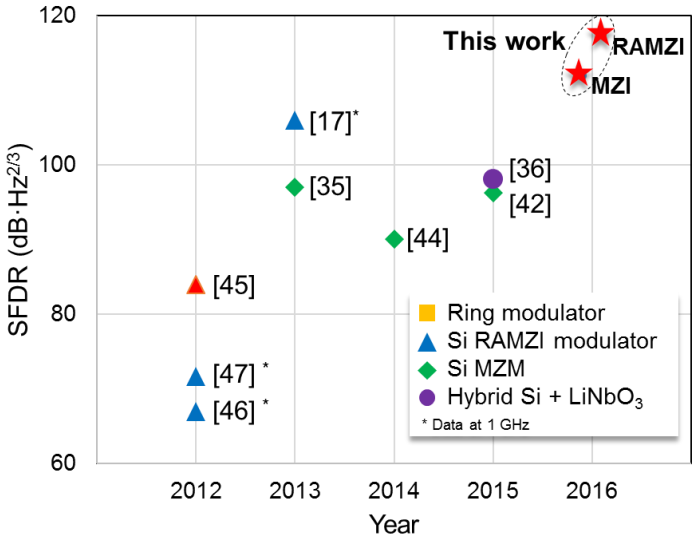

Figure 4-20. Comparison of modulators on Si: SFDR representing the degree of linearity.

4.3 Summary

In this chapter, two types of silicon based heterogeneous modulators are demonstrated. First, III-V/Si EAMs with a compact lump electrode are developed, showing low power and high speed operation in C-band. Short cavity EAM on silicon shows high extinction ratio with only 1 V bias swing for a wavelength range larger than 15 nm, which is important for a WDM data transmission system. In addition, the heterogeneous EAM circuit is successfully integrated with CMOS driver circuit with high yield, achieving 12.5 Gbps operation with limited voltage bias from the driving board. Those results strongly support that heterogeneous EAM is suitable for scalable optical interconnecting solutions.

Second, we have shown the advantages of heterogeneous integration on the highly linear modulator designs. High SFDR of up to 112 $dB \cdot Hz^{2/3}$ at a 10 GHz modulation frequency is achieved in a heterogeneously integrated MZI modulator, by using low nonlinearity III-V MQWs phase modulation sections to minimize nonlinear effects of the device and leaving only the nonlinearity of MZI itself. The heterogeneously integrated III-V/Si RAMZI modulator further improves the linearity, achieving a maximum SFDR of 117 $dB \cdot Hz^{2/3}$ for the strong-coupled design, and 117.5 $dB \cdot Hz^{2/3}$ for weak-coupled design. The strong-coupled heterogeneous RAMZI device provided much lower loss at the optimum SFDR bias, and therefore is the most practical for use in system applications. Compared to the standard heterogeneous MZI, the coupled-ring resonant structures of the RAMZI design provide extra tuning degrees of freedom. The positive nonlinearity of the ring phase characteristics is used to efficiently compensate the negative nonlinearity of the MZI transfer response. The RAMZI design achieves

SFDR results better than can be achieved with a heterogeneous MZI modulator or a commercial $LiNbO_3$ MZI modulator. This heterogeneous MZI and RAMZI modulator provides an ultra-linear integrated modulator for the silicon photonics platform, supporting high dynamic range analog optical systems, and integration with other components to form complex RF Photonic PICs.

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Chapter 5

Heterogeneously integrated transceiver circuits

For a realistic intra-chip and inter-chip optics link, the bandwidth density and total power consumption are major challenges. Consequently, full integration of all photonics components on chip with high-speed modulators and photodetectors, and especially lasers, is highly desired for scalable and energy efficient system topology designs. Particularly, an on-chip integrated laser source is required for flexible system design and the future low cost photonic packages [1, 2]. As discussed in previous chapters, a library of functional devices has been developed on silicon with the heterogeneous integration method, including ultralow loss waveguides, arrayed waveguide grating (AWG) routers, low threshold DFB lasers, high speed EAM, semiconductor optical amplifiers (SOA) and photodetectors (PD) on silicon [2-5], enabling a large scale photonic integration implementations.

5.1 Photonic network on chip

A typical on-off keying photonic transceiver is shown in *Figure 5-1*. This includes a high power, low noise laser with high efficiency and low threshold current; a high speed intensity modulator to convert the electrical radio frequency (RF) signal into

optical signal; a low loss optical link through waveguide or optical fiber guiding; low loss and low cross-talk multiplexer and demultiplexer in a multiplexing system; a high speed and low cross talk optical routing system and a high speed, low dark current photodetector to convert the optical signal back to an electrical RF signal at the receiver.

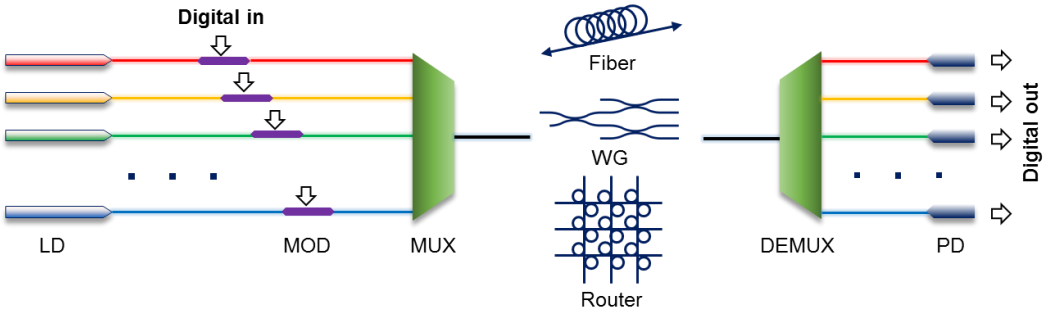


Figure 5-1. Diagram of a typical WDM optical communication system.

There are varied types of NoC network topologies based on specific applications depending on the specific application and technique solution on each type of components [6-8]. In this work, an integrated ring-type WDM network PIC is proposed and demonstrated for the first time. A schematic of the photonic circuit is shown in Figure 1-2. The NoC circuit consists of a reconfigurable ring-bus network and eight WDM transceiver nodes, with high speed transmitter and receivers in each node. All transceiver nodes connect to the circular bus waveguide through broadband optical switches. Extra ports are linked to waveguide edge-couplers for off-chip fiber coupling.

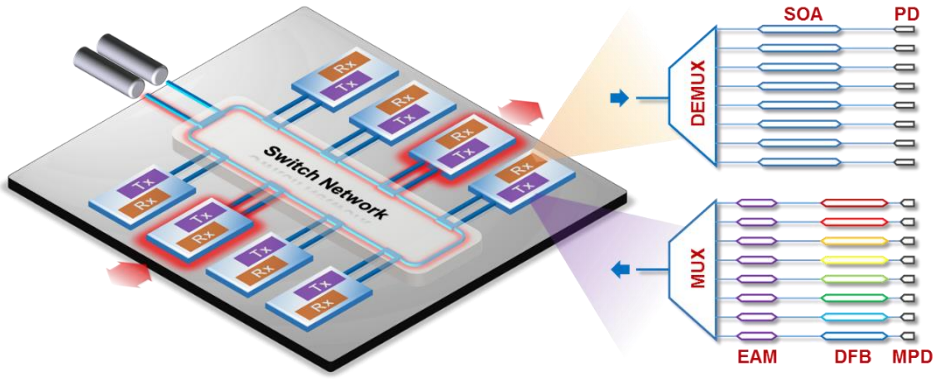


Figure 5-2. Diagram of the NoC circuit architecture

The ring-bus architecture defines a reconfigurable network on chip. *Figure 5-3* illustrates three major working modes. At default mode when a node with its optical switch normally-off, the corresponding transmitter only talks to its local receiver for self-configuration. When two of the switches are at on status, the eight-channel signal from one transmitter are routed to the WDM receiver at another node, or to optical fiber coupling for off-chip communication. It can be also defined to be a 1×N broadcasting network with one transmitter and N receivers by partially turning on the switches. This reconfigurable network architecture provides great flexibility on the system design for chip level optical interconnects.

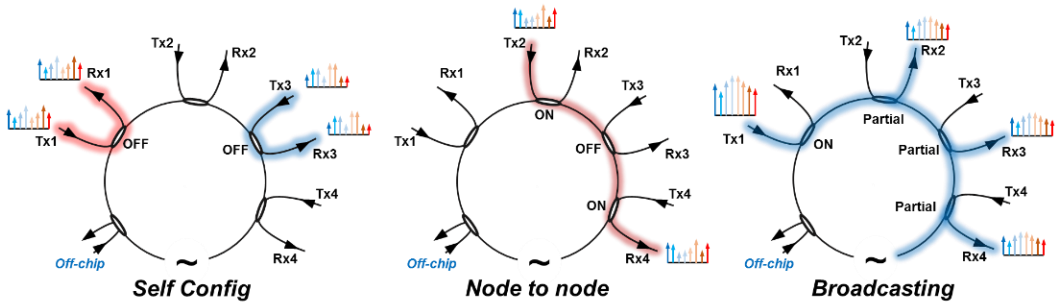


Figure 5-3. Reconfiguration modes of ring network.

It is worth to noting that, all the transceiver nodes share identical WDM channels, thus traffic conflicts may happen when multiple nodes upload signal at same channel,

which should be well managed by control circuits. On the other hand, the broad band switch turns on and off all WDM channels simultaneously, without selectively picking one of the channels. As an extension of this design, narrow band switch e.g. tunable ring switches can be used to route each single channel separately to expand the amount of the transceiver nodes.

A key part of designing optical networks involves analyzing propagating loss and optical power budgets. The power budget and margin of an optical link is given by:

$$Power\ budget\ [dB] = P_{Tx}[dBm] - P_{Rx}[dBm] \quad (5\text{-}1)$$

$$Power\ margin\ [dB] = Power\ budget\ [dB] - \sum \alpha_i\ [dB] \quad (5\text{-}2)$$

Where α_i is the loss of all the components, including waveguide or fiber propagation loss, and coupling loss. *Table 5-1* lists typical values of part of the components used in the link. For the intra-chip interconnects, the waveguide length between Tx and Rx is normally short due to the chip footprint, so the total waveguide propagation loss is not a major part. The total loss is normally dominated by the insertion loss of on-chip components such as modulator and (de)multiplexer. For inter-chip link, extra loss comes from the light coupling between fiber and waveguide on PIC. Power budget over 20 dB is required with the high total loss on each data channel.

Table 5-1. Loss analysis of optical link on chip

	Intra-chip	**Inter-chip**
Modulator	4 dB	4 dB
WG loss	1-2 dB/cm	0.5 dB/km
Coupling loss	--	1-5 dB/coupling
Mux (with channel nonuniformity)	3-6 dB	3-6 dB
DeMux (with channel nonuniformity)	3-6 dB	3-6 dB
Total loss	~16 dB	~18 dB

5.2 Circuit design and process

In each transceiver node, as shown in the *Figure 5-4*, the WDM transmitter has 8 wavelength channels with 200 GHz channel spacing in the C/L band. A single mode DFB laser provides the CW light source and a high-speed EAM is used for intensity modulation. Monitoring PDs (MPDs) at the backside of the lasers are used to *in-situ* monitor the laser output power, and provide feedback control. At the receiver side, each corresponding WDM channel has high speed waveguide photodetectors (PD). P-I-N type InGaAs PD is used in this design. On some of the channels, a semiconductor optical amplifier (SOA) is also integrated, acting as booster for compensating the extra coupling loss from off-chip communications.

Symmetric multiplexer and demultiplexer (Mux/DeMux) design of the chip is fulfilled using a 1×8 silicon array waveguide grating (AWG). The upstream and downstream of each transceiver node is through a Mach-Zehnder interferometer (MZI) switch to the bus waveguide. The switch controls 1.6 THz (8×200 GHz) broad optical bandwidth. Cascaded 3-dB adiabatic couplers (ACs) are used in the switch array. Thermal tuning with metal heater pads in the MZI arm is to route the signal among the transceiver nodes.

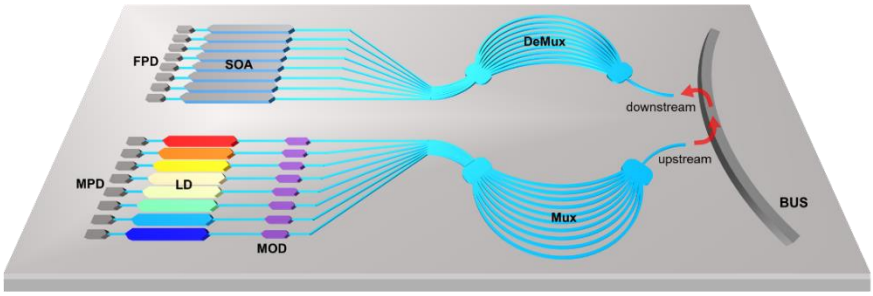
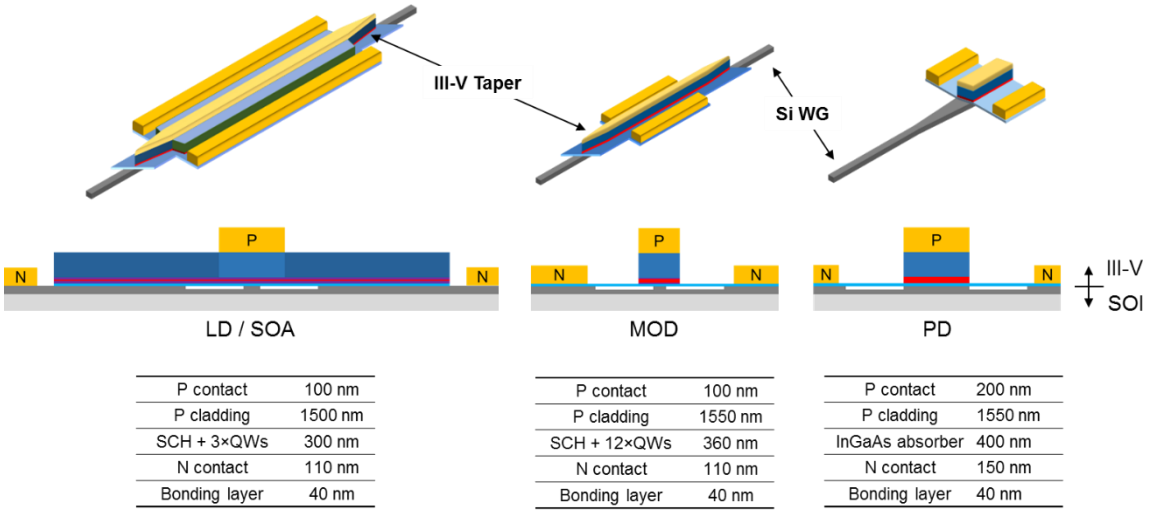


Figure 5-4. Diagram of transceiver node, including 8 channel WDM transmitter and receiver.

The four types of active devices: laser, modulator, photodetector and amplifier are heterogeneously integrated on the photonic circuit. The III-V epi stack and bandgap of gain materials for them are designed to optimize their performance individually. As shown in *Figure 5-5*, the laser and SOA have the same epi and device structure, with H^+ implanted wide mesa; the EAM has a single mode ridge mesa to depress the parasitic capacitance; the PD has a bulk InGaAs layer at active region instead of QWs, with wide mesa and multimode waveguide for high responsivity and high speed. A short (20 μm) taper is used to couple the light between silicon and III-V/Si waveguide in the laser/amplifier, while the long (60 μm) taper for EAM.



P contact	100 nm
P cladding	1500 nm
SCH + 3×QWs	300 nm
N contact	110 nm
Bonding layer	40 nm

P contact	100 nm
P cladding	1550 nm
SCH + 12×QWs	360 nm
N contact	110 nm
Bonding layer	40 nm

P contact	200 nm
P cladding	1550 nm
InGaAs absorber	400 nm
N contact	150 nm
Bonding layer	40 nm

Figure 5-5. Device structure, cross-sections and epi stack of heterogeneous laser/amplifier, modulator and photodetectors, respectively.

The epi structures of those devices are carefully designed so that all the devices are compatible with same process. The LD/SOA epi has 3 InAlGaAs QWs with PL wavelength centered at 1545 nm; the EAM epi has 12 InAlGaAs QWs centered at 1485 nm; the PD epi has 400 nm InGaAs bulk layer as the absorber. Same contact layer

materials are used, so that same contact metal can be applied with one deposition for n or p contact.

Three types of III-V epi are selectively transferred into one die, as shown in the layout of the transceiver circuit in *Figure 5-6*. Over 400 functional components, including both passive and active components, were integrated into a system on the NoC chip.

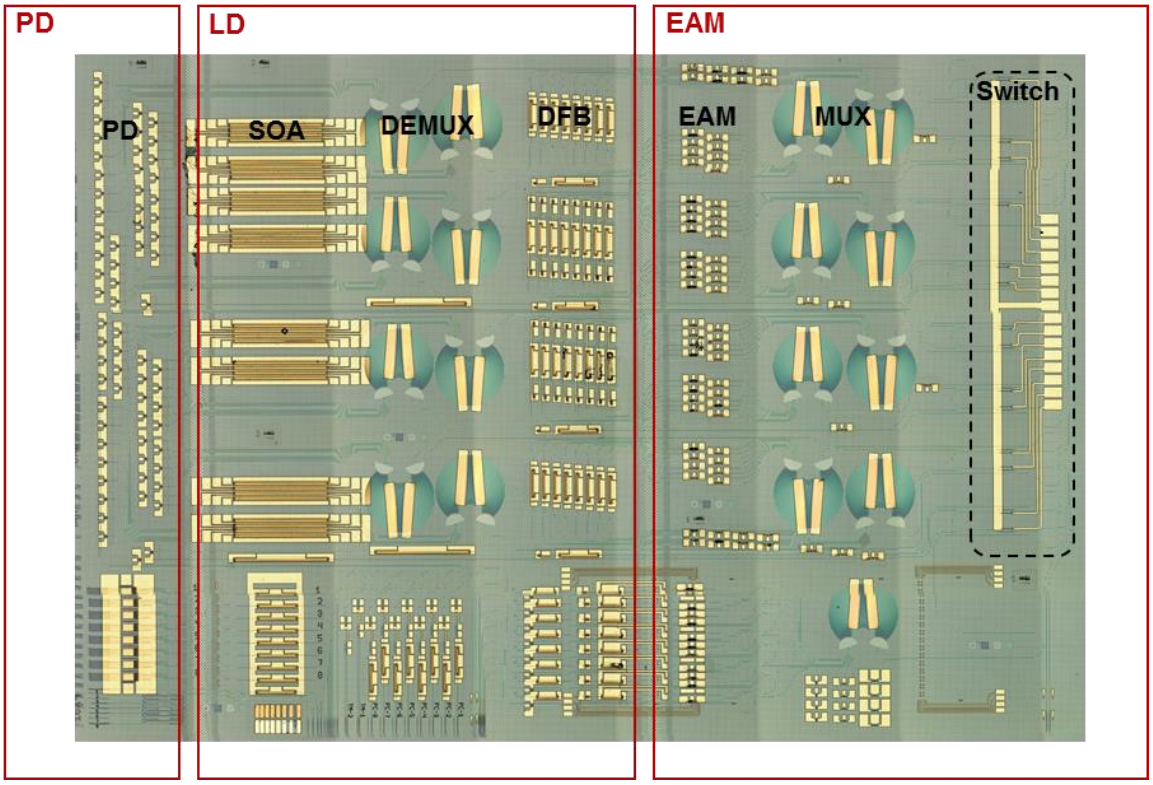


Figure 5-6. Microscope image of the photonic transceiver circuit. The red boxes indicate the locations of multiple die bonding.

The CMOS compatible fabrication of the NoC circuit has two major parts: silicon process (definition of surface type Bragg grating, silicon waveguide, edge coupler, optical switches and AWGs with a 4-inch process) and III-V process (die bonding and top-down III-V process for active components). The selective die bonding of three III-V

epis in a die is performed with the Finetech flip-chip bonder with precise alignment. The process details are summarized in Appendix A. All active and passive components were protected with 1 μm silicon oxide and 3 μm polymer before metallization to reduce capacitance and further improve the RF performance. *Figure 5-7* shows a microscope image of the chip after III-V die bonding, and SEM images of the dry etched mesa of the active devices. The process yield of passive components was close to 100%, and the overall yield was about 90% counting active and passive elements.

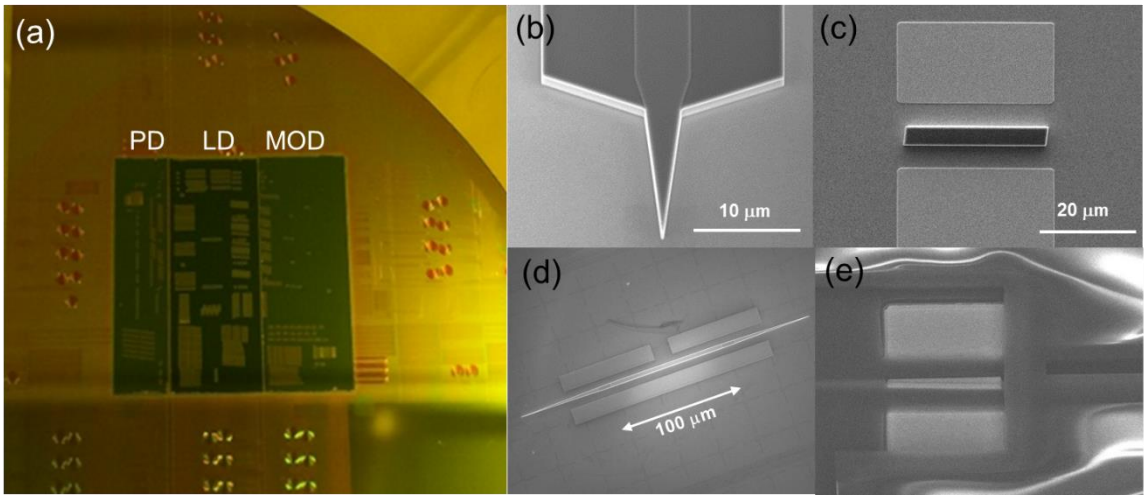


Figure 5-7. (a) Microscope image of the photonic chip after multiple die bonding and device mesa etch; and SEM images of (b) laser mesa with 20 μm taper; (c) PD mesa with n-contact metal; (d) EAM after mesa etch with 100 μm cavity and 60 μm tapers; (e) deep via in the thick polymer after surface planarization.

5.3 Device characterization

5.3.1 Individual device

The design and experimental results for each type of major components on the transceiver chip is described in detail as followed. The characterizations of individual

device are performed on the testing devices that locate on the transmitter chip, by coupling the light in/out the silicon waveguide with lens fibers.

(1) DFB laser

The heterogeneous DFB laser that is discussed in Chapter 3 is adopted in this photonic circuit design due to its low threshold and outstanding single mode operation. However, a major issue for the previous design is the poor thermal performance [4]. The short cavity DFB laser integrated on SOI substrate leads to a fast power roll-over at high injection. In this run, the cavity length is extended to 400 μm long to decrease the thermal impedance as well as the device series resistance. At the same time, 3 QWs instead of 7 QWs is used in the epi design, in order to depress the transparency current density as well as the threshold current. The SCH layers are constant InAlGaAs with PL wavelength at 1.25 μm. Most other layers are kept same as those shown in *Table 3-1*.

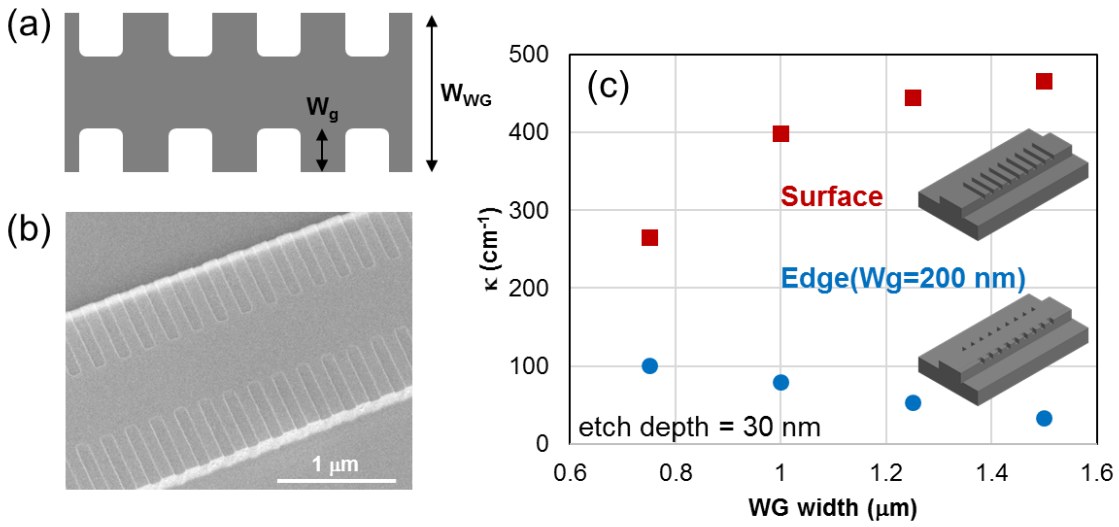


Figure 5-8. (a) Design of edge grating and (b) SEM image of silicon waveguide with edge grating; (c) compares the simulated grating strength of surface and edge grating with same etch depth.

A weaker Bragg grating is required to reach to reasonable effective reflections in the longer laser cavity. However, surface grating design, that is used in Chapter 3, tends to over-perturb the heterogeneous mode at the surface of the waveguide and cause strong grating strength. In this work, an edge type Bragg grating is designed, as shown in the *Figure 5-8*. Instead of a thorough line across the waveguide, corrugations are only defined at the edge of the waveguide, with another degree of freedom, grating width W_g, can be used to tune the grating reflection besides the etch depth and duty cycle. Figure 5-8(b) shows a SEM image of edge gratings on a silicon ridge waveguide.

Figure 5-8(c) compares the simulated grating strength, κ, of surface and edge grating with different silicon waveguide widths. By only overlapping with the tales of the optical mode in the III-V/Si cross-section, edge gratings with 400 nm W_g and 50% duty cycle have shown much weaker κ values with 30 nm etch depth on the silicon ridge waveguide (200 nm height). A precise alignment between grating and waveguide for edge gratings.

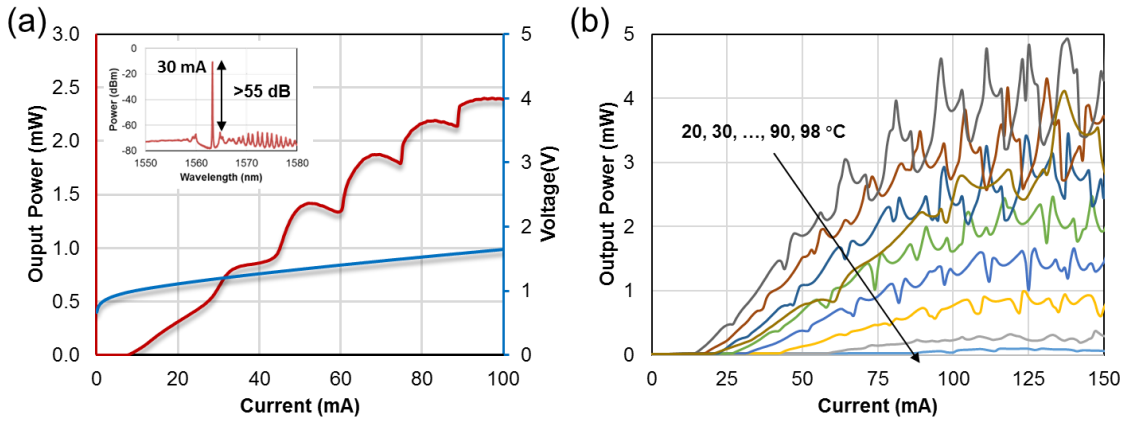


Figure 5-9. (a) L-I and I-V curves of 400 μm long heterogeneous DFB laser. Insert is the optical spectrum with 30 mA injection. (b) CW operation of a 400 μm long heterogeneous DFB laser at stage temperature up to 98 °C.

Figure 5-9(a) shows the L-I and I-V characteristics of heterogeneous DFB laser with 400 μm cavity and quarter wavelength shifted edge gratings at the III-V/Si interface. lengths under CW operation. The laser has a mesa with 26 μm width and 1 μm silicon waveguide, with 25-30 nm on the grating etch depth. The threshold current for the 400 μm DFB laser was measured to be 7.5 mA and it corresponds to a low threshold current density of 470 A/cm^2 at 20 °C. This shows an over 50% improvement compared with the 200 μm cavity DFB design that is demonstrated in Chapter 3. The spectra in the insert image indicates that DFB laser has single wavelength emission at wide wavelength range with a side mode suppression ratio (SMSR) over 55 dB. The kinks at the L-I curves relate to longitude mode hopping. In this run, the C-band heterogeneous DFB laser has a maximum CW lasing temperature up to 98 °C, as shown in the *Figure 5-9*(b). Besides the improvement on device thermal impedance and series resistance, modified 3-QWs design with better confinement with 1.25Q SCH layers is believed to improve the current injection efficiency at high ambient temperature.

(2) EA modulator

The modulator in the transceiver network circuit uses the EAM designs that is demonstrated in Chapter 4. Both the III-V epi and the process are modified to improve the performance. First, the epi design for the EAM is modified, with 12 layers of QWs with center PL moved to 1485 nm. The thickness of barrier is changed to 6 nm, and SCH layers both above and below the QWs are shrunk to 75 nm. This is to enhance the electric field in the wells with same voltage drop across the intrinsic layers, and to increase its optical absorption by increasing the mode confinement factor in the wells. The device fabrication is also optimized: (a) 600nm or 750 nm wide silicon waveguide

is defined by a DUV lithographic tool. The narrow waveguide further increases the mode confinement factor in the QWs; (b) 3 μm polymer planarization is applied to the chip before the final metallization step in order to decrease the parasitic capacitance of the large probe pads. The cavity length of the EAMs is set to 75 or 100 μm.

Figure 5-10(a) shows the transmission performance (TE polarization) of 100 μm long EAM at different reverse bias level from 0 to 6 V. Over 6 dB per 1 Vpp extinction ratio can be seen across 1550-1570 nm. Particularly, this maximum extinction ratio can be achieved with low bias voltage below 3 V, resulting from the new epi design. The small signal frequency response is shown in *Figure 5-10*(b). 3-dB bandwidth over 24 GHz is achieved on the EAM with a 75×2.5 μm^2 cavity. The insert shows its eye diagram for 25 Gbps operation with 1560 nm input light at 3.3 V reverse bias voltage. The clear eye shows its high-speed performance with error-free data transmission.

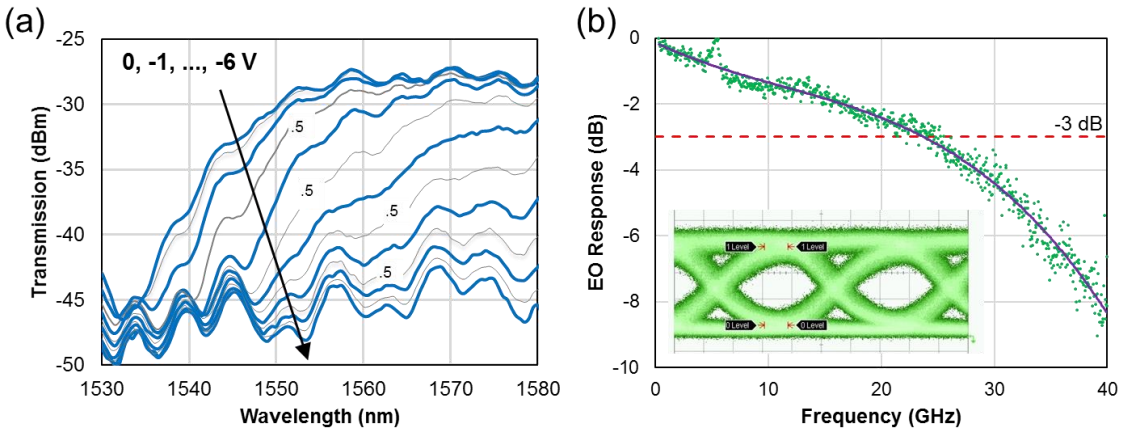


Figure 5-10. (a) Power transmission of 100×2.5 μm^2 EAM versus reverse bias from 0 to 6 V; (b) EO response of EAM with 75 μm cavity and 2.5 μm mesa width at 1560 nm wavelength and 2V reverse bias. Insert: eye diagram of 25 Gbps operation at 1560 nm wavelength and 3.3V reverse bias.

(3) Photodetector

A waveguide photodetector with a PIN structure photodetector structure is used in the heterogeneous receiver [9, 10]. The device structure is shown in *Figure 5-11*(a). The PIN junction with 400 nm InGaAs core is defined by dry etched mesa after III-V/Si bonding. Input single mode silicon waveguide is flared out to multimode waveguide with the same width of the photodetector. A constant waveguide width is used underneath the III-V mesa. The PD has a 7° slanted interface in order to eliminate unnecessary reflections back to input waveguide. Test devices with mesa widths of 2, 3, 4 and 8 μm and cavity length of 30, 50 and 100 μm are designed and fabricated on the transceiver chip.

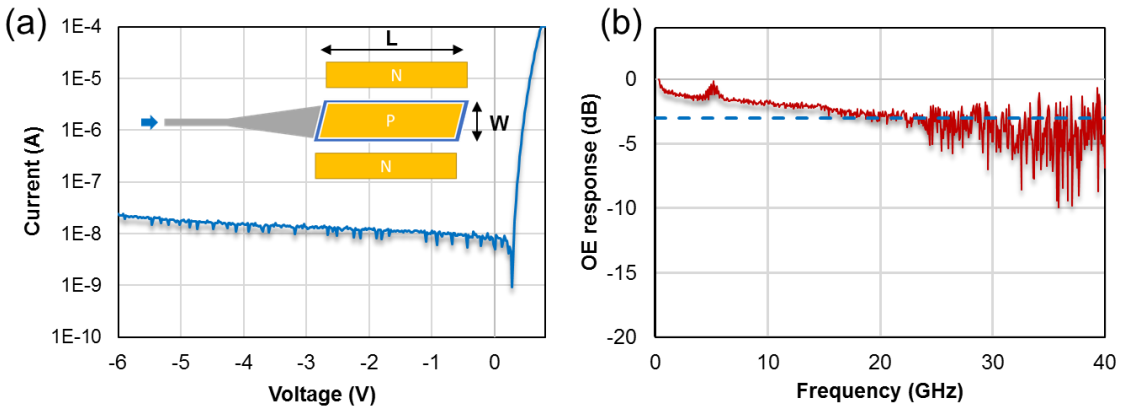


Figure 5-11. (a) Diagram of the heterogeneous PIN photodetector and its IV curve for PD with 4×30 μm²; (b) frequency response of heterogeneous PD with 4×30 μm².

A very low dark current of 10 nA at 2 V reverse voltage is achieved for the PD with 30 μm long and 4 μm wide mesa, as shown in the IV curve in *Figure 5-11*(a). The low dark current is mainly contributed by the optimized mesa dry etch and sidewall passivation process. Its frequency response show a flat response and a 3-dB bandwidth larger than 20 GHz. Internal responsivity of the photodetectors is measured at 1550

nm input light, as the results listed in *Table 5-2* for different device dimensions. The parasitic capacitance and resistance values, extracted from the S11 measurement, are also listed in the Table. Responsivity of the photodetectors with 30×4 μm^2 mesa is about 0.45, and a higher responsivity can be achieved with longer cavity. Efficiency of the waveguide photodetectors can be improved with further mode engineering, such as to squeeze the mode into absorber layer by tapering down the silicon waveguide.

Table 5-2. Responsivity and RC parameters of heterogeneous PIN PD

W (μm)	L (μm)	Responsivity (A/W)	Capacitance (fF)
2	50	0.48	38.6
2	75	0.56	54.8
2	100	0.66	71.5
3	30	0.43	46.9
4	30	0.45	38.9
8	30	0.79	130.3

(4) AWG

AWGs are widely used as a Mux or DeMux in the WDM system due to its good performance in dense channel wavelength routing and its design convenience [11-13]. As shown in *Figure 5-12*, the AWG includes three major parts: N×M port input/output (IO) waveguides, two star couplers with free propagation region (FPR), and the phase waveguide array with fixed phase difference. The design of the AWG used in this work follows the calculations in reference [13].

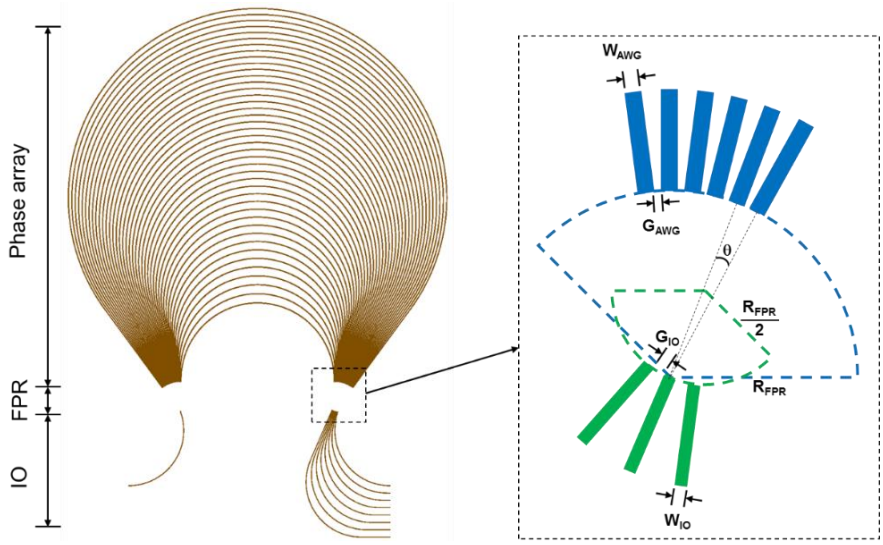


Figure 5-12. AWG design and layout in this work

The parameters for the 1×8 AWG used in this work are listed in *Table 5-1*. Partial etched ridge waveguide and 200 μm minimum bend radii were used for low propagation loss. The array waveguide is set to be certain width (1.2 μm) that is slight multimode for low loss and a low crosstalk [14]. The SEM images of processed AWG are shown in in *Figure 5-13*. The dimension of the 1×8 AWG is about 1.2 mm^2. A parabolic taper is used at the I/O waveguide to improve the channel uniformity [15]. Two major factors are considered to minimize the total insertion loss: (a) the gap width between two neighboring array waveguide, which blocks the mode coupling into the AWG. In this work this gap width is set to 200 nm, limited by the resolution of 248 nm DUV lithographic tool; (b) the propagation loss of silicon waveguide, which is not negligible due to the large footprint.

Table 5-3. Major parameters of 1×8 AWG design

General	T_{SOI}	500 nm
	T_{Ridge}	200 nm
	λ	1560 nm
	Δf	200 GHz
Array WG	N_{AWG}	127
	ΔL	17.471 μm
	W_{AWG}	1.2 μm
	G_{AWG}	200 nm
FPR	R_{FPR}	159.035 μm
IO WG	N_{IO}	1×8
	W_{IO}	1.2 μm
	G_{IO}	1.2 μm
	Taper	2 μm

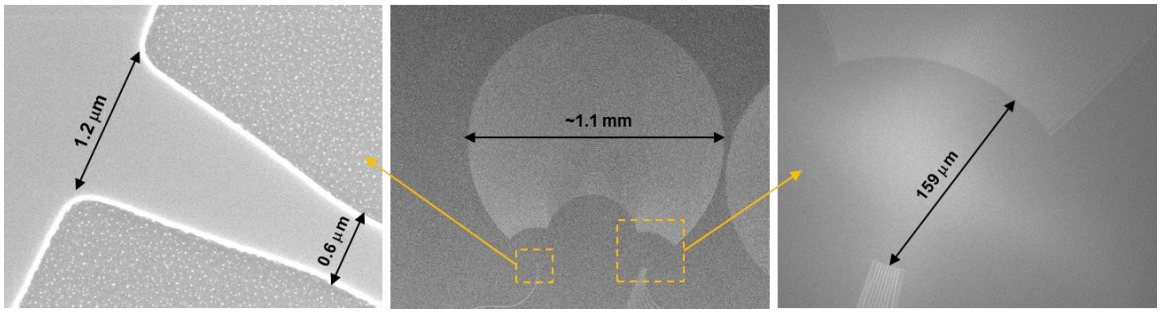


Figure 5-13. SEM images of silicon AWG after processing

The normalized transmission spectrum of the Si 1×8 AWG is shown in *Figure 5-14*. It shows a low insertion loss that is below 1.5 dB at center channels, and a below 1 dB non-uniformity among the eight channels; The crosstalk between different channels is as low as -28 dB. The average 3 dB optical bandwidth of each channel is about 0.62 nm, corresponding to about 75 GHz in the optical frequency domain.

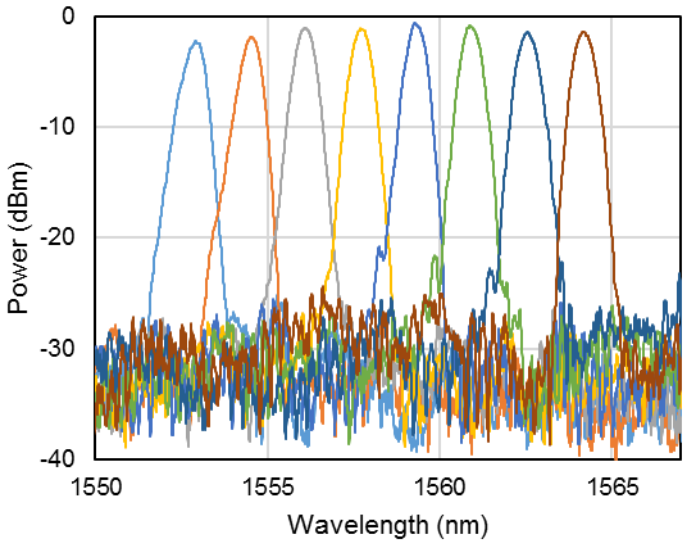


Figure 5-14. Normalized transmission spectrum of the 1×8 silicon AWG.

(5) Switch

A broadband optical switch is of great interest in an alignment free optical network or WDM system. Microelectromechanical systems (MEMS) based optical switches are normally broadband, but they have a large footprint and are difficult to integrate on chip [16]; Integratable ring resonator based switches have narrow bandwidth [17, 18]. Broadband optical switches are reported with MMI coupler or broadband 50% couplers based MZI switch [19, 20]; however, they are sensitive to fabrication imperfections. In this work, a novel adiabatic coupler MZI (ACMZI) switch is proposed as the data router for all WDM channels, which adopts the adiabatic coupler as the 3-dB power combiner/splitter in the MZI structure. This design yields an ultra-broadband optical switch on silicon with high tolerance to process variations.

In an adiabatic coupler, the two imbalanced arms need to be brought close gradually to avoid abrupt mode perturbation, then change the width up/down adiabatically with a constant gap width [21]. *Figure 5-15* shows a simulation of the

light propagation with 1550 nm wavelength and TE polarization with input to the adiabatic 3 dB power coupler from wide and narrow input ports, respectively. In the simulation, both the 700 nm and 500 nm port tapers to 600 nm within 400 μm coupling length with 300 nm gap width, resulting in an even power split. The difference is, as the mode propagation simulation shows in *Figure 5-15*, an even mode is excited in the AC when light entrance from wide port, so no phase difference between two outputs. However, the light entering from narrow port excites odd mode so there is π phase difference between output ports. The adiabatic coupler is simulated with commercial software [22], as shown in *Figure 5-15*.

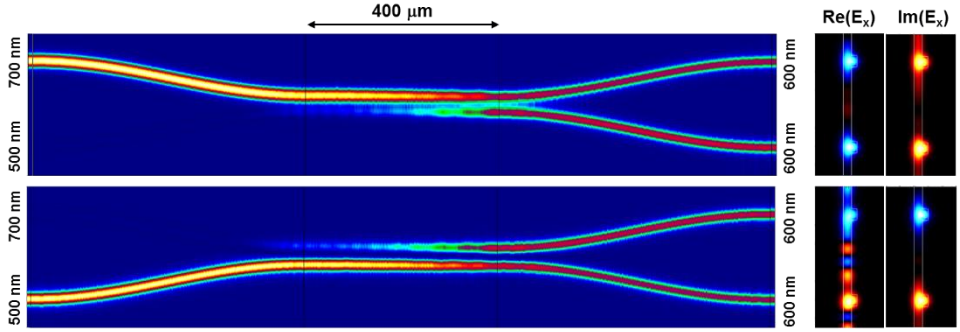


Figure 5-15. Simulations of light propagation in an adiabatic coupler

Figure 5-16 schematically shows the structure of the MZI switch with adiabatic couplers. Two 3 dB adiabatic couplers are connected back to back to form a symmetric interferometer structure. A thermal phase tuner on one arm is used to change the phase difference between two arms and control the switch. The device was fabricated together with the waveguide etch step. Therefore, the waveguide was partially etched with 200 nm ridge height and 300 nm slab thickness. Then 1 μm SiO_2 cap layer was deposited on the Si waveguide, isolating the 100 nm Ti/Pt heater metal from the silicon

waveguide. A 2 μm wide trench was etched on the silicon slab on both sides of the waveguide to improve the tuning efficiency of thermal phase tuner.

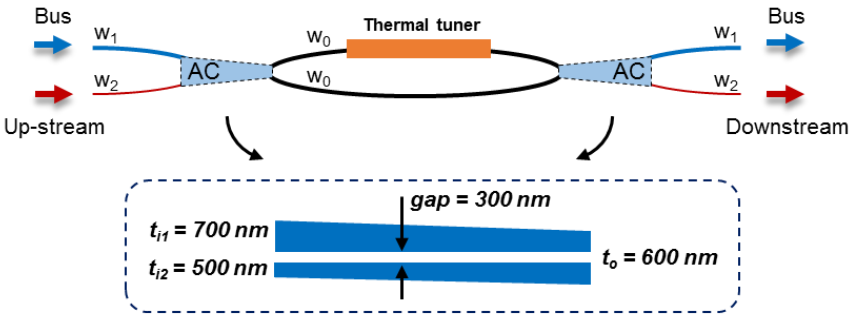


Figure 5-16. AC-MZI switch design in this work

The performance of AC-MZI switch is shown in Figure 5-17. It shows an extinction ratio (ER) larger than 16 dB over 80 nm wavelength range. From the tuning performance with a square wave signal, it has about 18 ms rise time which corresponds to a bandwidth of 30 kHz, which is limited by the footprint of the thermal phase tuner.

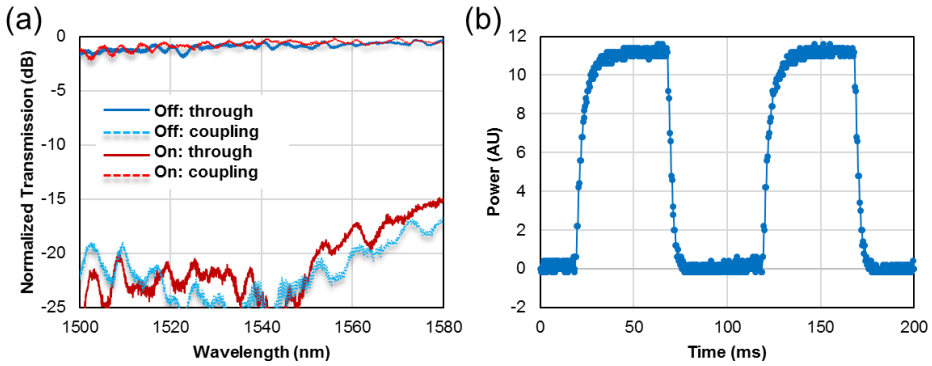


Figure 5-17. (a) Normalized transmission of AC-MZI switch and (b) response to 10 kHz square wave voltage driving

(6) Edge coupler

High off-chip coupling loss is one of the major sources of optical loss in inter-chip interconnects, and also a major barrier for low-cost package for photonic circuit.

Vertical coupling, such as grating coupler (GC), is widely used and low coupling loss up to 1.5 dB per coupling was reached with carefully design multi-level GC [23, 24]. However, a low reflection and low loss grating coupler design is not available for the SOI platform with 500 nm thick device layer. Instead, lateral edge coupling between the fiber and silicon waveguide is used in this work. But the coupling loss is high when coupling to a nano-scale silicon waveguide due to the large mode mismatch. Other optimizing techniques, such as waveguide mode convertor design [25-27], are not compatible with the thick device layer, which is necessary for efficient coupling between silicon and III-V/silicon sections in the heterogeneous silicon platform

In this work, a three-level inverse taper type mode convertor is designed to improve the light coupling efficiency on heterogeneous integrated circuit. As shown in *Figure 5-18*(a), the mode converter includes three sections: (a) transition from shallow etched ridge waveguide to fully etched stripe waveguide; (b) transition from stripe waveguide with 500 nm height to 300 nm height; (c) the waveguide with 300 nm height reversely tapers down to width below 200 nm. The insert figure in *Figure 5-18*(a) shows that a lower mode effective index n_{eff} can be achieved with 300 nm waveguide height, below 1.8 with waveguide width of 200 nm.

No ebeam lithography is required in this process. By calibrating the exposure energy in the DUV lithographic process, the inverse taper tip is controlled between 150 to 200 nm to avoid large propagation loss due to high sidewall roughness and substrate leakage. The waveguide at facet is 8 degree tilted to minimize the reflection. *Figure 5-18* (b) shows experimental results of coupling efficiency and reflection with different taper length and tip width. A minimum coupling loss is about 4.7 dB per

coupling for 225 nm taper tip width. The minimum reflection is about -20 dB for taper tip width below 200 nm. 50 μm long inverse taper has lowest coupling loss, with the trade-off between the taper transition efficiency and the waveguide propagation loss.

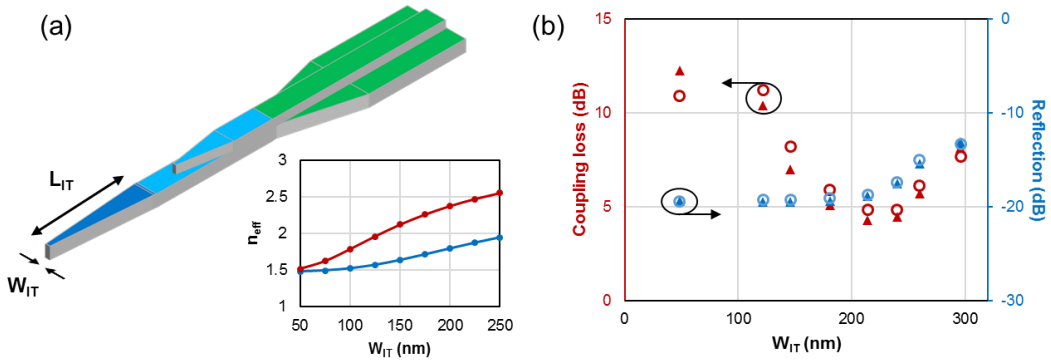


Figure 5-18. (a) Mode convertor on 500 nm SOI with (insert) the effective index change with waveguide width; (b) the coupling loss and reflection of mode convertor.

5.3.2 Transceiver circuit

The diagram in *Figure 5-19* shows the setup of the on-chip communication test. Due to lack of an appropriate driver circuit, only one channel is tested at a time. The switch array was driven by a multi-pin DC probe card to route the signal among transceivers. 50 Ω G-S-G probes are used to test modulators and photodetectors.

The DFB driving current and AWG heaters were adjusted appropriately to align the lasing wavelength to the transceiver channels. *Figure 5-20*(a) shows the parallel heater array on the AWG, with differential heater length in proportion to reciprocal of array waveguide index. The heater array can tune all the 8 channels simultaneously, as shown in *Figure 5-20*(b). However, this tuning is energy inefficient, with about 50 GHz/W power consumption mainly due to the heater design insulated from silicon waveguide.

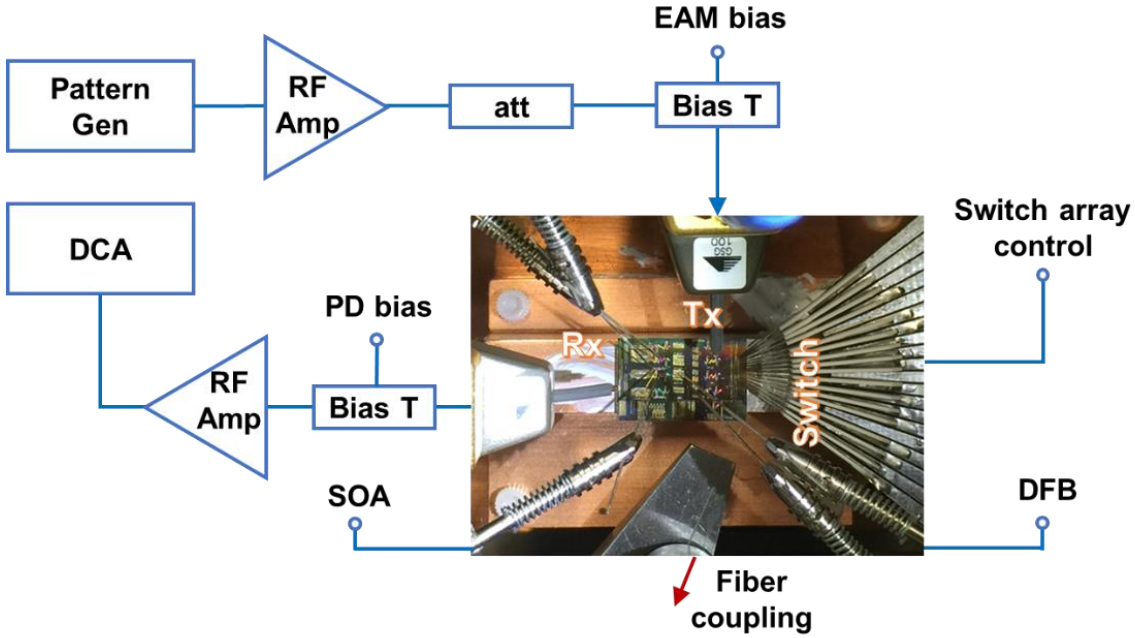


Figure 5-19. Setup for on-chip link test

Another approach to align the laser with the AWG channel is to tune the laser wavelength with injection current, as shown in *Figure 5-20*(c). With tuning both laser and AWG, eight DFB lasers with wavelength aligned to the corresponding AWG channels are shown in *Figure 5-20*(d). The missing channel was caused by a defective device on the chip. The manual wavelength alignment is performed by adjusting the driving currents of DFBs and the heater array on the AWG. It is noteworthy that the normalized transmission spectrum in *Figure 5-20*(b) and (d) is from two back-to-back 1×8 AWGs on one waveguide, representing an ultra-low total insertion loss below 3 dB through two AWGs in Tx and Rx.

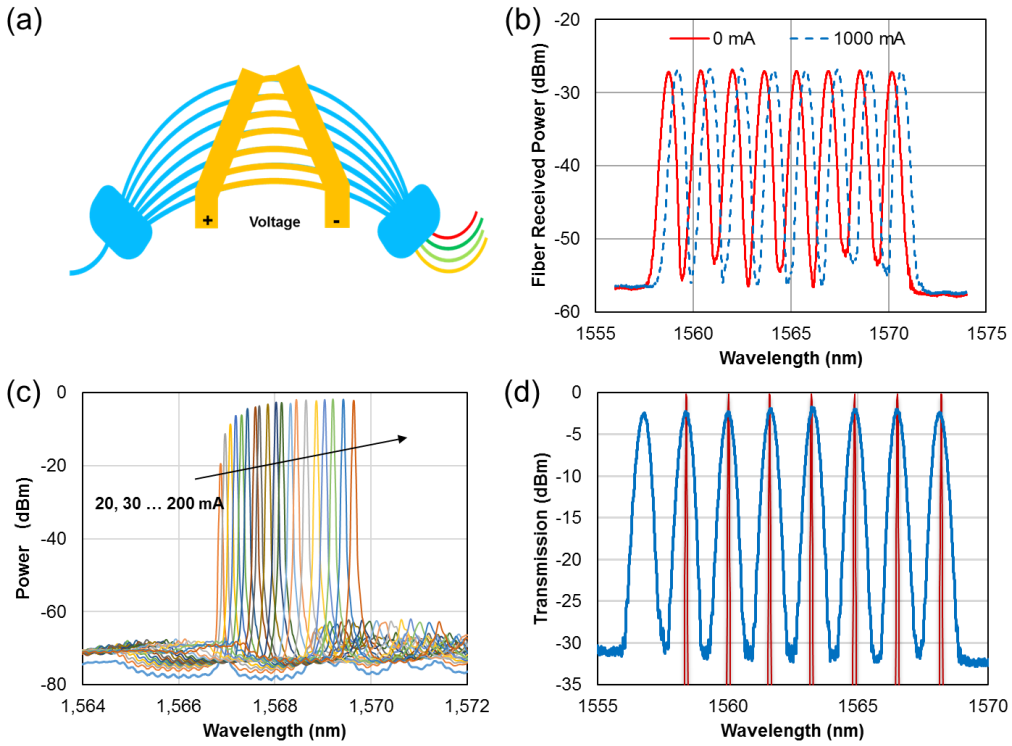


Figure 5-20. (a) Schematic diagram of AWG with differential thermal tuner; (b) transmission spectrum of back to back AWGs with thermal tuning; (c) output spectrum of 400 μm DFB laser with different injection current levels; and (d) the normalized wavelength of laser array aligned with the AWG channels.

It's worth noting that, the high-speed signal degenerates after the AWG MUX which has limited optical bandwidth. As shown in *Figure 5-21*(a), the optical spectrum filtering effect acts for NRZ data with certain carrier frequency (f_c) and modulation frequency (f_m) when it passes by an optical spectrum filter (Gaussian-like shape for AWG channels in this case). The sideband of the NRZ signal is truncated by the optical filter, causing degeneration in the frequency response of the transceivers. With the AWG transmission data of each channel that is shown in *Figure 5-14*, its frequency response can be calculated, showing a 3-dB bandwidth of about 26.5 GHz, as shown in *Figure 5-21*(b). A data-rate dependent bit error rate power penalty caused by this

spectrum filtering effect is about 0.25 dB and 0.52 dB for 25 Gbps and 50 Gbps, respectively, after each AWG that is used in the on-chip link in this work [28]. Here, zero-detuning between the laser wavelength and AWG channel wavelength is assumed.

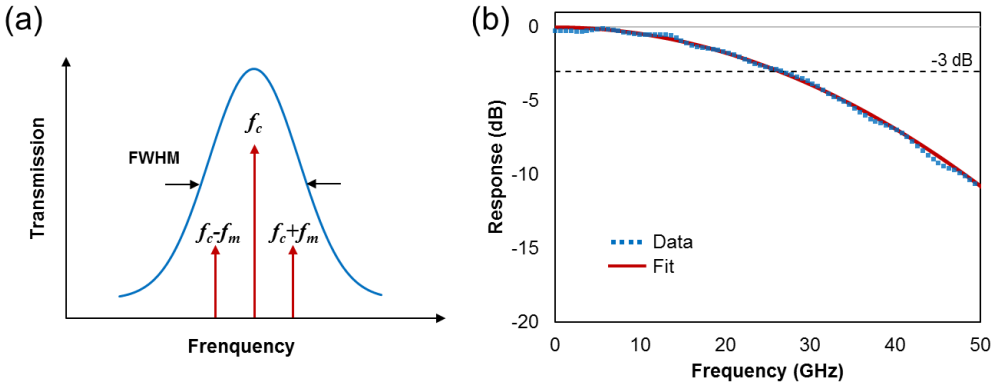


Figure 5-21. (a) Spectrum filtering effect in AWG channel as an optical band pass filter, the red arrows indicating the NRZ modulation signal; (b) calculated frequency response of one AWG optical channel.

The small signal modulation response of the modulator was tested together with the photodetector in the corresponding receiver, as shown in *Figure 5-22*(a). A 6-dB bandwidth of 24 GHz was observed for the EAM-PD link. This frequency response curve includes two 50 Ω RF probes that are on the modulator and photodetector. RF signal reflections are seen due to the impedance mismatch between probes and on-chip devices. The data transmission test was applied with a 40 GHz pattern generator and 2^7-1 PRBS signal with the setup shown in *Figure 5-19*. Two high-speed broadband microwave amplifiers are used to drive EAM and PD, and boost up the noise floor in the link. A data rate of 40 Gbps per channel performance is shown in *Figure 5-22*(b), with the vertical scale of 50 mV/div in the eye diagrams. The unsymmetrical eye patterns are due to the clock distortion from the pattern generator. Clear eyes can be seen up to 40 Gbps operation, which is the limit caused by the microwave amplifiers. The result

shows a potential large capacity of the transceiver array, with 320 (8×40) Gbps per transceiver node, and 2.56 Tbps (8×320 Gbps) for the whole photonic circuit. Further improvements are expected with integration of the photonic transceiver circuit with impedance matched CMOS driver circuit for low bit error rate operations.

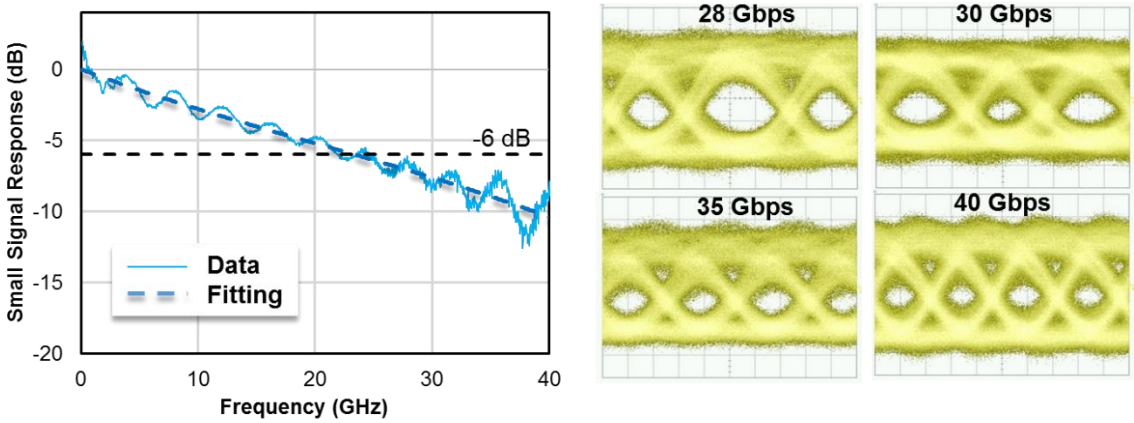


Figure 5-22. (a) Small signal frequency response of a Tx-Rx channel; (b) Eye diagram of on-chip communication from one channel.

In this demonstration of on-chip optical link, the power consumption of photonic circuit is dominated by the laser source, regardless the power consumed at the electrical driver side. The DC power consumption of the DFB laser shown in the data link in *Figure 5-22*(b) is about 1.5 pJ/bit at 70 mA injection and 40 Gbps operation. This can be improved by operating the laser source at lower pump current by optimizing the link power budget and bringing down the noise level in the testing. A dynamic laser power tuning is an effective way to save the energy consumption in practical application to control the laser output power according to the data transmission status. The high impedance modulator and photodetectors have about two orders of magnitude lower power consumption compared with laser. However, power drained

to their high-speed CMOS drivers takes a larger proportion in the total energy cost of the integrated transceiver chip.

5.4 Summary

In this chapter, we show breakthrough results on a fully integrated photonic interconnection circuit on silicon. With heterogeneous integration of III-V materials on Si, a fully integrated reconfigurable NoC circuit was demonstrated on a silicon chip, realizing an 8-nodes ring-type WDM system, with a large capacity transceiver system up to 8×8×40 Gbps. This heterogeneous integration technique promises a solution for future low cost and large bandwidth chip level interconnects.

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Chapter 6

Summary and future work

6.1 Summary of this thesis

This thesis has demonstrated that the heterogeneous integration platform on silicon is well suited for the application of photonic integration for optical interconnects. The ability to integrate different materials on silicon to extend the functionality and complexity of silicon photonics is the key advantage that enables highly integrated photonic circuits and large bandwidth density data transmission. In this thesis, the accomplishments of each chapter are summarized below.

In Chapter 2, the methods of heterogeneous integration with wafer bonding were discussed. The plasma-assisted bonding approach with outgassing channels ensured a high process yield in material transfer process. In addition, experiments were carried out to overcome the thermal budget limit of the heterogeneous system. By carefully designing the III-V layer stack and outgassing channel format, high-temperature anneal test and epitaxial regrowth were successfully performed on bonded III-V layers on silicon. In this way, the epitaxy method can be brought into the heterogeneous

integration platform, as an extra degree of freedom in designing and fabricating the optoelectronic devices.

In Chapter 3, a low threshold and high speed DFB laser on silicon was demonstrated. Quantum wells based active materials were transferred to patterned silicon waveguides with a surface Bragg grating, resulting in a single mode CW operation with high side mode suppression over 55 dB, and threshold currents as low as 8.8 mW for a 200 μm cavity length. Additionally, a novel thermal-shunt design was demonstrated for the heterogeneous micro-ring lasers in order to overcome the thermal barrier of the thick BOX layer in SOI substrates. About 40% improvement of thermal impedance of the ring lasers on silicon was achieved with a record high CW operation temperature up to 105 °C.

Two types of heterogeneous modulator were demonstrated in Chapter 4 for different applications. First, lumped EA modulators on silicon were designed and fabricated for low-power data transmission in the C band. Over 6 dB ER per 1 V_{pp} bias swing was achieved as well as large bandwidth up to 19.5 GHz. The photonic circuit was successfully integrated with a CMOS driver circuit by a flip-chip bonding method and reached 8 × 12.5 Gbps operation. Second, we demonstrated III-V/Si Mach-Zehnder modulators with superior linearity, which is essential for analog photonic links. By compensating the MZI nonlinear transfer function with multiple EO effects in the III-V and Si materials, even with extra tuning freedom from coupled-ring design on each arm of the MZI, state-of-art linearized modulators on silicon were achieved with high SFDR up to 117.5 $dB \cdot Hz^{2/3}$.

In Chapter 5, a fully integrated transceiver network circuit was demonstrated with the key building blocks proposed in previous chapters. This circuit is enabled by the heterogeneous integration with co-processing of the laser, modulator, photodetector and other elements. With over 400 total devices in a single circuit, the WDM transceiver network includes 8 nodes and 8 wavelength channels in each channel, giving a total data transmission capacity up to 2.56 Tbps. This photonic integrated circuit has shown the potential application of heterogeneous integration in the application of chip-level interconnects.

To summarize, we believe that the research in this thesis has shown the great advantages of the heterogeneous integration method, which make it one of the most competitive candidates for high-performance and low-cost photonic integration. Practically, being compatible with the fabrication techniques on Si and III-V materials, heterogeneous integration has a low technical barrier to be transferred to a foundry for large scale fabrication. *Figure 6-1* shows the "Moore's Law" in the field of photonic integration. Silicon photonics, especially the heterogeneous integration with a full library of active devices on silicon, has shown faster growth rate than the traditional III-V photonic integration. We believe that heterogeneous silicon integration has broad prospects, especially when the unit price dominates the application, such as optical interconnection in short distance up to on-chip communication.

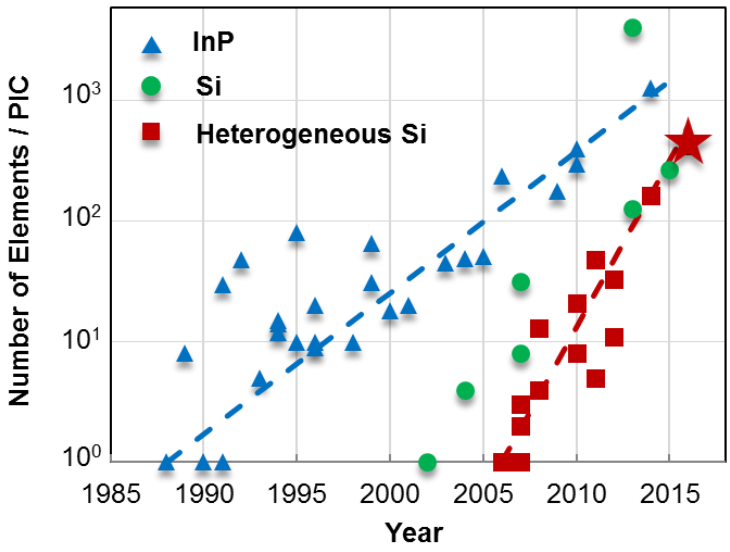

Figure 6-1. Moore's law of development of photonic integration with different material platforms. The star is the network on chip described in Chapter 5.

6.2 Outlook of future work

Besides further improvements to the critical devices that are discussed in this thesis, such as improvement of wall plug efficiency of on-chip laser sources and the reduction of the loss of modulators, there are a few major aspects of the heterogeneous integration platform that require improvement before it can become a mature technology. First, the III-V wafer cost is still counted in the total cost of the circuit process. Even though this part can be minimized by selective bonding III-V dies to the active device area, it limits the scaling-up of the high-volume device fabrication on large wafers. Second, the thermal performance of the heterogeneous device on the SOI wafer needs further improvement for uncooled operation. Third, packaging of photonic circuit is a major obstacle. In particular, the co-package with electrical circuit will be the major focus of the future developments. Therefore, the research directions shown below are worth considering.

1. Epitaxy on Si

As discussed in Chapter 1, epitaxial growth on a large silicon wafer is of great interest to lower the cost of high performance functional materials. Recent breakthroughs in growing QDs on silicon have shown encouraging results that promises for an integratable laser source on silicon with low threshold current density and good lifetime [2, 3]. However, one major remaining difficulty is the optical coupling between the grown gain materials with the silicon waveguides.

As we have shown in Chapter 2, epitaxial regrowth provides another possibility for large scale III-V deposition on silicon. Transferring only a thin layer of III-V material (such as thin InP layer) can be used as a template for epitaxial regrowth. The III-V substrate can be saved for reuse if it is combined with the so called "smart-cut" bonding technique [4].

2. Athermal design and feedback circuit

In the WDM system, the laser wavelength has to be carefully aligned with the channel wavelength, in order to minimize the insertion loss and total power consumption. However, the operation ambient temperature of the photonic circuit may be as high as 80-100 °C in a server cabinet or integrated with a processor chip, which results in a large wavelength shift and degradation in efficiency. A low-cost optical link cannot afford a power-hungry TEC circuit.

Athermal design will be important for the uncooled operation of the optical transceiver circuit. Passive athermal design could use special materials with thermal expansion coefficient of different signs to compensate over the total effective device

length [5]. An active athermal design has feedback controlling circuit to actively align the channels among different units [6].

3. Integration with CMOS circuit

Silicon photonic interconnects that are 3D integrated with electronic integrated circuits (EICs) have the potential to overcome the I/O bottleneck of copper interconnects and achieve high-speed and cost-effective chip level photonic interconnects to enable future exascale performance computers and datacenters [7, 8]. For instance, the active athermal transceiver design would be more flexible with integrated optical-electronic circuit design. Combined with thermal path optimization on a thermal sink and 3-D integration of the driver circuit, the thermal performance of heterogeneous transceivers can be improved over a large range of ambient temperatures.

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Appendix

A. Process flow of heterogeneous integrated transceiver circuit

The transceiver circuit process, as shown below, is optimized for selective die bonding and the parallel fabrication of multiple devices such as laser, modulator and photodetector. Process for individual type of device such as that discussed in Chapter 3 and 4 might be simplified or modified for performance or yield purposes. The process flow is schematically shown in *Figure A-1*.

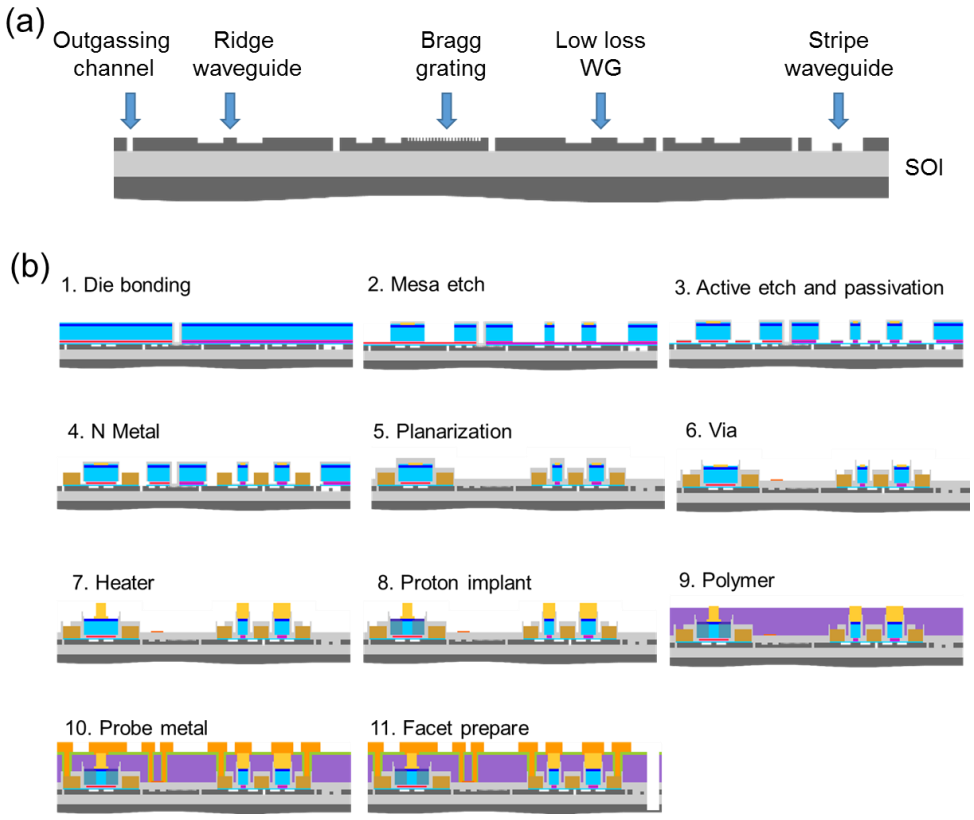

Figure A-1. Fabrication steps of (a) SOI and (b) III-V/Si process.

All the process steps listed are performed in the fabrication facility at UC Santa Barbara except the proton implant step. Lithography tools include an EBL lithography tool (JEOL JBX-6300FS), an i-line stepper (GCA 200) and a DUV stepper (ASML PAS 5500/300). The process is performed on a 4-inch wafer base for DUV lithography and then diced into small chips for i-line lithography.

1. SOI wafer preparation and alignment mark etch

Clean:

- 1165, solvent, Piranha at 80 °C, 10 min
- BHF dip 10-20 second to remove native oxide, DI rinse 1 min

Lithography:

- Dehydration bake at 150 °C
- Spin AR_2-600, 3500 rpm, bake at 220 °C for 3 min
- Spin UV6 0.8, 5000 rpm, bake at 135 °C for 1min
- Exposure in ASML, NA=0.63, 0.8/0.4, does=19 mJ/cm^2, focus offset=0
- PEB 135 °C for 90 sec
- Develop in AZ300MIF for 20 sec, no agitation, DI rinse 1 min
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

Dry etch:

- DRIE, Manual O_2 clean with Silicon wafer with SiO_2 coat, 825 W for 30 min
- Season the chamber, 30 min
- Etch with $C4F_8/SF_8$/AR = 54/26/20 sccm, 6 min 30 sec
- Strip resist in 1165 at 80 °C for 20 min

2. Bragg gratings

Clean:

- Piranha at 80 °C, 10 min
- BHF dip 10-20 second to remove native oxide, DI rinse 1 min

Lithography:

- Dehydration bake at 150 °C
- Spin CSAR (1:1), 3000 rpm, bake at 180 °C for 5 min
- Coat 10 nm Au film with thermal evaporation
- Exposure in EBL, current = 500 pA, with automatic mark detection, step=4 nm
- Au etchant to remove Au film
- Develop in MIKB:ISO=1:1 for 1 min, no agitation
- Rinse in MIKB:ISO=9:1 for 20 sec, no agitation

- O_2 descum in PEII, 300 sccm/100 W for 7 sec

Dry etch:

- DRIE, Manual O_2 clean with Silicon wafer with SiO_2 coat, 825 W for 30 min
- Season the chamber, 30 min
- Etch with $C4F_8/SF_8$/AR = 54/26/20 sccm, 16 sec
- Strip resist in 1165 at 80 °C for 20 min

3. Ridge waveguide etch

Clean:

- Piranha at 80 °C 10 min
- BHF dip 10-20 second to remove native oxide, DI rinse 1 min

Lithography:

- Dehydration bake at 150 °C
- Spin AR2-600, 3500 rpm, bake at 220 °C for 3 min
- Spin UV6 0.8, 5000 rpm, bake at 135 °C for 1 min
- Exposure in ASML, NA=0.63, 0.8/0.4, does=23 mJ/cm^2, focus offset=0
- PEB 135 °C for 90 sec
- Develop in AZ300MIF for 20 sec, no agitation, DI rinse 1 min
- Reflow at hotplate, 140 °C for 3 min
- O_2 RIE etch, 20 sccm/100 W for 30 sec

Dry etch:

- DRIE, Manual O_2 clean with Silicon wafer with SiO_2 coat, 825 W for 30 min
- Season the chamber, 30 min
- Etch with $C4F_8/SF_8$ = 60/30 sccm, with laser monitor
- Strip resist in 1165 at 80 °C for 20 min

4. Strip waveguide etch

Clean:

- Piranha at 80 °C, 10 min
- BHF dip 10-20 second to remove native oxide, DI rinse 1 min

Lithography:

- Dehydration bake at 150 °C
- Spin AR2-600, 3500 rpm, bake at 220 °C for 3 min
- Spin UV6 0.8, 5000 rpm, bake at 135 °C for 1 min
- Exposure in ASML, NA=0.63, 0.8/0.4, does=23 mJ/cm^2, focus offset=0
- PEB 135 °C for 90 sec
- Develop in AZ300MIF for 20 sec, no agitation, DI rinse 1 min
- Reflow at hotplate, 140 °C for 3 min
- O_2 RIE etch, 20 sccm/100 W for 30 sec

Dry etch:

- DRIE, Manual O_2 clean with Silicon wafer with SiO_2 coat, 825 W for 30 min
- Season the chamber, 30 min
- Etch with $C4F_8/SF_8$ = 60/30 sccm, with laser monitor
- Strip resist in 1165 at 80 °C for 20 min

5. Die bonding

SOI Clean:
- Piranha at 80 °C, 10 min
- BHF dip 10-20 second to remove native oxide, DI rinse 1 min
- Bake on hotplate, 150 °C, 5 min

InP chip clean:
- Remove coating in developer
- Rinse and gently swab with diluted Tergitol
- Remove InGaAs cap layer if necessary

Bonding:
- Plasma activation in EVG chamber, 100/50 W, 0.2 mBar, 30 sec
- Align the III-V chips to the target position on SOI die with the gap between two chips larger than 50 μm
- Clamp the bonded wafer in fixture, anneal at 300 °C for 2 hours
- Protection SiO_2 deposition, 600 nm
- Remove InP substrate with mechanical polish and selective wet etch

6. Pre-metal on mesa

Clean:
- Solvent clean, DI rinse 1 min
- Wet etch to remove the InP cap layer above the InGaAs contact layer

Lithography:
- Dehydration bake at 150 °C
- Spin PMGI SF5, 5000 rpm, bake at 190 °C for 2 min
- Spin second layer of PMGI SF5, 5000 rpm, bake at 190 °C for 2 min
- Spin UV6 0.8, 5000 rpm, bake at 135 °C for 1min
- Exposure in ASML, NA=0.63, 0.8/0.4, does=17 mJ/cm^2, focus offset=0
- PEB 135 °C for 90 sec
- Develop in AZ300MIF for 40 sec, no agitation, DI rinse 1 min
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

Metal deposition:
- Remove native oxide in HCl:DI=1:10, 30 sec, DI rinse
- Vacuum < 3×10^{-6} Torr in Ebeam evaporation chamber
- Pd/Ti/Pd/Au/Ti = 3 nm/17 nm/17 nm/103 nm/10 nm
- Lift off the metal layer in 1165, at 80 °C

7. Mesa etch

Clean:

- Solvent clean, DI rinse 1 min

Hard mask deposition:

- Sputter, 200 nm SiO_2

Lithography:

- Dehydration bake at 150 °C
- Spin AR2-600, 3500 rpm, bake at 220 °C for 3 min
- Spin UV6 0.8, 5000 rpm, bake at 135 °C for 1 min
- Exposure in ASML, NA=0.63, 0.8/0.4, does=16 mJ/cm^2, focus offset=0
- PEB 135 °C for 90 sec
- Develop in AZ300MIF for 20 sec, no agitation, DI rinse 1 min
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

HM etch:

- ICP etch, $CF_4/CHF_3/O_2$=5/35/5 sccm, 500/50 W, 0.5 Pa, 20% over etch
- O_2 ash, 500 W, 50 sccm, 20 min
- Strip photoresist in 1165, at 80 °C

III-V etch:

- Remove native oxide layer in HCl:DI=1:10, 1 min
- RIE etch Methane/H_2/Ar=4/20/10 sccm, 75 mTorr, 500 V, with laser monitor
- O2 plasma clean, 20 sccm, 125 mTorr, 300V, 20 min

8. Active region etch

Clean:

- Solvent clean, DI rinse 1 min

Lithography:

- Dehydration bake at 150 °C
- Spin HMDS, 4000 rpm
- Spin SPR955-1.8, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.5 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 60 sec, with agitation, DI rinse 1 min
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

III-V etch:

- H_3PO_4:H_2O_2:DI = 1:5:15, 45 sec, DI rinse 1 min
- Strip photoresist in 1165, at 80 °C

9. N contact metal

Clean:
Solvent clean, DI rinse 1 min

Lithography:

- Dehydration bake at 150 °C
- Spin PMGI SF15, 3000 rpm, bake at 190 °C for 2 min
- Spin SPR955-1.8, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.65 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 60 sec, with agitation, DI rinse 1 min
- DUV flood exposure, and develop until clear undercut in the bi-layer
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

Metal deposition:

- Remove sacrificial layer in H_3PO_4:H_2O_2:DI = 1:5:15, 45 sec, DI rinse
- Vacuum < 3×10^{-6} Torr in Ebeam evaporation chamber
- Pd/Ge/Pd/Au/Ti = 10 nm/110 nm/25 nm/1000 nm/10 nm
- Lift off the metal layer in 1165, at 80 °C

10. n-InP etch

Passivation:

- Remove native oxide layer in HCl:DI=1:10, 1 min
- ALD deposition, Al_2O_3, 30 nm, 130 °C

Lithography:

- Dehydration bake at 150 °C
- Spin HMDS, 4000 rpm
- Spin SPR955-1.8, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.5 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 60 sec, with agitation, DI rinse 1 min
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

HM etch:

- ICP etch of Al_2O_3, CHF_3=40 sccm, 900/100 W, 2 Pa, 20% over etch
- O_2 ash, 500 W, 50 sccm, 20 min
- Strip photoresist in 1165, at 80 °C

III-V etch:

- RIE etch Methane/H_2/Ar=4/20/10 sccm, 75 mTorr, 500V, with laser monitor
- O2 plasma clean, 20 sccm, 125 mTorr, 300V, 20 min

11. III-V clear

Lithography:

- Dehydration bake at 150 °C
- Spin HMDS, 4000 rpm
- Spin SPR220-7, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.5 sec
- PEB 110 °C for 90 sec
- Develop in AZ300MIF for 3 min, with agitation, DI rinse 1 min
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

III-V stack wet etch (repeat until IIIV is cleared):

- Oxide HM etch: BHF
- Metal etch: Au etchant type TFA
- InP etch: H_3PO_4:HCl=3:1
- InGaAs/ InGaAsP/AlGaInAs etch: H_3PO_4:H_2O_2:DI =1:5:15
- O2 plasma clean, 20 sccm, 125 mTorr, 300V, 20 min

12. Oxide protection and via etch

Passivation:

- Sputter, SiO_2, 1000 nm

Lithography:

- Dehydration bake at 150 °C
- Spin HMDS, 4000 rpm
- Spin SPR220-3, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.76 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 75 sec, with agitation, DI rinse 1 min
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

SiO_2 etch:

- ICP etch of Al_2O_3, CHF_3=40 sccm, 900/100 W, 2 Pa, 20% over etch
- O_2 ash, 500 W, 50 sccm, 30 min
- Strip photoresist in 1165, at 80 °C

13. P contact metal

Clean:

- Solvent clean, DI rinse 1 min

Lithography:

- Dehydration bake at 150 °C
- Spin PMGI SF15, 3000 rpm, bake at 190 °C for 2 min
- Spin SPR955-1.8, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.65 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 60 sec, with agitation, DI rinse 1 min
- DUV flood exposure, and develop until clear undercut in the bi-layer

- O_2 descum in PEII, 300 sccm/100 W for 60 sec

Metal deposition:
- Remove native oxide in HCl:DI = 1:10, 60 sec, DI rinse
- Vacuum < 3×10^{-6} Torr in Ebeam evaporation chamber
- Pd/Ti/Pd/Au/Ti = 3 nm/17 nm/17 nm/1500 nm/10 nm
- Lift off the metal layer in 1165, at 80 °C

14. Proton implant

Lithography:
- Dehydration bake at 150 °C
- Spin PMGI SF15, 3000 rpm, bake at 190 °C for 2 min
- Spin SPR330-3, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.68 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 75 sec, with agitation, DI rinse 1 min
- DUV flood exposure, and develop until clear undercut in the bi-layer
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

Proton implant:

(1)10 keV 5e13 cm-2
(2) 35 keV 8e13 cm-2
(3) 70 keV 9e13 cm-2
(4) 110 keV 1e14 cm-2
(5) 150 keV 1e14 cm-2
(6) 160 keV 8e13 cm-2
(7) 170 keV 8e13 cm-2

- Lift off the metal layer in 1165, at 80 °C

15. Insulation etch

Lithography:
- Dehydration bake at 150 °C
- Spin PMGI SF15, 3000 rpm, bake at 190 °C for 2 min
- Spin SPR955-1.8, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.65 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 60 sec, with agitation, DI rinse 1 min
- DUV flood exposure, and develop until clear undercut in the bi-layer
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

Wet etch:
- InGaAs etch: H_3PO_4:H_2O_2:DI =1:5:15, 20 sec, verify the etch depth with microscope
- Lift off the metal layer in 1165, at 80 °C

16. Thermal heater metal

Clean:

- Solvent clean, DI rinse 1 min

Lithography:

- Dehydration bake at 150 °C
- Spin PMGI SF8, 3000 rpm, bake at 190 °C for 2 min
- Spin SPR955-1.8, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.65 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 60 sec, with agitation, DI rinse 1 min
- DUV flood exposure, and develop until clear undercut in the bi-layer
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

Metal deposition:

- Vacuum < 3×10^{-6} Torr in Ebeam evaporation chamber
- Ti/Pt/Ti = 10 nm/100 nm/10 nm
- Lift off the metal layer in 1165, at 80 °C

17. Planarization metal deposition

Clean:

- Solvent clean, DI rinse 1 min

Lithography:

- Dehydration bake at 150 °C
- Spin PMGI SF15, 3000 rpm, bake at 190 °C for 2 min
- Spin SPR955-1.8, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.65 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 60 sec, with agitation, DI rinse 1 min
- DUV flood exposure, and develop until clear undercut in the bi-layer
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

Metal deposition:

- Vacuum < 3×10^{-6} Torr in Ebeam evaporation chamber
- Ti/Au/Ti = 10 nm/1500 nm/10 nm
- Lift off the metal layer in 1165, at 80 °C

18. Polymer planarization

Polymer:

- Sticking layer deposition, Sputter, SiN_x, 100 nm
- Dispense AP3000 and wait for 30 sec, spinning at 3500 rpm
- Bake at 150 °C for 30 sec
- Spin BCB 3022-46, 3000 rpm (for ~3um thickness)
- Let the sample sit in air for ~ 10 mins

- Place in blue oven with following recipe
- 5 min ramp time to 50degC, 5 min soak time at 50degC
- 15 min ramp time to 100degC, 15 min soak time at 100degC
- 15 min ramp time to 150degC, 15 min soak time at 150degC
- 60 min ramp time to 250degC, 60 min soak time at 250degC
- Blank ICP ash to roughen surface, CF4/O2 = 25/100 sccm, 500 W, 1 min
- Sticking layer deposition, Sputter, SiN_x, 100 nm

Lithography:
- Dehydration bake at 150 °C
- Spin HMDS, 4000 rpm
- Spin SPR220-3, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exp time=0.68 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 75 sec, with agitation, DI rinse 1 min
- DUV flood exposure, and develop until clear undercut in the bi-layer
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

Via etch:
- ICP etch, CF_4/O_2 = 10/50 sccm, 50/500 W, until via cleared
- O_2 ash, 500 W, 50 sccm, 30 min
- Strip the photoresist in Acetone, Isopropyl/DI rinse

19. Probe metal pads

Clean:
- Solvent clean, DI rinse 1 min

Lithography:
- Dehydration bake at 150 °C
- Spin PMGI SF15, 3000 rpm, bake at 190 °C for 2 min
- Spin SPR955-1.8, 3000 rpm, bake at 110 °C for 90 sec
- Exposure in i-line stepper, exposure time=0.65 sec
- PEB 110 °C for 90 sec
- Develop in AZ726MIF for 60 sec, with agitation, DI rinse 1 min
- DUV flood exposure, and develop until clear undercut in the bi-layer
- O_2 descum in PEII, 300 sccm/100 W for 60 sec

Metal deposition:
- Vacuum < 3×10^{-6} Torr in Ebeam evaporation chamber
- Ti/Au = 10 nm/1500 nm
- Lift off the metal layer in Acetone, Isopropyl/DI rinse

20. Sample diced, facet prepared for chip testing